

### ● General Description

The AGM60P06S combines advanced trench MOSFET technology with a low resistance package to provide extremely low  $R_{DS(ON)}$ .

This device is ideal for load switch and battery protection applications.

### ● Features

- Advance high cell density Trench technology
- Low  $R_{DS(ON)}$  to minimize conductiveloss
- Low Gate Charge for fast switching
- Low Thermal resistance

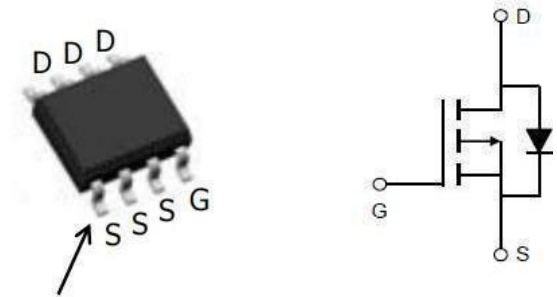
### ● Application

- MB/VGA Vcore
- SMPS 2<sup>nd</sup> Synchronous Rectifier
- POL application
- BLDC Motor driver

### Product Summary

BVDSS	RDSON	ID
-60V	48mΩ	-5.7A

### SOP-8 Pin Configuration



### Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
AGM60P06S	AGM60P06S	SOP8	----	----	3000

**Table 1. Absolute Maximum Ratings (TA=25°C)**

Symbol	Parameter	Value	Unit
VDS	Drain-Source Voltage (VGS=0V)	-60	V
VGS	Gate-Source Voltage (VDS=0V)	±20	V
ID	Drain Current-Continuous(TA=25°C) <b>(Note 1)</b>	-5.7	A
	Drain Current-Continuous(TA=100°C)	-2.6	A
IDM (pluse)	Drain Current-Continuous@ Current-Pulsed <b>(Note 2)</b>	-22.8	A
PD	Maximum Power Dissipation(TA=25°C)	2.5	w
	Maximum Power Dissipation(TA=100°C)	1.0	w
EAS	Avalanche energy <b>(Note 3)</b>	18	mJ
TJ,TSTG	Operating Junction and Storage Temperature Range	-55 To 150	°C

**Table 2. Thermal Characteristic**

Symbol	Parameter	Typ	Max	Unit
RθJA	Thermal Resistance Junction-ambient (Steady State) <sup>1</sup>	---	50	°C/W

**Table 3. Electrical Characteristics (TA=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>On/Off States</b>						
BVDSS	Drain-Source Breakdown Voltage	VGS=0V ID=-250μA	-60	--	--	V
IDSS	Zero Gate Voltage Drain Current	VDS=-30V,VGS=0V	--	--	-1	μA
IGSS	Gate-Body Leakage Current	VGS=±20V,VDS=0V	--	--	±100	nA
VGS(th)	Gate Threshold Voltage	VDS=VGS,ID=-250μA	-1.1	-1.7	-2.5	V
gFS	Forward Transconductance	VDS=5V,ID=-12A	--	7.0	--	S
RDS(on)	Drain-Source On-State Resistance	VGS=-10V, ID=-3A	--	53	67	mΩ
		VGS=-4.5V, ID=-2A	--	67	88	mΩ
<b>Dynamic Characteristics</b>						
Ciss	Input Capacitance	VDS=0V,VGS=0V, F=1MHZ	--	1200	--	pF
Coss	Output Capacitance		--	75	--	pF
Crss	Reverse Transfer Capacitance		--	58	--	pF
Rg	Gate resistance	VGS=0V, VDS=-0V,f=1.0MHz	--	7	--	Ω
<b>Switching Times</b>						
td(on)	Turn-on Delay Time	VGS=-10V,VDS=-30V, RL=2.5Ω,RGEN=3Ω	--	10	--	nS
tr	Turn-on Rise Time		--	6.0	--	nS
td(off)	Turn-Off Delay Time		--	40	--	nS
tf	Turn-Off Fall Time		--	13	--	nS
Qg	Total Gate Charge	VGS=-10V, VDS=-30V, ID=-3A	--	25	--	nC
Qgs	Gate-Source Charge		--	5.8	--	nC
Qgd	Gate-Drain Charge		--	3.1	--	nC
<b>Source-Drain Diode Characteristics</b>						
ISD	Source-Drain Current(Body Diode)		--	--	-5.7	A
VSD	Forward on Voltage	VGS=0V,IS=-2A	--	-0.8	-1.2	V
trr	Reverse Recovery Time	IF=-25A , dI/dt=100A/μs , TJ=25°C	--	50	--	ns
Qrr	Reverse Recovery Charge		--	105	--	nc

Notes 1.The maximum current rating is package limited.

Notes 2.Repetitive Rating: Pulse width limited by maximum junction temperature

Notes 3.EAS condition: TJ=25°C

### P-Channel Typical Characteristics

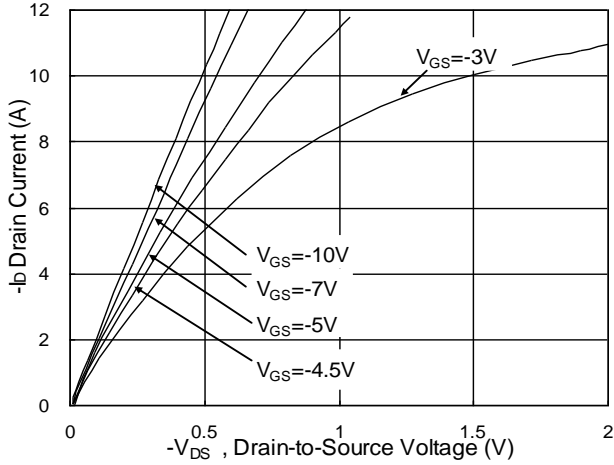


Fig.1 Typical Output Characteristics

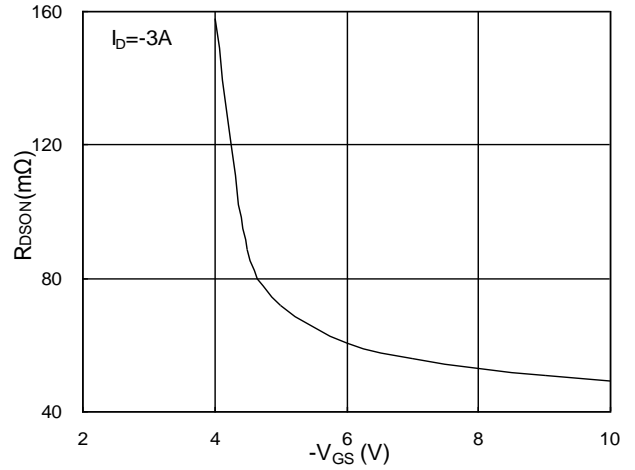


Fig.2 On-Resistance v.s Gate-Source

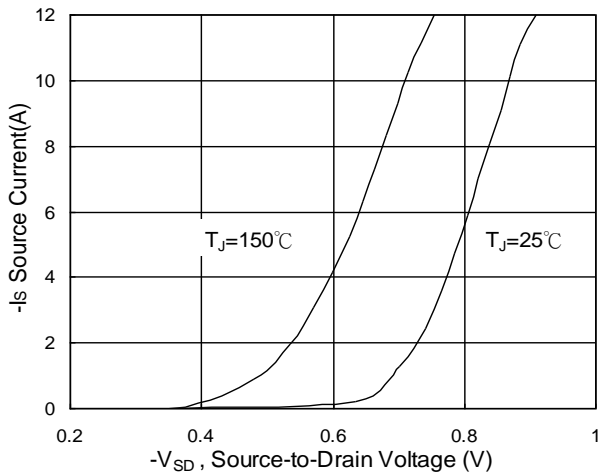


Fig.3 Forward Characteristics of Reverse

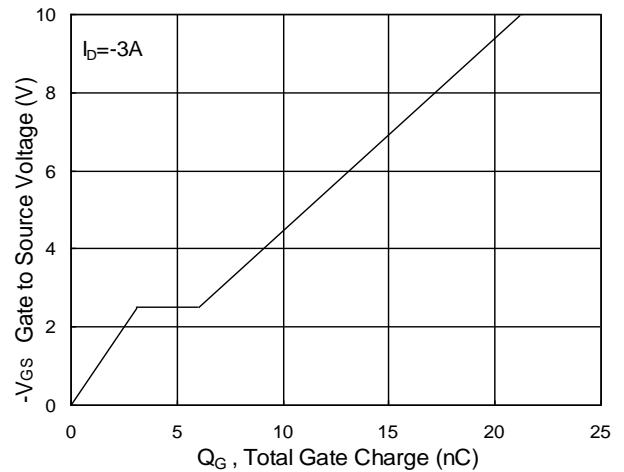


Fig.4 Gate-Charge Characteristics

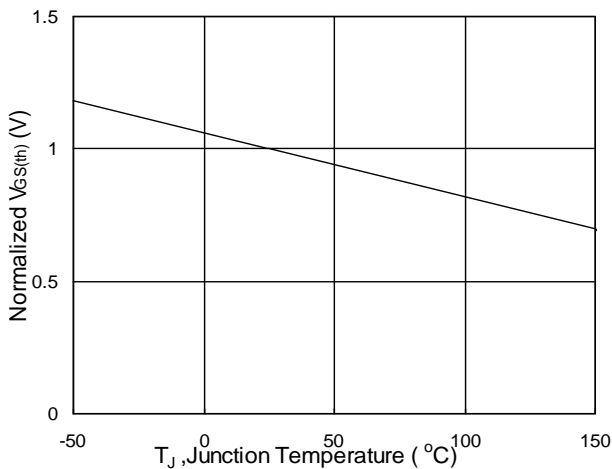


Fig.5 Normalized  $V_{GS(th)}$  v.s  $T_J$

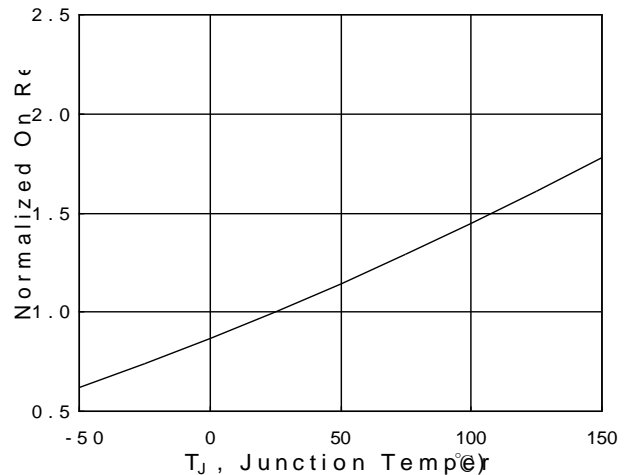
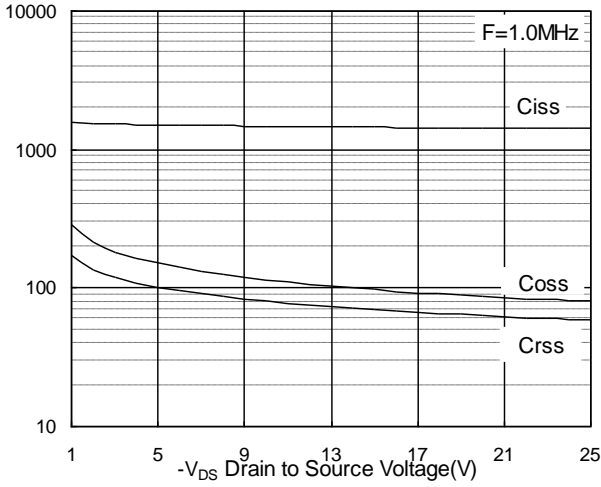
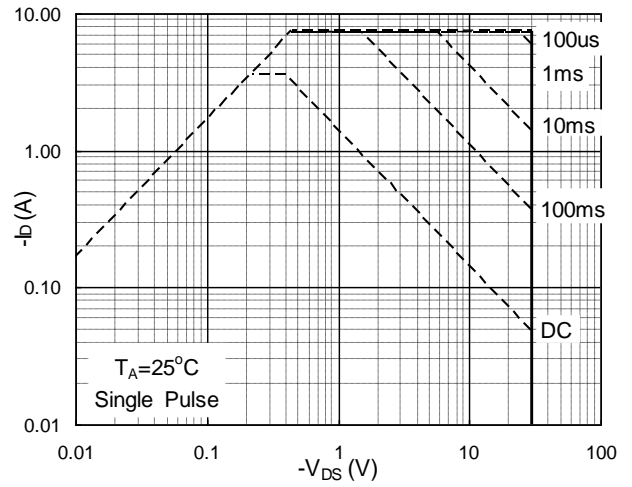


Fig.6 Normalized  $R_{DS(on)}$  v.s  $T_J$

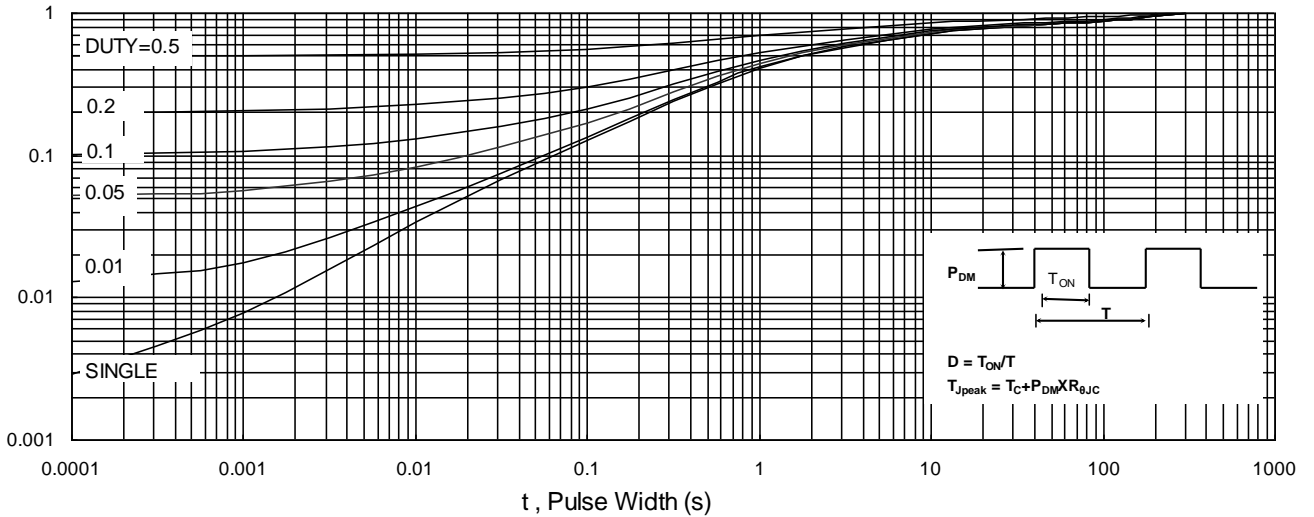
**P-Channel Typical Characteristics**



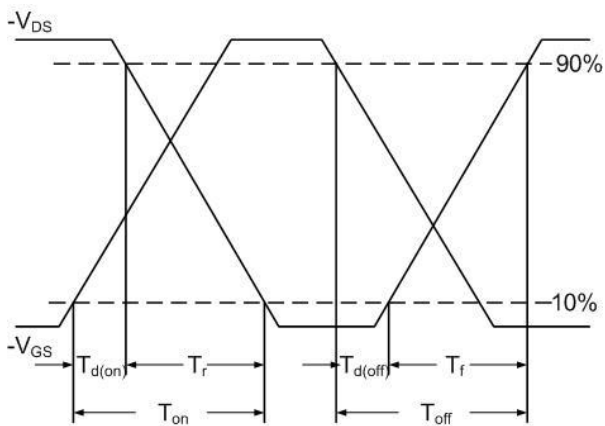
**Fig.7 Capacitance**



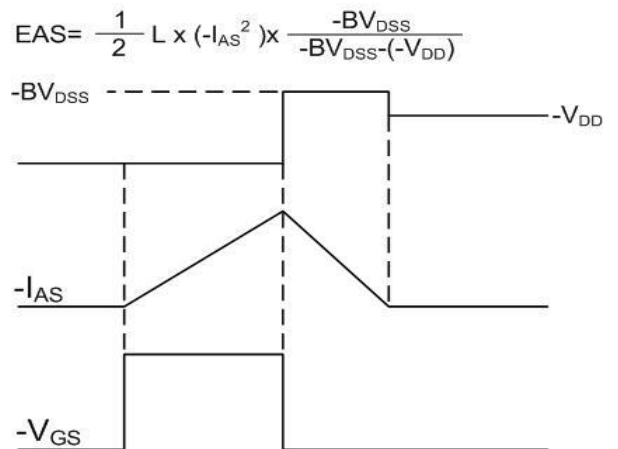
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**



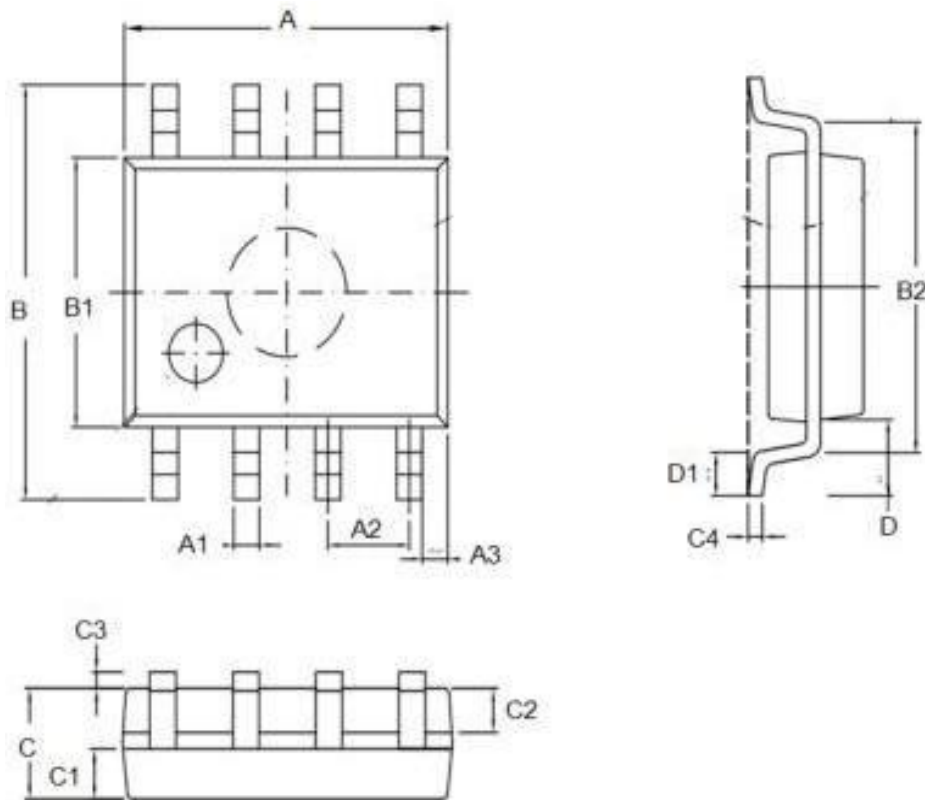
**Fig.10 Switching Time Waveform**



**Fig.11 Unclamped Inductive Waveform**

• **Dimensions(SOP8)**

SYMBOL	min	TYP	max	SYMBOL	min		max
A	4.80		5.00	C	1.30		1.50
A1	0.37		0.47	C1	0.55		0.75
A2		1.27		C2	0.55		0.65
A3		0.41		C3	0.05		0.20
B	5.80		6.20	C4	0.19	0.20	0.23
B1	3.80		4.00	D		1.05	
B2		5.00		D1	0.40		0.62




Disclaimer:

The information provided in this document is believed to be accurate and reliable. however, Shenzhen Core Control Electronics Technology Co., Ltd. does not assume any responsibility for the following consequences. Do not consider the use of such information or use beyond its scope.

The information mentioned in this document may be changed at any time without notice.

The products and information provided in this document do not infringe patents. Shenzhen Core Control Electronics Technology Co., Ltd. assumes no responsibility for any infringement of any other rights of third parties. The result of using such products and information.

This document is the third version issued on February 10, 2023. This document replaces and Replace all previously provided information.

 It is a registered trademark of Shenzhen Core Control Electronics Technology Co., Ltd.

Copyright © 2017 Shenzhen Core Control Electronics Technology Co., Ltd. all rights reserved.