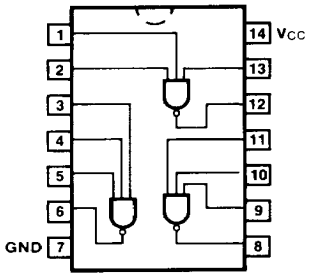
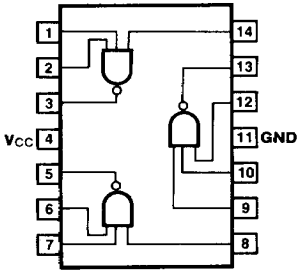
54/7410 011054
54H/74H10 011058
54S/74S10 011059
54LS/74LS10 011057

TRIPLE 3-INPUT NAND GATE

CONNECTION DIAGRAMS
PINOUT A



PINOUT B



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7410PC, 74H10PC 74S10PC, 74LS10PC		9A
Ceramic DIP (D)	A	7410DC, 74H10DC 74S10DC, 74LS10DC	5410DM, 54H10DM 54S10DM, 54LS10DM	6A
Flatpak (F)	A	74S10FC, 74LS10FC	54S10FM, 54LS10FM	3I
	B	7410FC, 74H10FC	5410FM, 54H10FM	

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74H (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	1.25/1.25	1.25/1.25	0.5/0.25
Outputs	20/10	12.5/12.5	25/12.5	10/5.0 (2.5)

DC AND AC CHARATERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74H Min	54/74H Max	54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS	
I_{CCH}	Power Supply		6.0		12.6		12		1.2	mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}	Current		16.5		30		27		3.3		V_{IN} = Open	
t_{PLH} t_{PHL}	Propagation Delay		22 15		10 10	2.0 2.0	4.5 5.0		15 15	ns	Fig. 3-1, 3-4	

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.