

GTLP1B153 1-Bit LVTTTL/GTLP Driver/Receiver Pair

General Description

The GTLP1B153 is a 1-bit bus buffer pair with separate bit paths, that provide LVTTTL-to-GTLP and GTLP-to-LVTTTL signal level translation. High speed backplane operation is a direct result of GTLP's reduced output swing (<1V), reduced input threshold levels and output edge rate control. The edge rate control minimizes bus settling time. GTLP is a Fairchild Semiconductor derivative of the Gunning Transistor logic (GTL) JEDEC standard JESD8-3.

Fairchild's GTLP has internal edge-rate control and is process, voltage and temperature compensated. GTLP's I/O structure is similar to GTL and BTL but offers different output levels and receiver threshold. Typical GTLP output voltage levels are: $V_{OL} = 0.5V$, $V_{OH} = 1.5V$, and $V_{REF} = 1V$.

Features

- Interface between LVTTTL and GTLP logic levels
- Designed with edge rate control circuitry to reduce output noise in the GTLP port
- V_{REF} pin provides external supply reference voltage for receiver threshold adjustability
- Special PVT compensation circuitry to provide consistent performance over variations of process, supply voltage and temperature
- TTL compatible driver and control inputs
- Designed using Fairchild advanced BiCMOS technology
- Bushold data inputs on A Port to eliminate the need for external pull-up resistors for unused inputs
- Power up/down and power off high impedance for live insertion
- Open drain on GTLP to support wired-or connection
- Flow through pinout optimizes PCB layout
- A Port source/sink $-24mA/+24mA$
- B Port sink $+50mA$

Ordering Code:

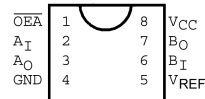
Order Number	Package Number	Package Description
GTLP1B153M	M08A	8-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow [TUBE]
GTLP1B153MX	M08A	8-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow [TAPE and REEL]
GTLP1B153K8X	MAB08A (Preliminary)	8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide [TAPE and REEL]

Pin Descriptions

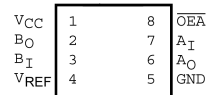
Pin Names	Description
\overline{OEA}	LVTTTL Bit Level Output Enable (Active LOW for Receive)
V_{CC} , GND, V_{REF}	Device Supplies
B_O , B_I	B Port GTLP Outputs/ Inputs
A_O / A_I	A Port LVTTTL Outputs/ Inputs

Connection Diagrams

US8



SOIC



Functional Description

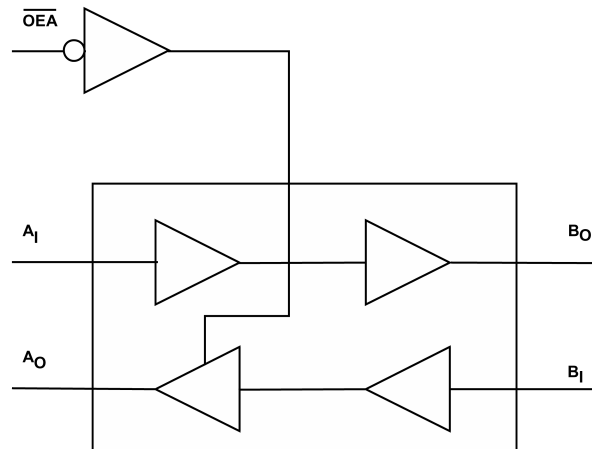
The GTLP1B153 is a 2-bit transceiver that supports GTLP and LVTTTL signal levels. Data polarity is non-inverting and the data flow in the B-to-A direction is controlled by the OEA pin.

Functional Table

Inputs		Outputs	Description
OEA	B _I	A _O	
L	L	L	A Output Data Bit Enabled
L	H	H	A Output Data Bit Enabled
H	X	Z	A Output Data Bit High Impedance
OEA	A _I	B _O	
X	L	L	B Output Data Bit Enabled
X	H	H	B Output Data Bit Enabled
		(Note 1)	

Note 1: Denotes that the bit would be in high impedance mode if there was no pull-up circuit due to open drain nature of the GTLP output.

Logic Diagram



Absolute Maximum Ratings ^(Note 2)		Recommended Operating Conditions	
Supply Voltage (V_{CC})	-0.5V to +4.6V	Supply Voltage V_{CC}	3.15V to 3.45V
DC Input Voltage (V_I)	-0.5V to +4.6V	Bus Termination Voltage (V_{TT})	
DC Output Voltage (V_O)		GTLP	1.47V to 1.53V
Outputs 3-STATE	-0.5V to +4.6V	V_{REF}	0.98V to 1.02V
Outputs Active (Note 3)	-0.5V to +4.6V	Input Voltage (V_I)	
DC Output Sink Current into		on A Port and Control Pins	0.0V to V_{CC}
A Port I_{OL}	48 mA	HIGH Level Output Current (I_{OH})	
DC Output Source Current from		A Port	-24 mA
A Port I_{OH}	-48 mA	LOW Level Output Current (I_{OL})	
DC Output Sink Current into		A Port	+24 mA
B Port in the LOW State, I_{OL}	100 mA	B Port	+50 mA
DC Input Diode Current (I_{IK})		Operating Temperature (T_A)	-40°C to +85°C
$V_I < 0V$	-50 mA	Note 2: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.	
DC Output Diode Current (I_{OK})		Note 3: I_O Absolute Maximum Rating must be observed.	
$V_O < 0V$	-50 mA		
ESD Rating	>2000V		
Storage Temperature (T_{STG})	-65°C to +150°C		

DC Electrical Characteristics

Over Recommended Operating Free-Air Temperature Range, $V_{REF} = 1.0V$ (unless otherwise noted).

Symbol	Test Conditions		Min	Typ (Note 4)	Max	Units
V_{IH}	B Port		$V_{REF} + 0.05$		V_{TT}	V
	Others		2.0			
V_{IL}	B Port		0.0		$V_{REF} - 0.05$	V
	Others				0.8	
V_{REF}	B Port		0.7V	1.0	1.3V	V
V_{TT}	B Port		$V_{REF} + 50\text{ mV}$	1.5	V_{CC}	V
V_{IK}		$V_{CC} = 3.15V$	$I_I = -18\text{ mA}$		-1.2	V
V_{OH}	A Port	$V_{CC} = \text{Min to Max (Note 5)}$	$I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC} - 0.2$		V
		$V_{CC} = 3.15V$	$I_{OH} = -8\text{ mA}$	2.4		
		$V_{CC} = 3.15V$	$I_{OH} = -24\text{ mA}$	2.2		
V_{OL}	A Port	$V_{CC} = \text{Min to Max (Note 5)}$	$I_{OL} = 100\text{ }\mu\text{A}$		0.2	V
		$V_{CC} = 3.15V$	$I_{OL} = 8\text{ mA}$		0.4	
		$V_{CC} = 3.15V$	$I_{OL} = 24\text{ mA}$		0.5	
	B Port	$V_{CC} = 3.15V$	$I_{OL} = 40\text{ mA}$		0.4	V
		$V_{CC} = 3.15V$	$I_{OL} = 50\text{ mA}$		0.55	
I_I	Control Pins	$V_{CC} = 3.45V$	$V_I = 3.45V$ $V_I = 0V$		5 -5	μA
	A Port	$V_{CC} = 3.45V$	$V_I = 3.45V$ $V_I = 0V$		10 -10	
	B Port	$V_{CC} = 3.45V$	$V_I = 3.45V$ $V_I = 0$		5 -5	
I_{OFF}	A Port, Control Pins	$V_{CC} = 0$	V_I or $V_O = 0$ to 3.45V		30	μA
	B Port	$V_{CC} = 0$	V_I or $V_O = 0$ to 3.45V		30	
$I_I(\text{HOLD})$	A Port	$V_{CC} = 3.15V$	$V_I = 0.8V$ $V_I = 2.0V$	75	-75	μA
I_{OZH}	A Port	$V_{CC} = 3.45V$	$V_O = 3.45V$		10	μA
	B Port		$V_O = 3.45V$		5	

DC Electrical Characteristics (Continued)

Symbol		Test Conditions	Min	Typ (Note 4)	Max	Units
I _{OZL}	A Port	V _{CC} = 3.45V	V _O = 0V		-10	μA
	B Port		V _O = 0V		-5	
I _{PU/PD}	All Ports	V _{CC} = 0 to 1.5V	V _I = 0 to 3.45V		30	μA
I _{CC}	A Port or B Port	V _{CC} = 3.45V I _O = 0 V _I = V _{CC} /V _{TT} or GND	Outputs HIGH		11	mA
			Outputs LOW		11	
			Outputs Disabled		11	
ΔI _{CC} (Note 6)	A Port and Control Pins	V _{CC} = 3.45V, A or Control Inputs at V _{CC} or GND	One Input at V _{CC} -0.6V		2	mA
C _i	Control Pins A and B Port		V _I = V _{CC} , V _{TT} or 0		3	pF
C _O	A Port		V _I = V _{CC} or 0		5	pF
	B Port		V _I = V _{TT} or 0		5	pF

Note 4: All typical values are at V_{CC} = 3.3V and T_A = 25°C.

Note 5: For conditions shown as Min, use the appropriate value specified under recommended operating conditions.

Note 6: This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

Note 7: GTLP V_{REF} and V_{TT} are specified to 2% tolerance since signal integrity and noise margin can be significantly degraded if these supplies are noisy. In addition, V_{TT} and R_{TERM} can be adjusted beyond the recommended operating to accommodate backplane impedances other than 50Ω, but must remain within the boundaries of the DC Absolute Maximum Ratings. Similarly, V_{REF} can be adjusted to optimize noise margin.

AC Electrical Characteristics

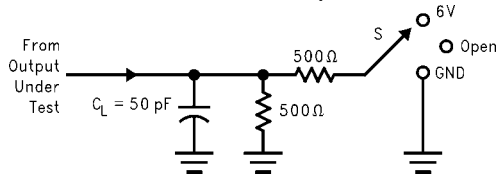
Over recommended range of supply voltage and operating free-air temperature, V_{REF} = 1.0V (unless otherwise noted).
 C_L = 30 pF for B Port and C_L = 50 pF for A Port.

Symbol	From (Input)	To (Output)	Min	Typ (Note 7)	Max	Unit
t _{PLH}	A	B	1.2	2.9	7.3	ns
t _{PHL}			0.8	2.0	4.5	
t _{PLH}	B	A	1.4	2.5	4.4	ns
t _{PHL}			1.6	2.7	5.0	
t _{RISE}	Transition Time, B Outputs (20% to 80%)			1.5		ns
t _{FALL}	Transition Time, B Outputs (80% to 20%)			1.8		ns
t _{RISE}	Transition Time, C Outputs (10% to 90%)			2.5		ns
t _{FALL}	Transition Time, C Outputs (90% to 10%)			2.2		ns
t _{PZH} , t _{PZL}	OEA	A	1.2	2.7	5.3	ns
t _{PHZ} , t _{PLZ}			1.4	2.8	4.9	

Note 7: All typical values are at V_{CC} = 3.3V, and T_A = 25°C.

Test Circuits and Timing Waveforms

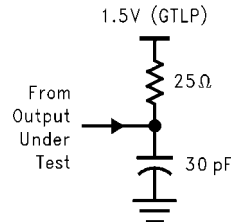
Test Circuit for A Outputs



Test	S
t_{PLH}/t_{PHL}	OPEN
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

Note: C_L includes probes and Jig capacitance.

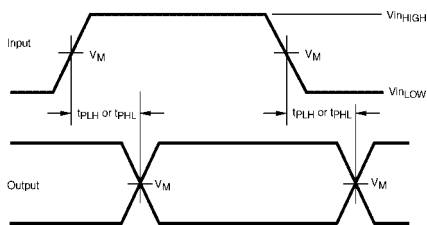
Test Circuit for B Outputs



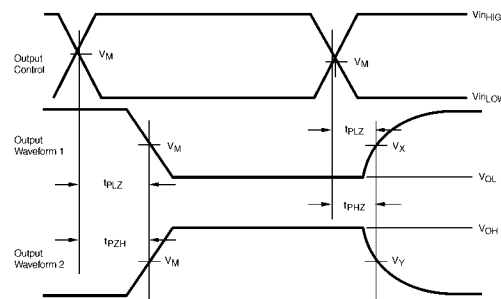
Note: C_L includes probes and Jig capacitance.

Note: For B Port, $C_L = 30$ pF is used for worst case.

Voltage Waveforms Propagation Delay



Voltage Waveform Enable and Disable Times



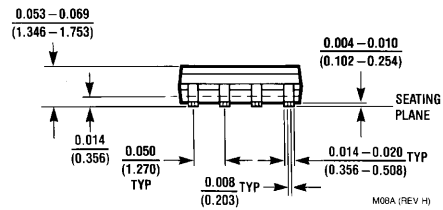
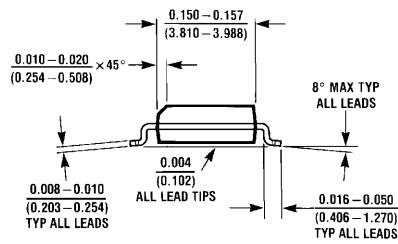
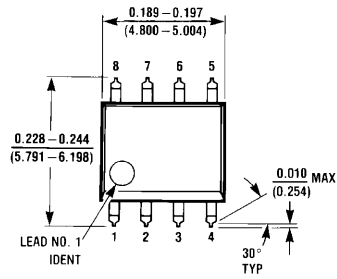
	A or LVTTTL Pins	B or GTLP Pins
V_{INHIGH}	V_{CC}	1.5
V_{INLOW}	0.0	0.0
V_M	$V_{CC}/2$	1.0
V_X	$V_{OL} + 0.3V$	N/A
V_Y	$V_{OH} - 0.3V$	N/A

Note: Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled by the output control.

Note: All input pulses have the following characteristics:

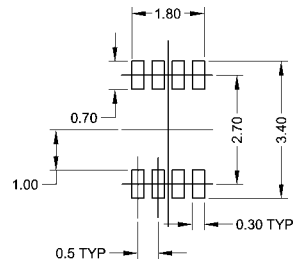
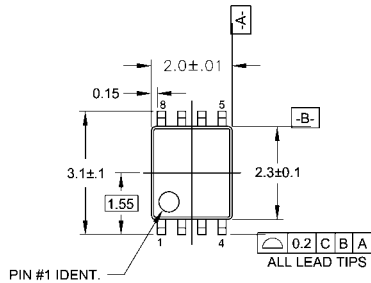
Frequency = 10MHz, $t_{RISE} = t_{FALL} = 2$ ns (10% to 90%), $Z_O = 50\Omega$. The outputs are measured one at a time with one transition per measurement.

Physical Dimensions inches (millimeters) unless otherwise noted

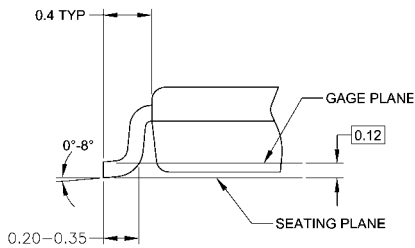
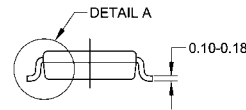
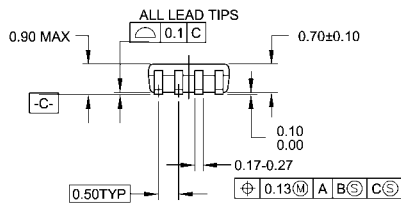


**8-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M08A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



DETAIL A

NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-187
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MAB08AREVC

**8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide
Package Number MAB08A
Preliminary**

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