MC14049UB

Hex Buffers

The MC14049UB hex inverter/buffer is constructed with MOS P−channel and N−channel enhancement mode devices in a single monolithic structure. This complementary MOS device finds primary use where low power dissipation and/or high noise immunity is desired. This device provides logic−level conversion using only one supply voltage, V_{DD}. The input−signal high level (V_{IH}) can exceed the V_{DD} supply voltage for logic−level conversions. Two TTL/DTL Loads can be driven when the device is used as CMOS−to−TTL/DTL converters (V_{DD} = 5.0 V, $V_{OL} \leq$ 0.4 V, $I_{OL} \geq$ 3.2 mA). Note that pins 13 and 16 are not connected internally on this device; consequently connections to these terminals will not affect circuit operation.

Features

- High Source and Sink Currents
- High−to−Low Level Converter
- Supply Voltage Range = 3.0 V to 18 V
- Meets JEDEC UB Specifications
- V_{IN} can exceed V_{DD}
- Improved ESD Protection on All Inputs
- Pb−Free Packages are Available*

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}	Input Voltage Range (DC or Transient)	−0.5 to +18.0	V
V_{out}	Output Voltage Range (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}	Input Current (DC or Transient) per Pin	±10	mA
I_{out}	Output Current (DC or Transient) per Pin	+45	mA
P_D	Power Dissipation, per Package (Note 14) Plastic SOIC	 825 740	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

14. Temperature Derating: All Packages: See Figure 4.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields referenced to the V_{SS} pin, only. Extra precautions must be taken to avoid applications of any voltage higher than the maximum rated voltages to this high−impedance circuit. For proper operation, the ranges $V_{SS} \leq V_{in} \leq 18$ V and $V_{SS} \leq V_{out} \leq V_{DD}$ are recommended.

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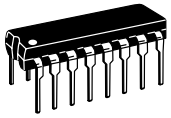
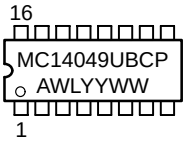
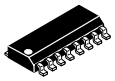
MARKING DIAGRAMS

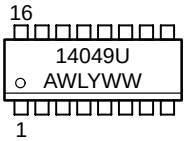


PDIP−16
P SUFFIX
CASE 648

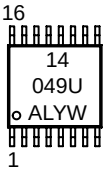


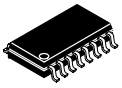


SOIC−16
D SUFFIX
CASE 751B

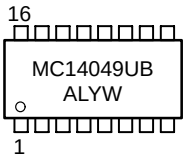


TSSOP−16
DT SUFFIX
CASE 948F





SOEIAJ−16
F SUFFIX
CASE 966



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 145 of this data sheet.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

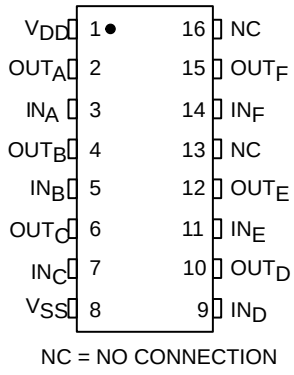


Figure 1. Pin Assignment

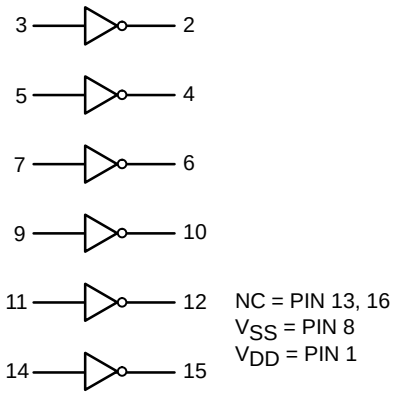


Figure 2. Logic Diagram MC14049UB

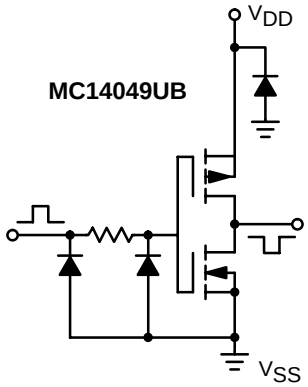


Figure 3. Circuit Schematic
(1/6 of circuit shown)

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	− 55°C Min	− 55°C Max	25°C Min	25°C Typ (Note 15)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage “0” Level V_{in} = V_{DD} or 0	V_{OL}	5.0	−	0.05	−	0	0.05	−	0.05	Vdc
		10	−	0.05	−	0	0.05	−	0.05	
		15	−	0.05	−	0	0.05	−	0.05	
“1” Level V_{in} = 0 or V_{DD}	V_{OH}	5.0	4.95	−	4.95	5.0	−	4.95	−	Vdc
		10	9.95	−	9.95	10	−	9.95	−	
		15	14.95	−	14.95	15	−	14.95	−	
Input Voltage “0” Level	V_{IL}									Vdc
(V_O = 4.5 Vdc)		5.0	−	1.0	−	2.25	1.0	−	1.0	
(V_O = 9.0 Vdc)		10	−	2.0	−	4.50	2.0	−	2.0	
(V_O = 13.5 Vdc)		15	−	2.5	−	6.75	2.5	−	2.5	
“1” Level	V_{IH}									Vdc
(V_O = 0.5 Vdc)		5.0	4.0	−	4.0	2.75	−	4.0	−	
(V_O = 1.0 Vdc)		10	8.0	−	8.0	5.50	−	8.0	−	
(V_O = 1.5 Vdc)		15	12.5	−	12.5	8.25	−	12.5	−	
Output Drive Current	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	– 1.6	−	– 1.25	– 2.5	−	– 1.0	−	
(V_{OH} = 9.5 Vdc)		10	– 1.6	−	– 1.3	– 2.6	−	– 1.0	−	
(V_{OH} = 13.5 Vdc)		15	– 4.7	−	– 3.75	– 10	−	– 3.0	−	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	3.75	−	3.2	6.0	−	2.6	−	mAdc
(V_{OL} = 0.5 Vdc)		10	10	−	8.0	16	−	6.6	−	
(V_{OL} = 1.5 Vdc)		15	30	−	24	40	−	19	−	
Input Current	I_{in}	15	−	± 0.1	−	±0.000 01	± 0.1	−	± 1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	−	−	−	−	10	20	−	−	pF
Quiescent Current (Per Package)	I_{DD}	5.0	−	1.0	−	0.002	1.0	−	30	μAdc
		10	−	2.0	−	0.004	2.0	−	60	
		15	−	4.0	−	0.006	4.0	−	120	
Total Supply Current (Note 16 and 17) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.8 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (3.5 μA/kHz) f + I_{DD}							
		15	I_T = (5.3 μA/kHz) f + I_{DD}							

15. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.
16. The formulas given are for the typical characteristics only at 25°C.
17. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.

SWITCHING CHARACTERISTICS (Note 18) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ (Note 19)	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (0.8 ns/pF) C_L + 60 ns		5.0	–	100	160	
t_{TLH} = (0.3 ns/pF) C_L + 35 ns		10	–	50	100	
t_{TLH} = (0.27 ns/pF) C_L + 26.5 ns		15	–	40	60	
Output Fall Time	t_{THL}					ns
t_{THL} = (0.3 ns/pF) C_L + 25 ns		5.0	–	40	60	
t_{THL} = (0.12 ns/pF) C_L + 14 ns		10	–	20	40	
t_{THL} = (0.1 ns/pF) C_L + 10 ns		15	–	15	30	
Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (0.38 ns/pF) C_L + 61 ns		5.0	–	80	120	
t_{PLH} = (0.20 ns/pF) C_L + 30 ns		10	–	40	65	
t_{PLH} = (0.11 ns/pF) C_L + 24.5 ns		15	–	30	50	
Propagation Delay Time	t_{PHL}					ns
t_{PHL} = (0.38 ns/pF) C_L + 11 ns		5.0	–	30	60	
t_{PHL} = (0.12 ns/PF) C_L + 9 ns		10	–	15	30	
t_{PHL} = (0.11 ns/pF) C_L + 4.5 ns		15	–	10	20	

18. The formulas given are for the typical characteristics only at 25°C.
19. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

ORDERING INFORMATION

Device	Package	Shipping†
MC14049UBCP	PDIP−16	2,000 Units / Box
MC14049UBCPG	PDIP−16 (Pb−Free)	2,000 Units / Box
MC14049UBD	SOIC−16	2,400 Units / Box
MC14049UBDG	SOIC−16 (Pb−Free)	2,400 Units / Box
MC14049UBDR2	SOIC−16	2,500 / Tape & Reel
MC14049UBDR2G	SOIC−16 (Pb−Free)	2,500 / Tape & Reel
MC14049UBDT	TSSOP−16	96 Units / Rail
MC14049UBDTEL	TSSOP−16*	96 Units / Rail
MC14049UBDTR2	TSSOP−16*	2,500 / Tape & Reel
MC14049UBF	SOEIAJ−16	See Note 20
MC14049UBFEL	SOEIAJ−16	See Note 20

20. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*This package is inherently Pb−Free.

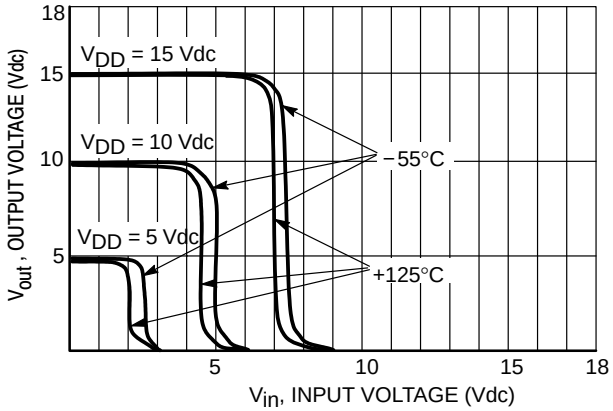
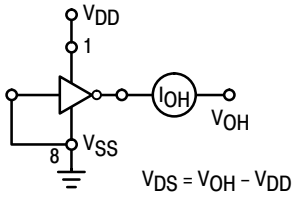
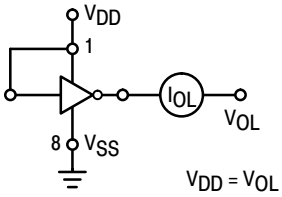


Figure 4. Typical Voltage Transfer Characteristics versus Temperature





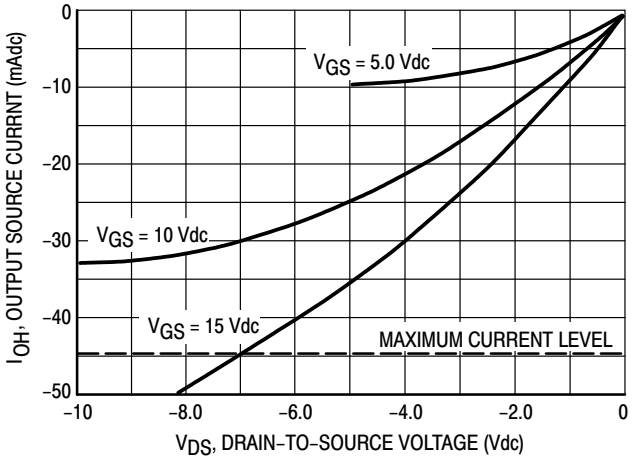


Figure 5. Typical Output Source Characteristics

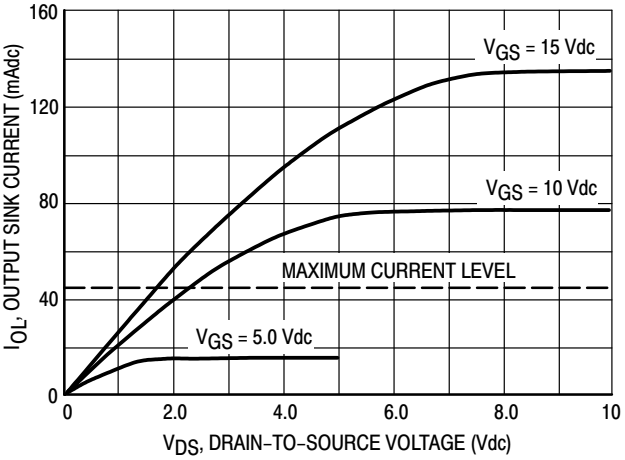


Figure 6. Typical Output Sink Characteristics

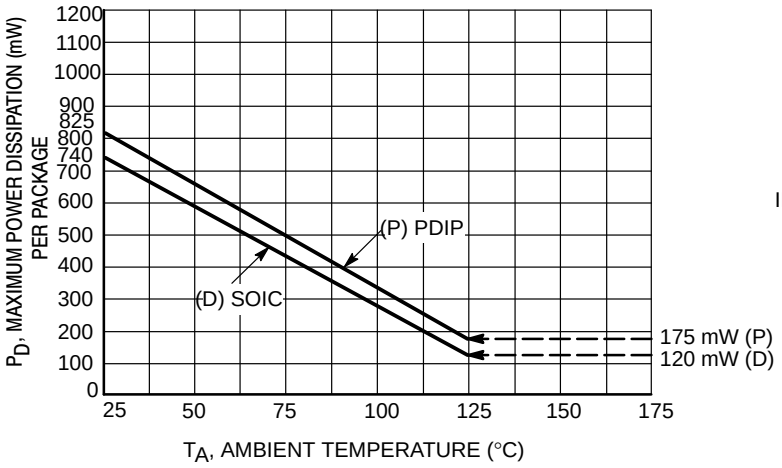


Figure 7. Ambient Temperature Power Derating

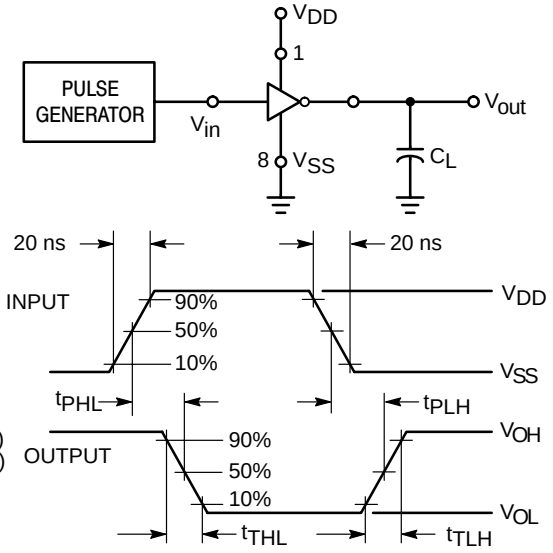


Figure 8. Switching Time Test Circuit and Waveforms