

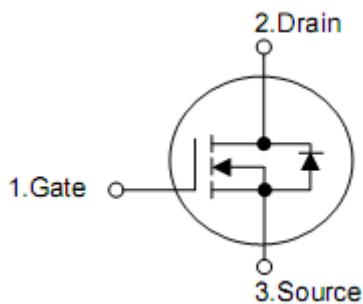
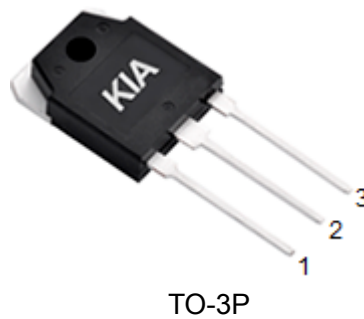
1. Features

- Proprietary New Planar Technology
- $R_{DS(ON)}=70m\Omega(\text{typ.})@V_{GS}=10V$
- Low Gate Charge Minimize Switching Loss
- Fast Recovery Body Diode

2. Applications

- DC-DC Converters
- DC-AC Inverters for UPS
- SMPS and Motor controls

3. Pin configuration



Pin	Function
1	Gate
2	Drain
3	Source

4. Ordering Information

Part Number	Package	Brand
KNH3730A	TO-3P	KIA

5. Absolute maximum ratings

(T_c= 25 °C , unless otherwise specified)

Parameter	Symbol	Ratings	Unit	
Drain-to-Source Voltage ¹⁾	V _{DSS}	300	V	
Gate-to-Source Voltage	V _{GSS}	±20	V	
Continuous Drain Current	T _c =25 °C	I _D	50	A
	T _c =100 °C	I _D	31	A
Pulsed Drain Current at V _{GS} =10V ²⁾	I _{DM}	200	A	
Single Pulse Avalanche Energy	EAS	3044	mJ	
Peak Diode Recovery dv/dt ³⁾	dv/dt	5.0	V/ns	
Power Dissipation	P _D	305	W	
Derating Factor above 25°C	P _D	2.5	W/°C	
Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10 seconds, Package Body for 10 seconds	T _L T _{PAK}	300 260	°C	
Operating and Storage Temperature Range	T _J &T _{STG}	-55 to 150	°C	

Caution: Stresses greater than those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device.

6. Thermal characteristics

Parameter	Symbol	Ratings	Unit
Thermal Resistance, Junction-to-Case	R _{θJC}	0.41	°C/W
Thermal Resistance, Junction-to-Ambient	R _{θJA}	50	°C/W

7. Electrical characteristics

(T_J=25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-to-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250uA	300	-	-	V
Drain-to-Source Leakage Current	I _{DSS}	V _{DS} =300V, V _{GS} =0V	-	-	1	uA
		V _{DS} =240V, T _J =125°C	-	-	100	uA
Gate-to-Source Leakage Current	I _{GSS}	V _{GS} =±30V, V _{DS} =0V	-	-	±100	nA
Drain-to-Source ON Resistance ⁴⁾	R _{DS(ON)}	V _{GS} =10V, I _D =25A	-	70	88	mΩ
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250uA	2.0	-	4.0	V
Forward Transconductance ⁴⁾	g _{fs}	V _{DS} =15V, I _D =25A	-	18	-	S
Input Capacitance	C _{iss}	V _{GS} =0V, V _{DS} =25V, f=1.0MHZ	-	5108	-	pF
Reverse Transfer Capacitance	C _{rss}		-	275	-	
Output Capacitance	C _{oss}		-	500	-	
Total Gate Charge	Q _g	V _{DD} =150V, I _D =25A, V _{GS} =0~10V	-	220	-	nC
Gate-to-Source Charge	Q _{gs}		-	16	-	
Gate-to-Drain (Miller) Charge	Q _{gd}		-	128	-	
Turn-on Delay Time	t _{d(ON)}	V _{DD} =150V, I _D =25A, R _G =1.2Ω, V _{GS} =10V	-	25	-	nS
Rise Time	t _{rise}		-	50	-	
Turn-Off Delay Time	t _{d(OFF)}		-	100	-	
Fall Time	t _{fall}		-	35	-	
Continuous Source Current ⁴⁾	I _{SD}	Integral PN-diode in MOSFET	-	-	50	A
Pulsed Source Current ⁴⁾	I _{SM}		-	-	200	A
Forward Voltage	V _{SD}	I _S =25A, V _{GS} =0V	-	-	1.5	V
Reverse recovery time	t _{rr}	V _{GS} =0V, I _F =25A, diF/dt=100A/μs	-	516	-	ns
Reverse recovery charge	Q _{rr}		-	4.16	-	uC

Note:

1) T_J=+25°C to +150°C

2) Repetitive rating; pulse width limited by maximum junction temperature.

3) I_{SD}=20A, di/dt<100 A/μs, V_{DD}<BV_{DSS}, T_J=+150°C.

4) Pulse width≤380μs; duty cycle≤2%.

8. Test circuits and waveforms

Figure 1a Safe Operating Area

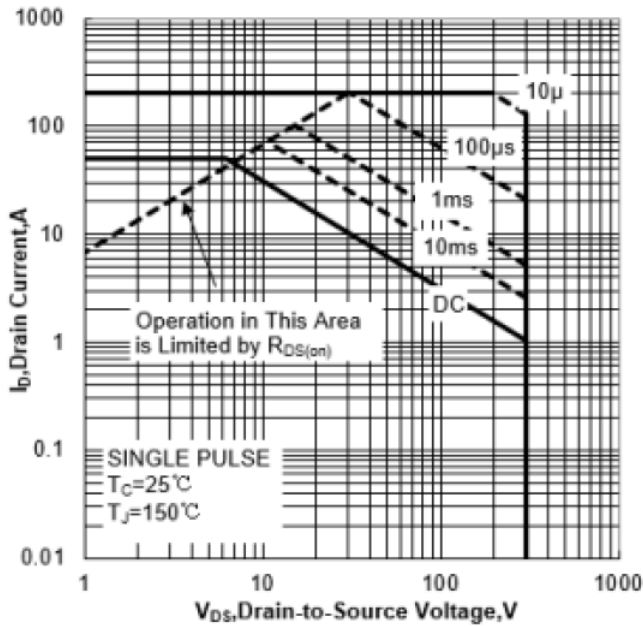


Figure 2 Power Dissipation

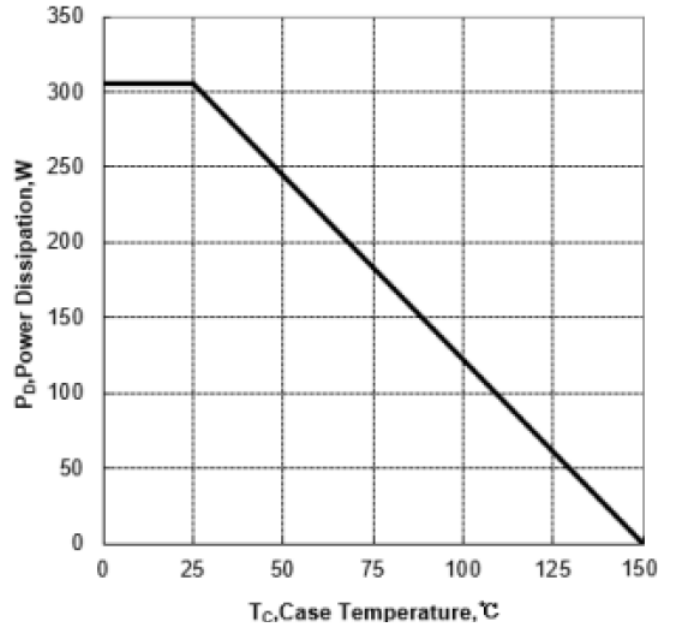


Figure 3 Max Thermal Impedance

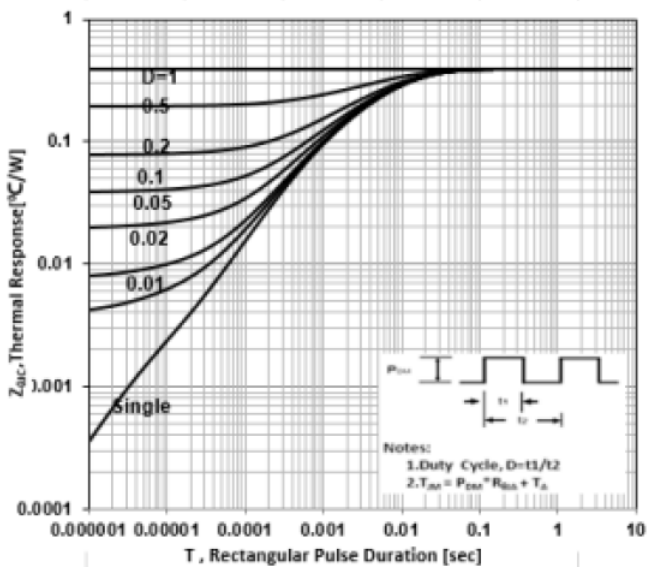


Figure 4 Typical Output Characteristics

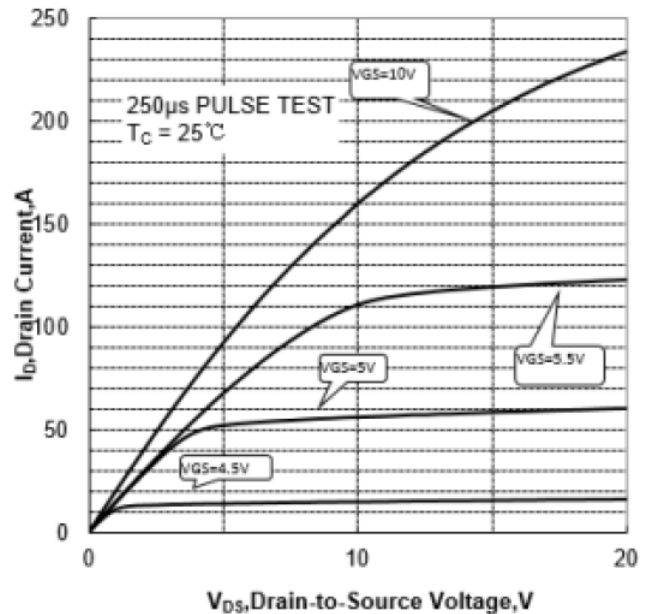


Figure 5 Typical Transfer Characteristics

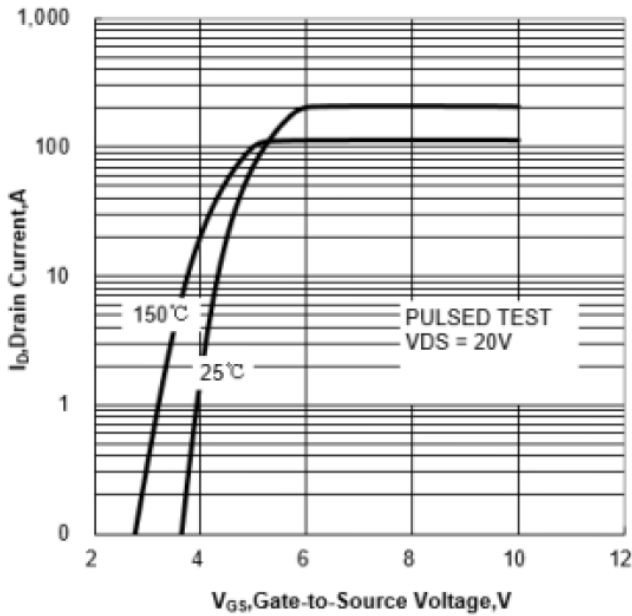


Figure 6 Typical Drain to Source ON Resistance vs Drain Current

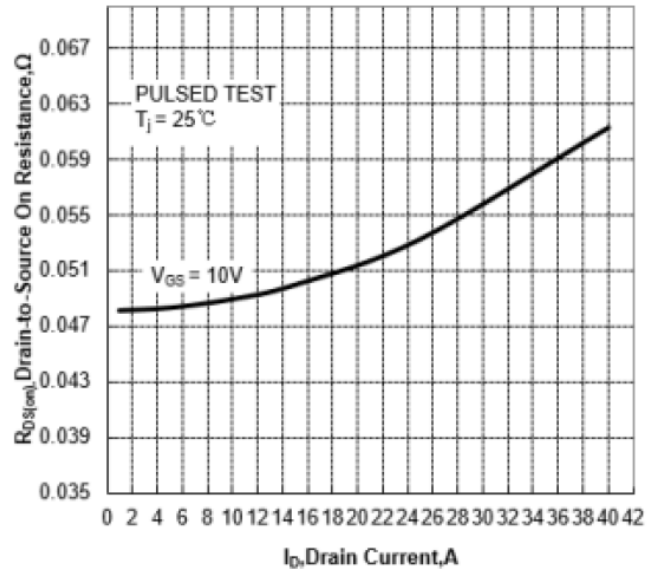


Figure 7 Typical Drain to Source on Resistance vs Junction Temperature

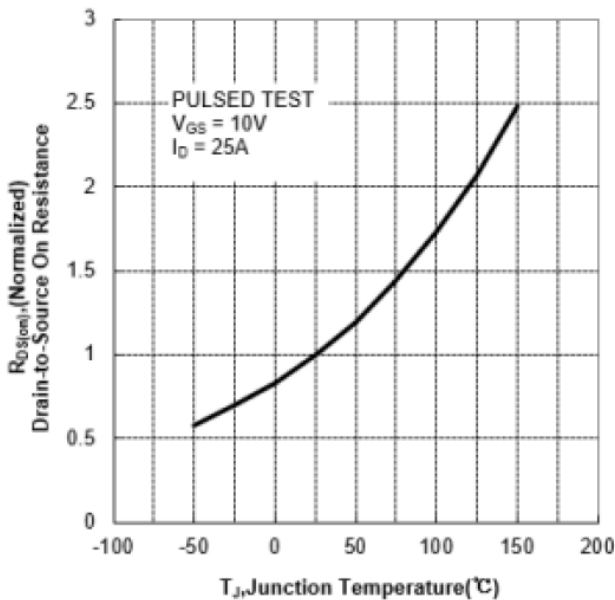


Figure 8 Typical Theshold Voltage vs Junction Temperature

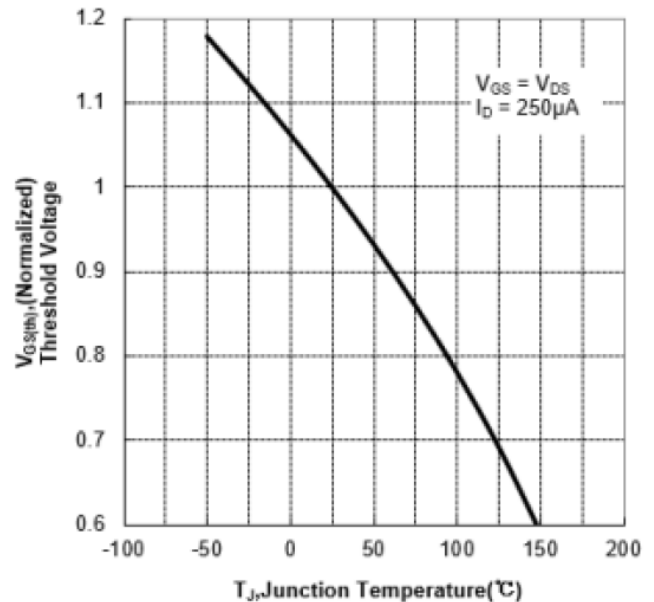


Figure 9 Typical Breakdown Voltage vs Junction Temperature

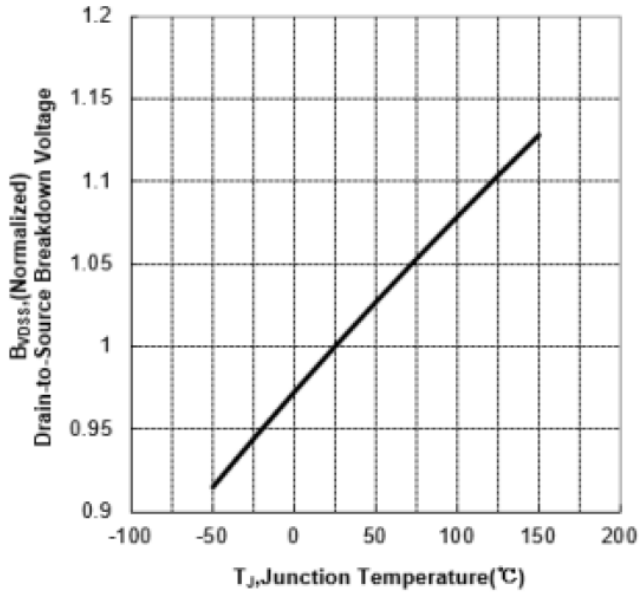


Figure 10 Typical Capacitance vs Drain to Source Voltage

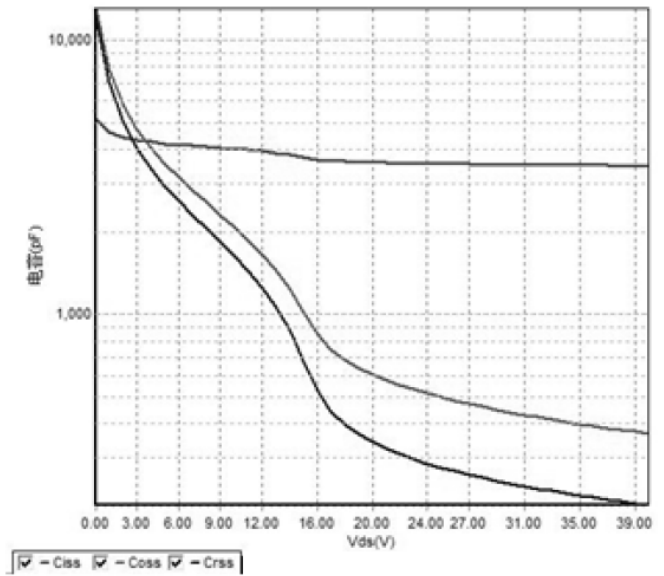
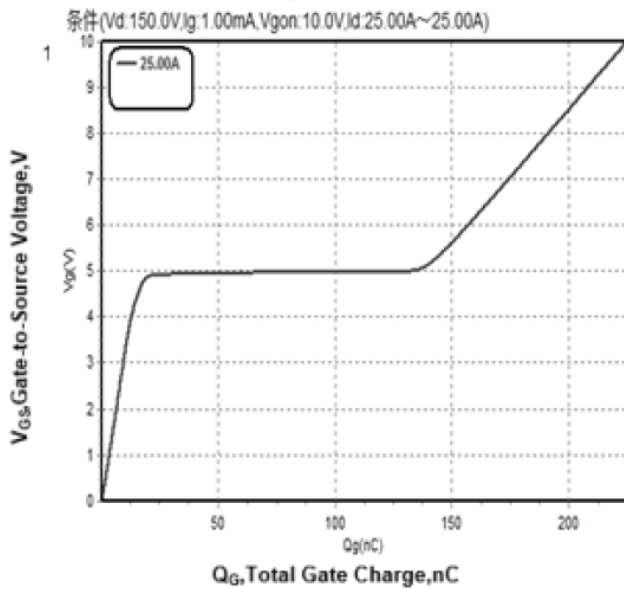


Figure 11 Typical Gate Charge vs Gate to Source Voltage



9. Test Circuits and Waveforms

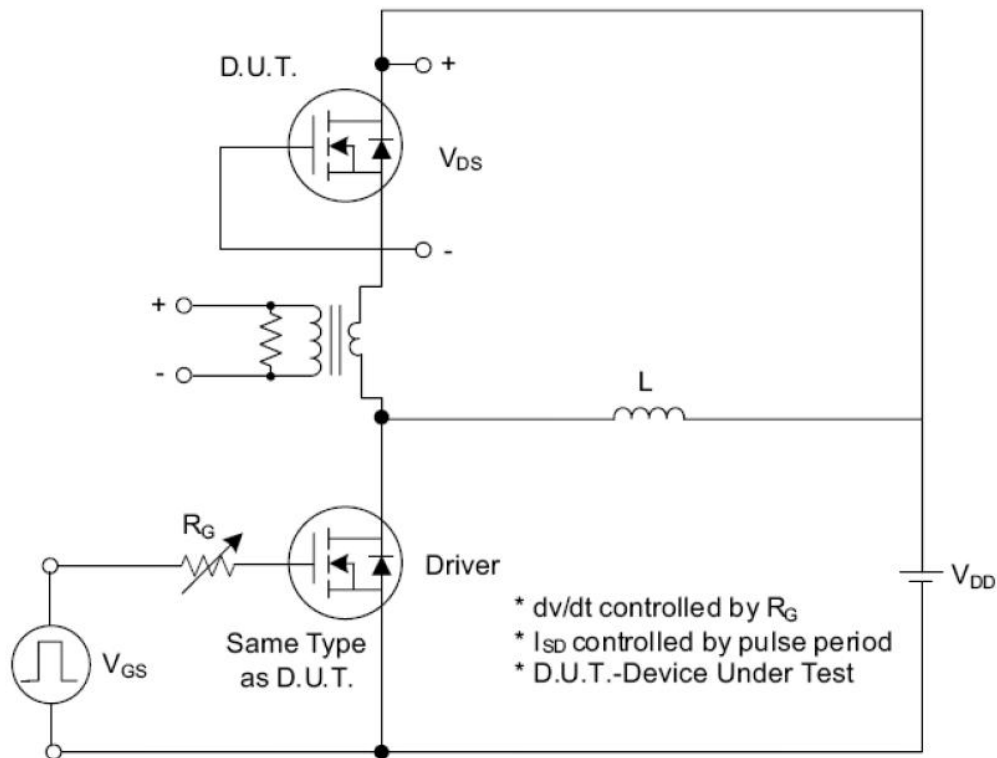


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

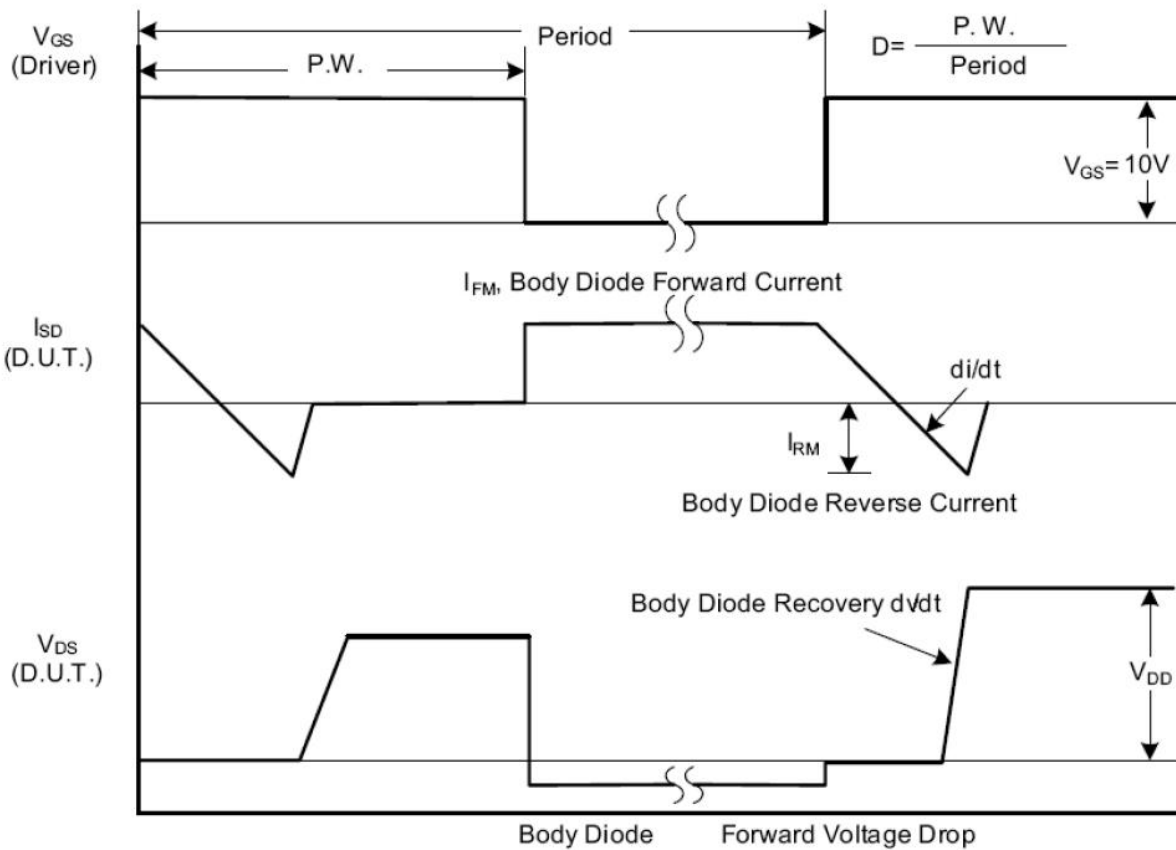


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

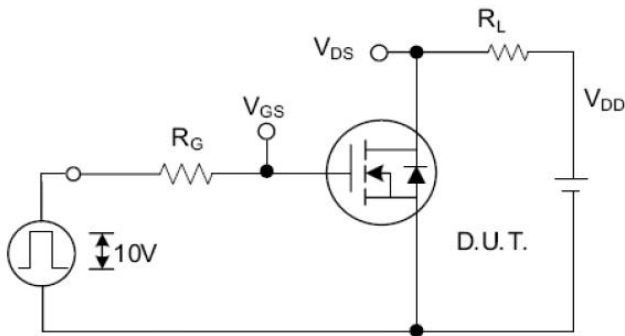


Fig. 2.1 Switching Test Circuit

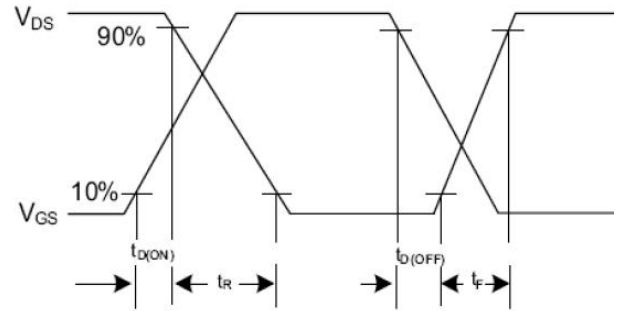


Fig. 2.2 Switching Waveforms

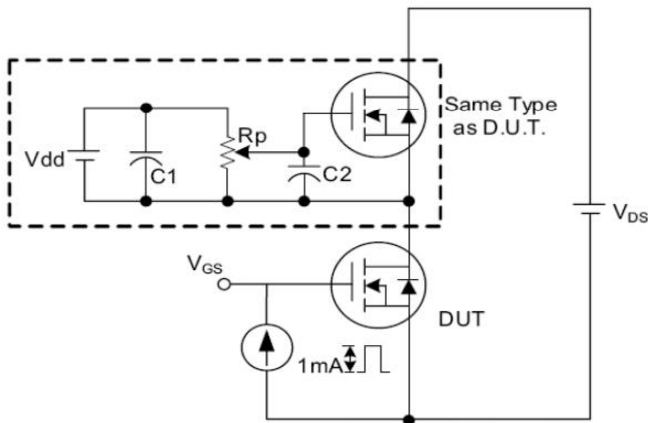


Fig. 3.1 Gate Charge Test Circuit

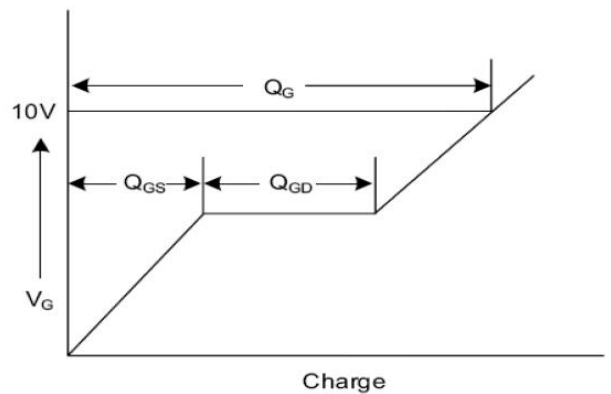


Fig. 3.2 Gate Charge Waveform

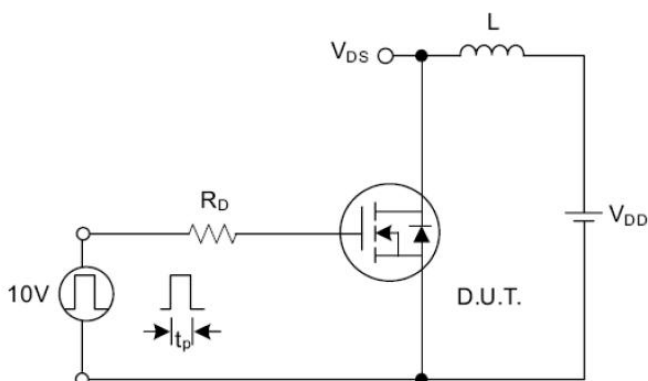


Fig. 4.1 Unclamped Inductive Switching Test Circuit

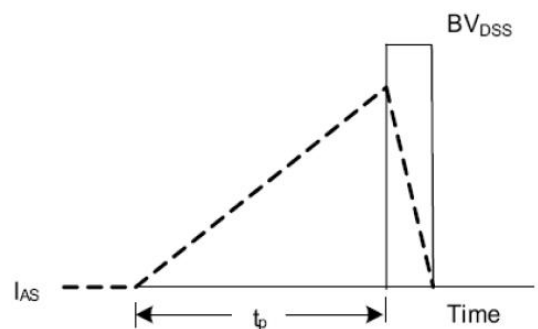


Fig. 4.2 Unclamped Inductive Switching Waveforms