

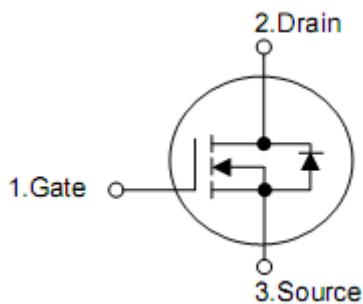
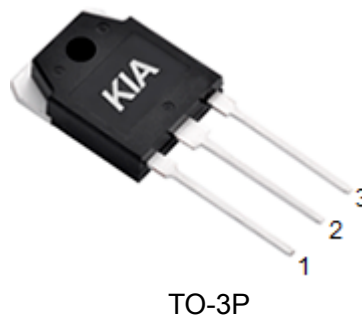
1. Features

- Proprietary New Planar Technology
- $R_{DS(ON)}=45m\Omega(\text{typ.})@V_{GS}=10V$
- Low Gate Charge Minimize Switching Loss
- Rugged Poly silicon Gate Structure

2. Applications

- BLDC Motor Driver
- Electric Welder
- High Efficiency SMPS

3. Pin configuration



Pin	Function
1	Gate
2	Drain
3	Source

4. Ordering Information

Part Number	Package	Brand
KNH3530A	TO-3P	KIA

5. Absolute maximum ratings

(T_c= 25 °C , unless otherwise specified)

Parameter		Symbol	Ratings	Unit
Drain-to-Source Voltage ¹⁾		V _{DSS}	300	V
Gate-to-Source Voltage		V _{GSS}	±30	V
Continuous Drain Current	T _c =25 °C	I _D	70	A
	T _c =100 °C	I _D	42	A
Pulsed Drain Current at V _{GS} =10V ^{2),4)}		I _{DM}	276	A
Single Pulse Avalanche Energy		EAS	4494	mJ
Peak Diode Recovery dv/dt ³⁾		dv/dt	5.0	V/ns
Power Dissipation		P _D	520	W
Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10 seconds, Package Body for 10 seconds		T _L T _{PAK}	300 260	°C
Operating and Storage Temperature Range		T _J &T _{STG}	-55 to 150	°C

Caution: Stresses greater than those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device.

6. Thermal characteristics

Parameter	Symbol	Ratings	Unit
Thermal Resistance, Junction-to-Case	R _{θJC}	0.24	°C/W
Thermal Resistance, Junction-to-Ambient	R _{θJA}	50	°C/W

7. Electrical characteristics

 (T_J=25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-to-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250uA	300	-	-	V
Drain-to-Source Leakage Current	I _{DSS}	V _{DS} =300V, V _{GS} =0V	-	-	1	uA
		V _{DS} =240V, T _J =125°C	-	-	125	uA
Gate-to-Source Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Drain-to-Source ON Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =35A	-	45	52	mΩ
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250uA	2.0	-	4.0	V
Forward Transconductance	g _{fs}	V _{DS} =15V, I _D =30A	-	55	-	S
Input Capacitance	C _{iss}	V _{GS} =0V, V _{DS} =25V, f=1.0MHz	-	5975	-	pF
Reverse Transfer Capacitance	C _{rss}		-	455	-	
Output Capacitance	C _{oss}		-	815	-	
Total Gate Charge	Q _g	V _{DD} =150V, I _D =70A, V _{GS} =0~10V	-	380	-	nC
Gate-to-Source Charge	Q _{gs}		-	28	-	
Gate-to-Drain (Miller) Charge	Q _{gd}		-	205	-	
Turn-on Delay Time	t _{d(ON)}	V _{DD} =150V, I _D =35A, R _G =10Ω, V _{GS} =10V	-	40	-	nS
Rise Time	t _{rise}		-	200	-	
Turn-Off Delay Time	t _{d(OFF)}		-	515	-	
Fall Time	t _{fall}		-	180	-	
Continuous Source Current ^{2),5)}	I _{SD}	Integral PN-diode in MOSFET	-	-	70	A
Pulsed Source Current ^{2),5)}	I _{SM}		-	-	276	A
Forward Voltage	V _{SD}	I _S =69A, V _{GS} =0V	-	-	1.5	V
Reverse recovery time	t _{rr}	V _{GS} =0V, I _F =70A, diF/dt=100A/μs	-	611	-	ns
Reverse recovery charge	Q _{rr}		-	5904	-	nC

Note:

- 1) T_J=+25°C to +150°C.
- 2) Silicon limited current only.
- 3) Package limited current.
- 4) Repetitive rating; pulse width limited by maximum junction temperature.
- 5) Pulse width ≤ 380us; duty cycle ≤ 2%.

8. Test circuits and waveforms

Figure 1. Maximum Transient Thermal Impedance

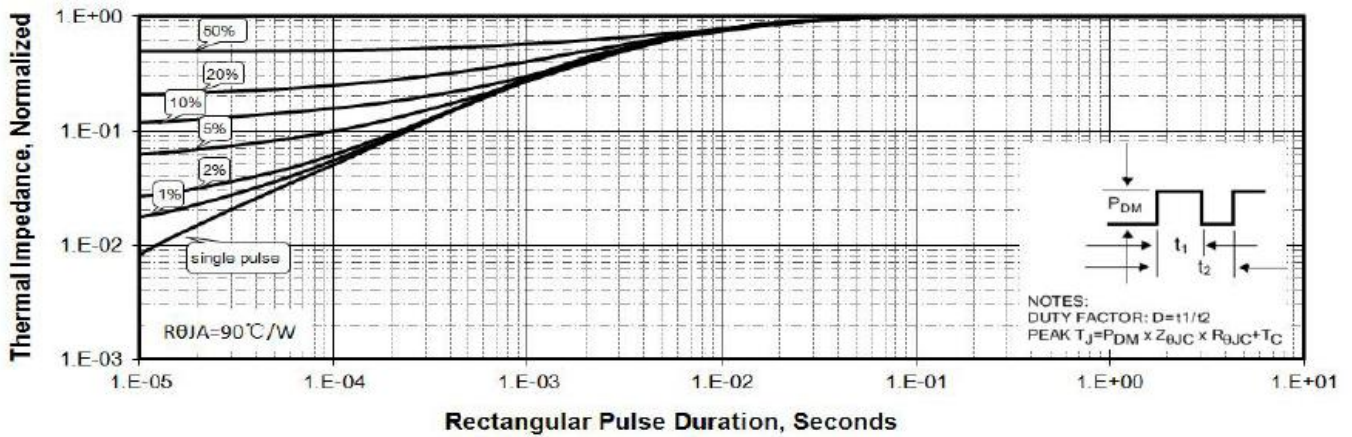


Figure 2 . Max. Power Dissipation vs Case Temperature

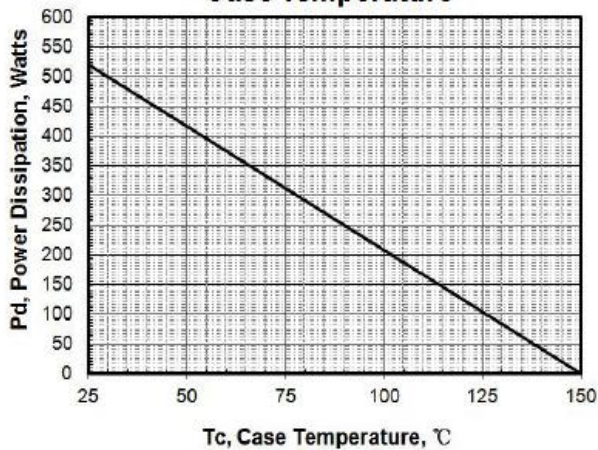


Figure 3 .Maximum Continuous Drain Current vs Tc

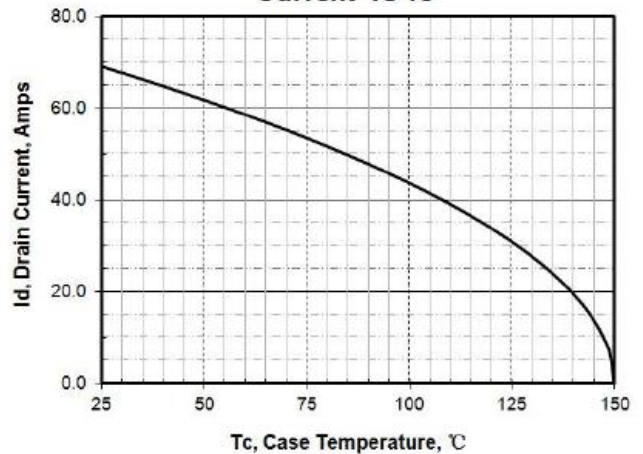


Figure 4. Output Characteristics

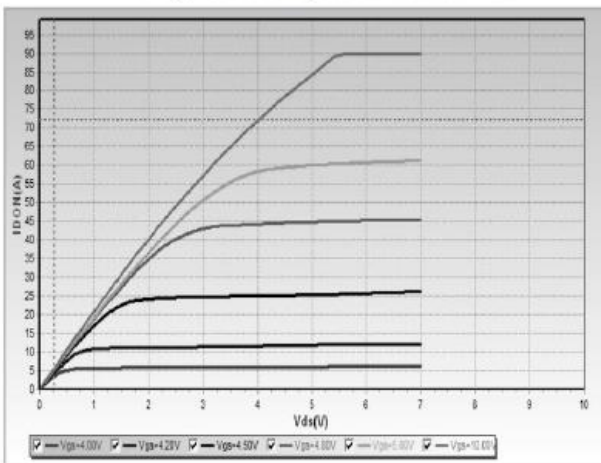


Figure 5. Rdson vs Gate Voltage

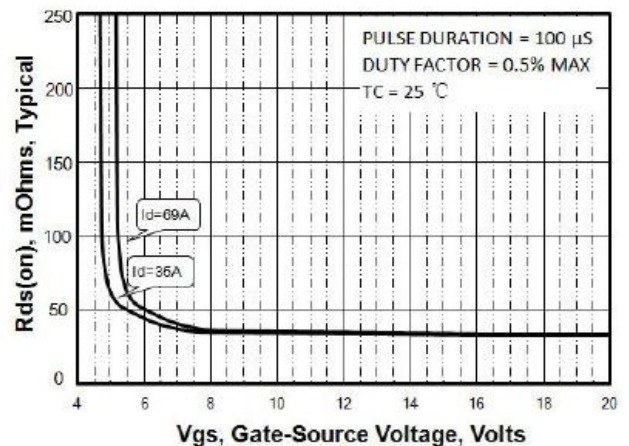


Figure 6. Peak Current Capability

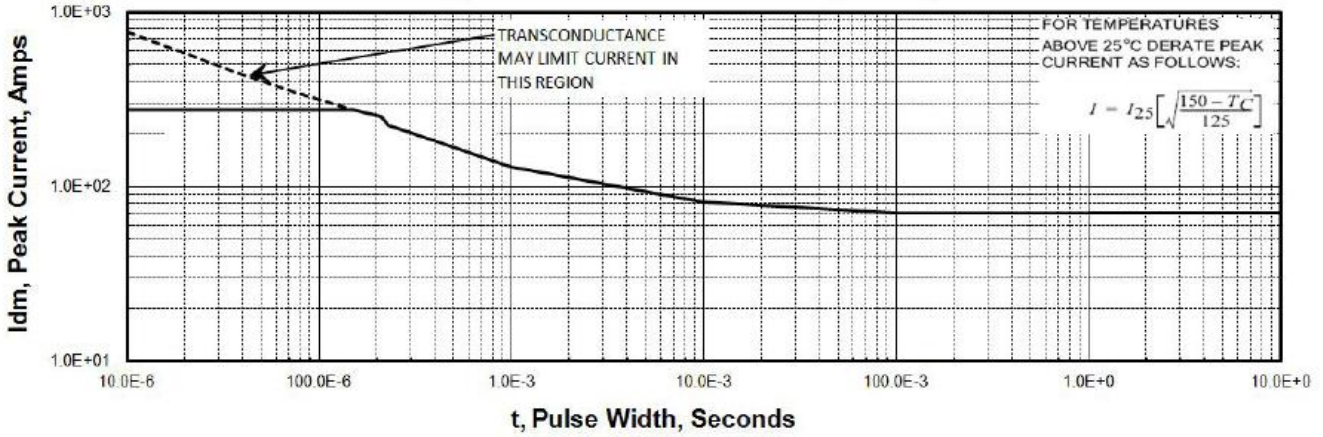


Figure 7. Transfer Characteristics

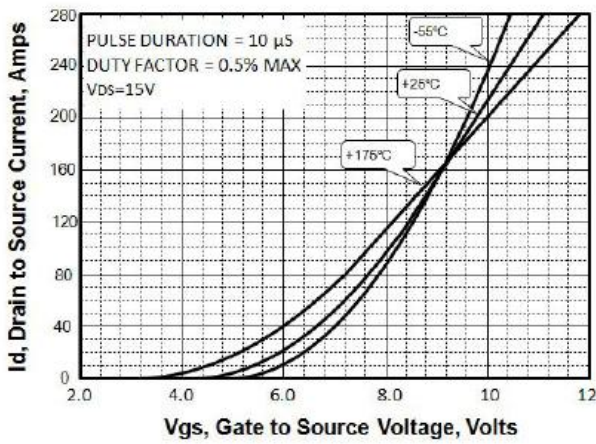


Figure 8. Unclamped Inductive Switching Capability

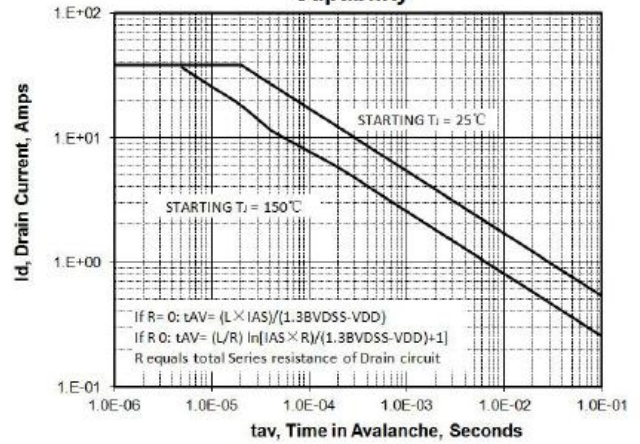


Figure 9. Drain to Source ON Resistance vs Drain Current

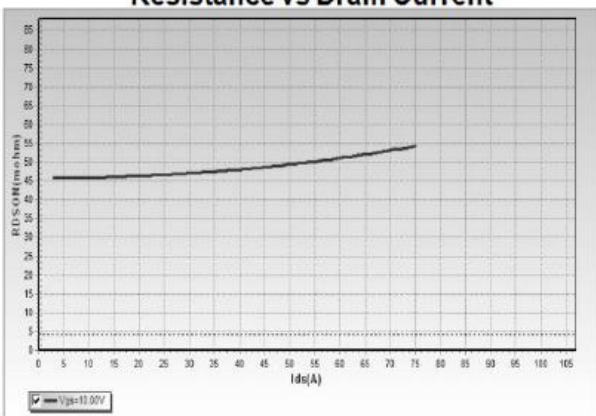


Figure 10. Rds(on) vs Junction Temperature

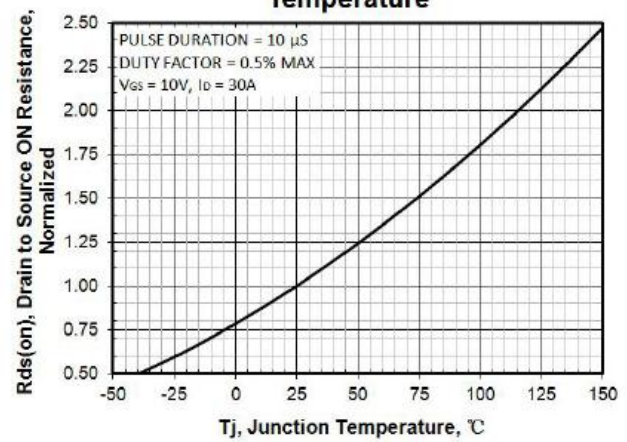


Figure 11. Breakdown Voltage vs Temperature

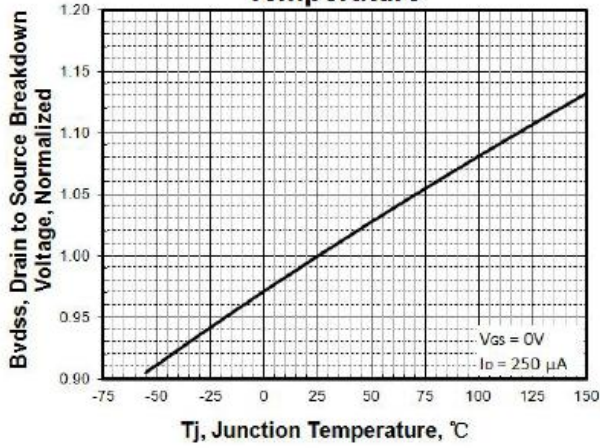


Figure 12. Threshold Voltage vs Temperature

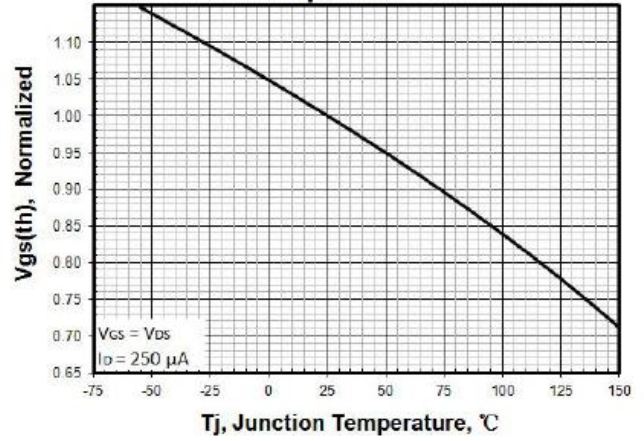


Figure 13. Maximum Safe Operating Area

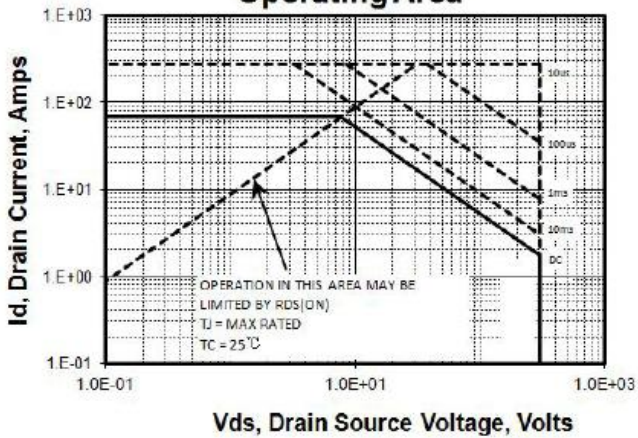


Figure 14. Capacitance vs Vds

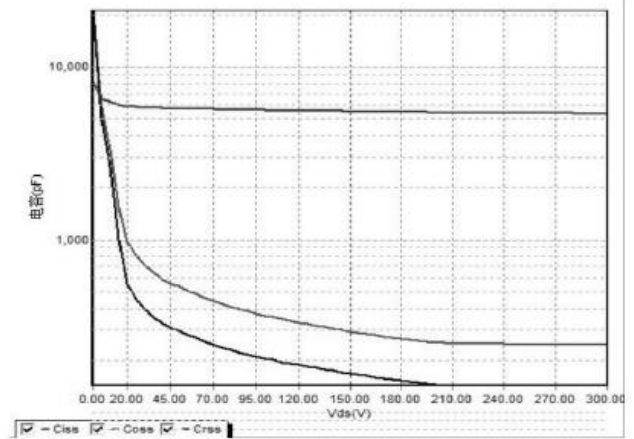


Figure 15. Typical Gate Charge

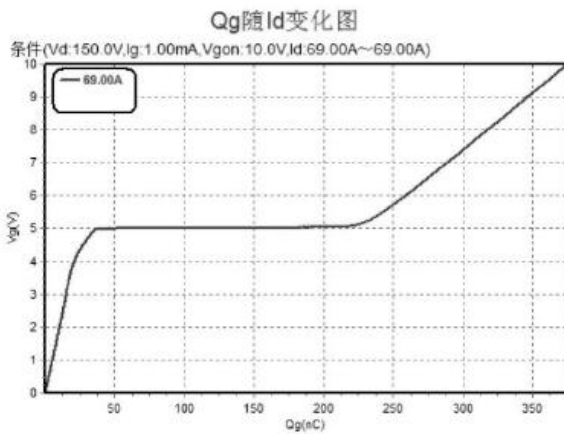
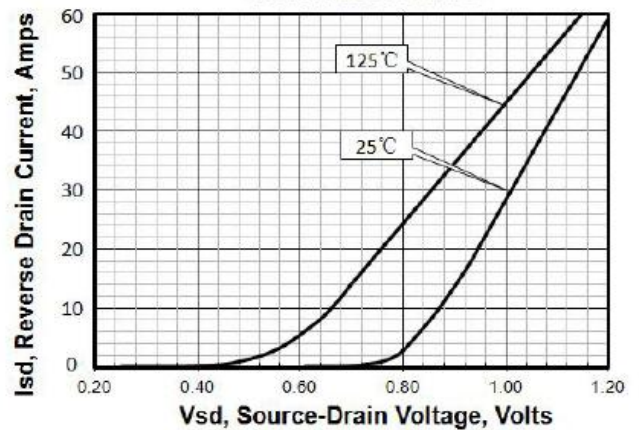


Figure 16. Body Diode Transfer Characteristics



9. Test Circuits and Waveforms

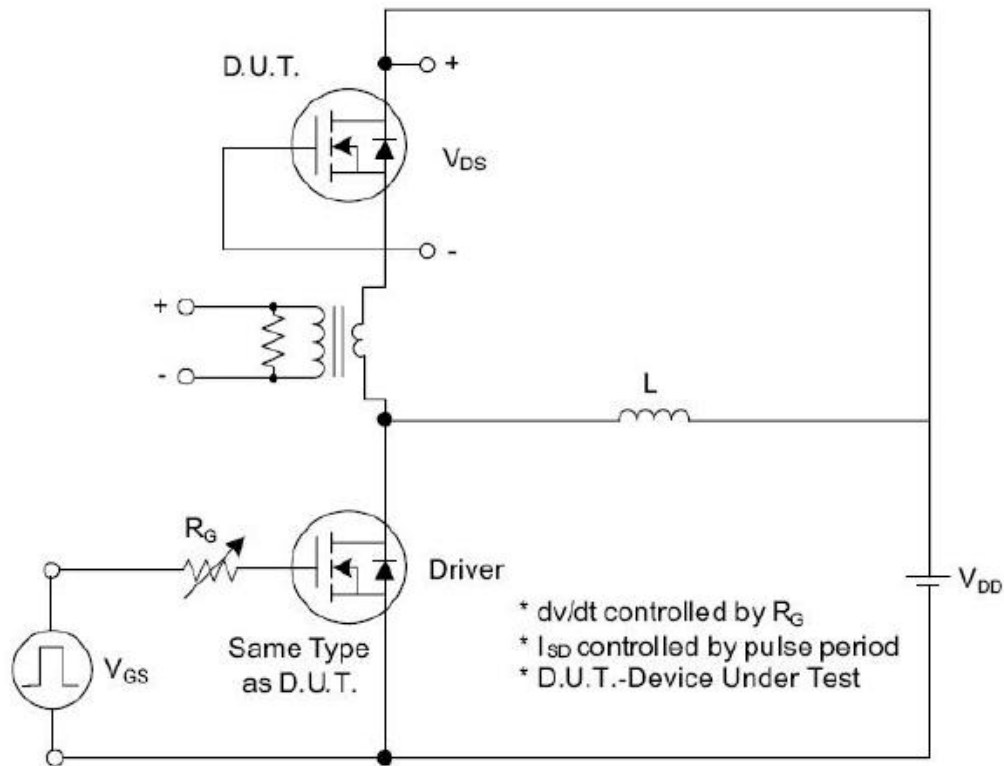


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

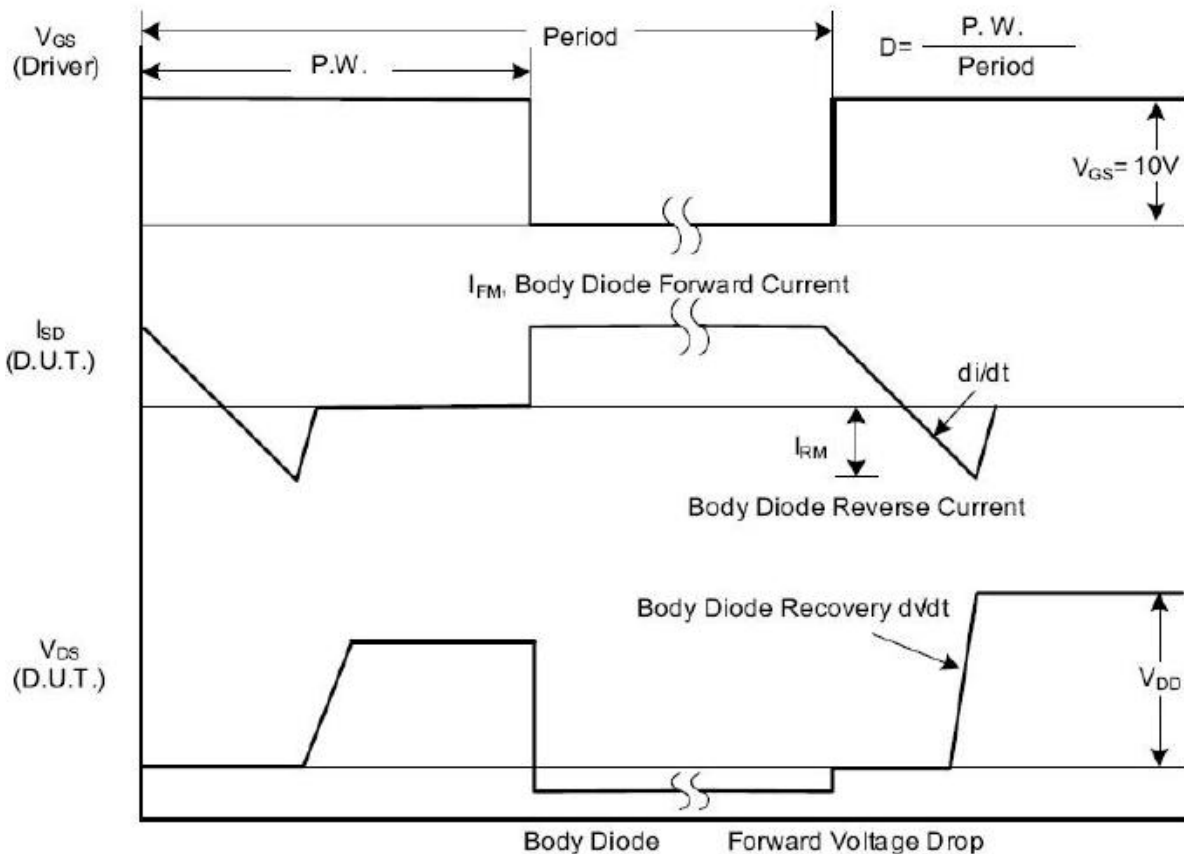


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

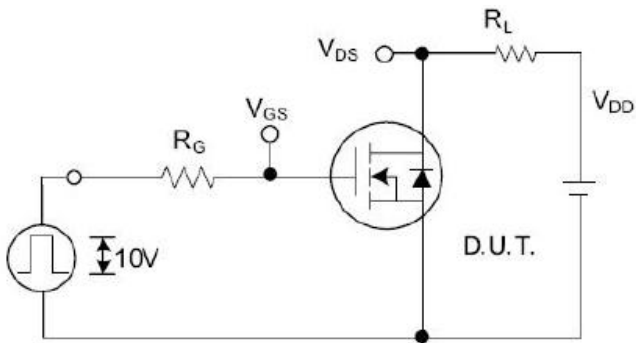


Fig. 2.1 Switching Test Circuit

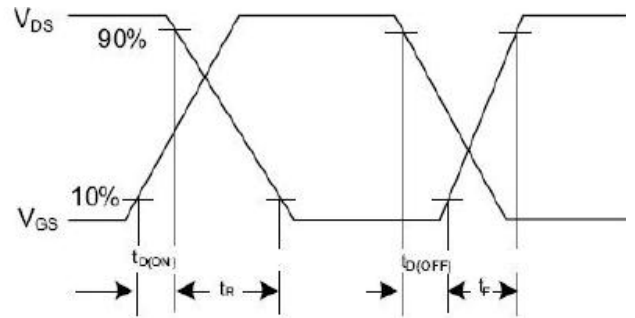


Fig. 2.2 Switching Waveforms

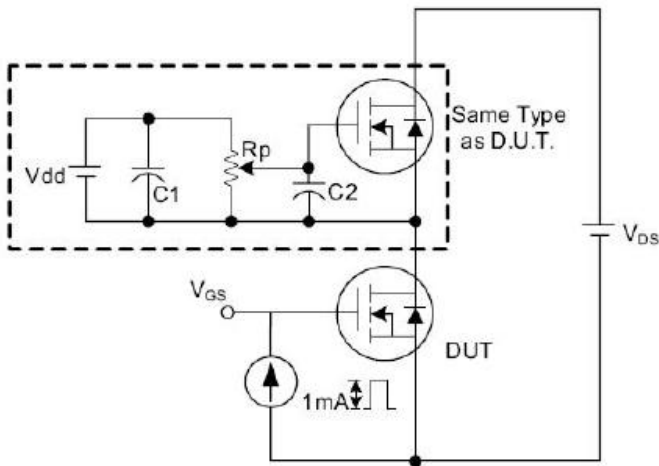


Fig. 3.1 Gate Charge Test Circuit

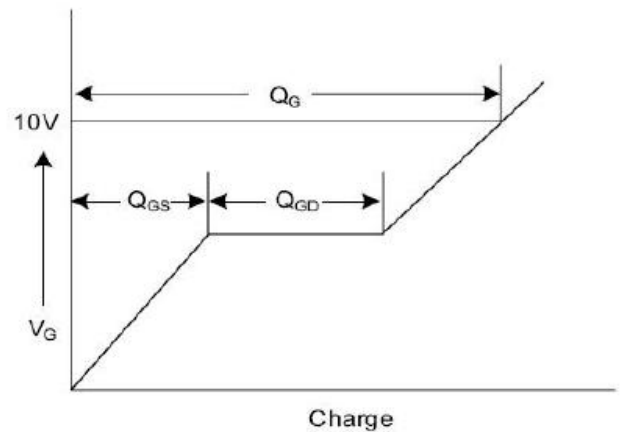


Fig. 3.2 Gate Charge Waveform

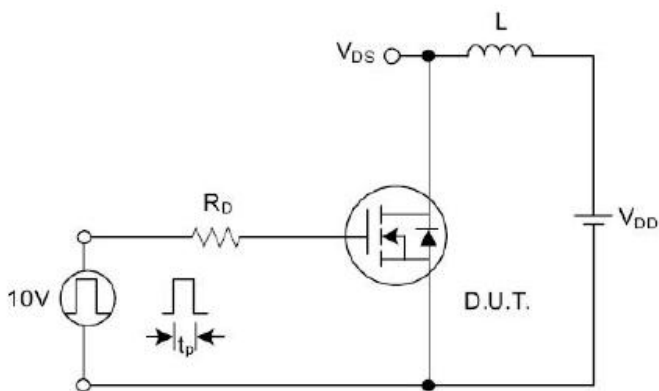


Fig. 4.1 Unclamped Inductive Switching Test Circuit

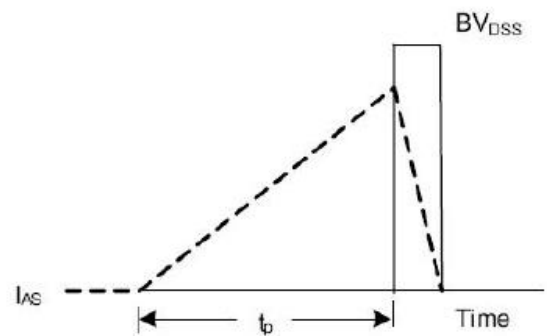


Fig. 4.2 Unclamped Inductive Switching Waveforms