

Description

The UMW UCC27524DR device is a dual-channel, high-speed, low-side, gate-driver device capable of effectively driving MOSFET and IGBT power switches. It has a matching rise and fall time when charging and discharging the gate of the power switch. In addition, UMW UCC27524DR has a high degree of latch resistance under all conditions in its rated power and voltage range. UMW UCC27524DR is not damaged when noise spikes (any polarity) of up to 5V appear on the ground pin. UMW UCC27524DR can accept up to 500mA of reverse current without causing damage or logic confusion. All terminals are fully protected by ESD up to 2.0 kV.

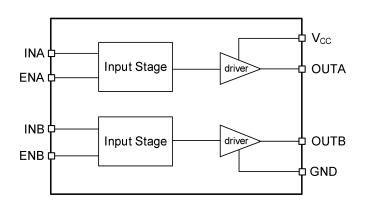
Applications

- line drivers
- Pulse transformer driver
- Driving MOSFETs and IGBTs
- Motor drives
- pulse generator
- Switch-Mode Power Supplies
- DC-to-DC Converters
- class D switching amplifier

Features

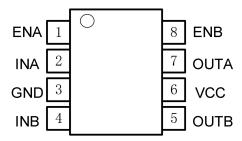
- Latch Protection: withstand 0.5 A reverse current
- Ability to Handle Negative Voltages (-10 V) at Inputs
- Low Output Impedance
- Two Independent Gate-Drive Channel
- Independent-Enable Function for Each Output
- 4-A Peak Source and Sink-Drive Current
- 4.5 to 20-V Single-Supply Range
- High Ability of driving capacitive load:
 - -- Switch time at 1nF load < 25ns
- Rise/Fall time matching
- Fast Propagation Delays (40-ns Typical)
- Operating Temperature Range of -40 to 125°C
- Turn on/Turn off Delays:
 - -- Ton/Toff =70ns/70ns

Pin Configuration





Pin Configuration and Functions



8-Pin SOIC8 Package Top View

Pin Functions

PIN	NAME	DESCRIPTION			
1	ENA	Enable input for Channel A: ENA is biased LOW to disable the Channel A output regardless of the INA state. ENA is biased HIGH or left floating to enable the Channel A output. ENA is allowed to float; hence the pin-to-pin compatibility with the 27524 N/C pin.			
2	INA	Input to Channel A: INA is the non-inverting input in the 27524 device. OUTA is held LOW if INA is unbiased or floating.			
3	GND	Ground: All signals are referenced to this pin.			
4	INB	Input to Channel B: INA is the non-inverting input in the 27524 device. OUTB is held LOW if INB is unbiased or floating.			
5	OUTB	Output of Channel B			
6	VCC	Bias supply input			
7	OUTA	Output of Channel A			
8	ENB	Enable input for Channel B: ENB is biased LOW to disable the Channel B output regardless of the INB state. ENB is biased HIGH or left floating to enable the Channel B output. ENB is allowed to float; hence the pin-to-pin compatibility with the 27524 N/C pin.			



Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. All voltages are with respect to GND unless otherwise noted, Currents are positive into, negative out of the specified terminal, environment temperature is 25 $^{\circ}$ C.

Symbol	Definition	MIN	MAX	UNIT	
Vcc	Supply voltage range	_	25	.,	
V _{IN}	INA, INB voltage	GND-10	V _{CC} +0.3	V	
ESD	Human body model (HBM)	_	2000	V	
	Charged device model (CDM)	_	500	V	
PD	SOIC package power(TA ≤70°C)	_	470	mW	
TJ	Operating junction temperature	_	+150	°C	
Ts	Storage temperature	-45	+150	+150 °C	
Vcc	Supply voltage range	4.5	20	V	
Tc	ambient temperature	-40	125	°C	



Electrical Characteristics

TA= 25°C, 4.5V ≤VCC≤18V (unless otherwise noted)

Symbol	Definition	MIN	TYP	MAX	UNIT
V_{IH}	Input signal high threshold	2.4	_	_	V
V_{IL}	Input signal low threshold		_	0.8	V
I _{IN}	Input current(0V≤V _{IN} ≤V _{CC})		_	300	μA
V_{OH}	High output voltage	V _{CC} -0.025	_	_	V
VoL	Low output voltage	_	_	0.025	V
R _{OH}	Output pullup resistance(V _{CC} =18V,I _O =100mA)	_	0.7	_	Ω
R _{OL}	Output pulldown resistance(V _{CC} =18V,l _O =100mA)	_	04	_	Ω
I _{PK}	Peak output source current		4	_	А
I _{REV}	Reverse current that latch protection can withstand (Working cycle≤2%,t≤300us,V _{CC} =18V)	_	>0.5	_	А
t _R	Rise time(V _{CC} =18V,C _{LOAD} =100pF)	_	_	15	ns
t _F	Fall time(V _{CC} =18V,C _{LOAD} =100pF)	_	_	15	ns
t _{ON}	Turn-on propagation delay(V _{CC} =18V,C _{LOAD} =100pF)	_	25	40	ns
t _{OFF}	Turn-off propagation delay(V _{CC} =18V,C _{LOAD} =100pF)	_	25	40	ns
t _{EN}	Enable propagation delay(Vcc=18V,CLOAD=100pF)	_	25	40	ns
I _{Q1}	VCC quiescent supply current(V _{INA} =V _{INB} =HIGH)	_	_	1.5	mA
I _{Q0}	VCC quiescent supply current(V _{INA} =V _{INB} =LOW)	_	_	1.5	mA

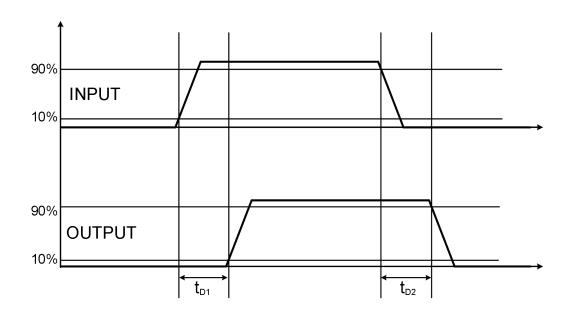


Figure 1 Input-Output waveform(non-inverting)



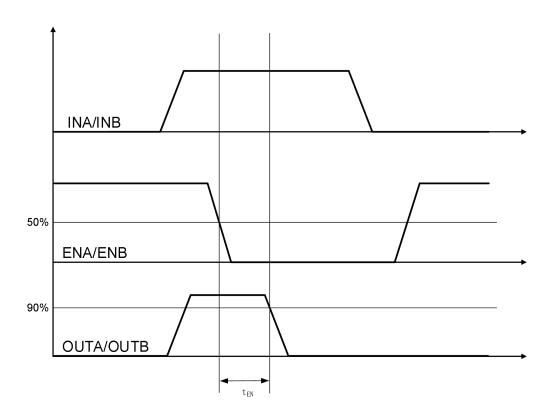


Figure 2 Enable Function waveform



Typical Characteristics

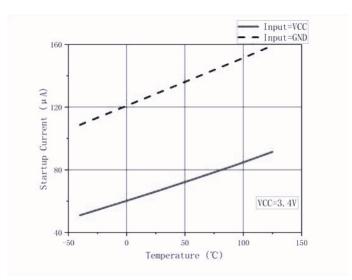


Figure 3. Start-Up Current vs Temperature

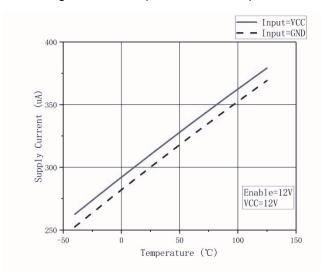


Figure 5. Supply Current vs Temperature (Outputs In DC On/Off Condition)

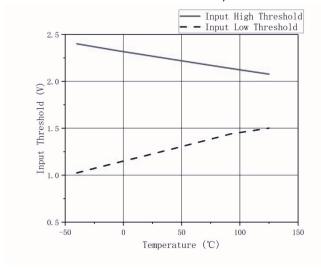


Figure 7. Input Threshold vs Temperature

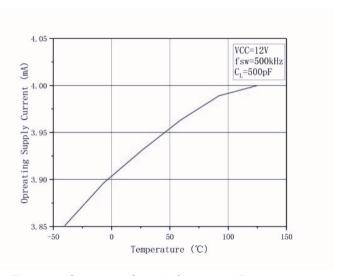


Figure 4. Operating Supply Current vs Temperature (Outputs Switching)

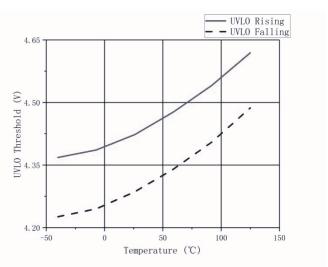


Figure 6. UVLO Threshold vs Temperature

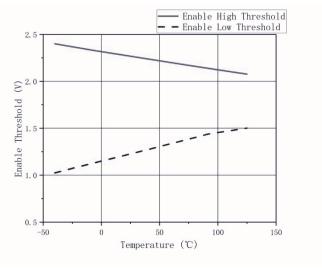


Figure 8. Enable Threshold vs Temperature



Typical Characteristics(continued)

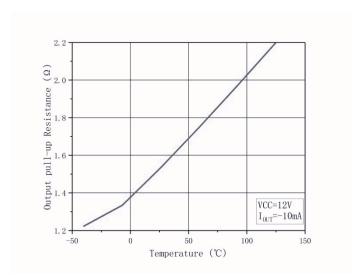


Figure 9. Output Pull-up Resistance vs Temperature

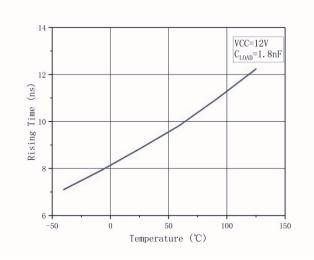


Figure 11. Rise Time vs Temperature

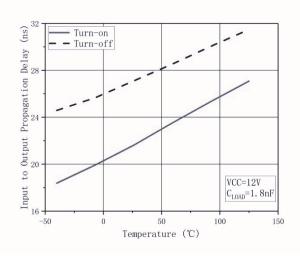


Figure 13. Input to Output Propagation Delay vs
Temperature

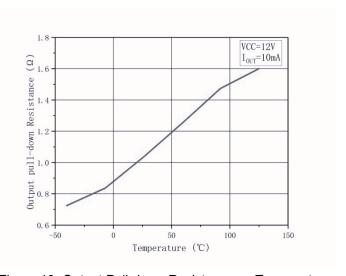


Figure 10. Output Pull-down Resistance vs Temperature

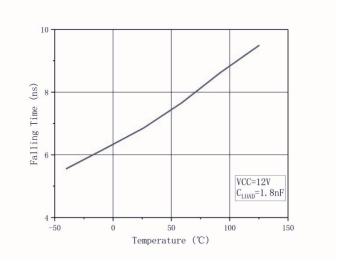


Figure 12. Fall Time vs Temperature

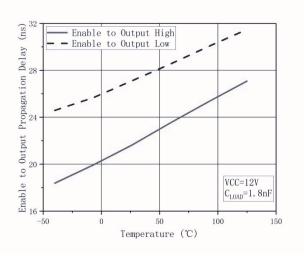


Figure 14. En to Output Propagation Delay vs
Temperature



Typical Characteristics(continued)

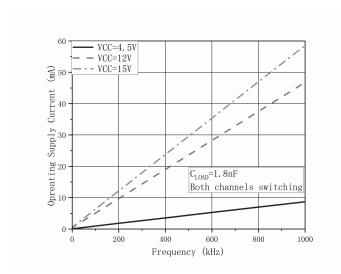


Figure 15. Operating Supply Current vs Frequency

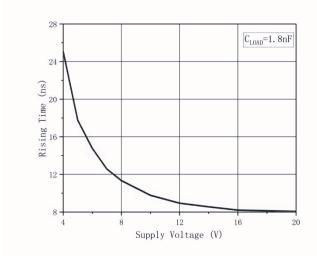


Figure 17. Rise Time vs Supply Voltage

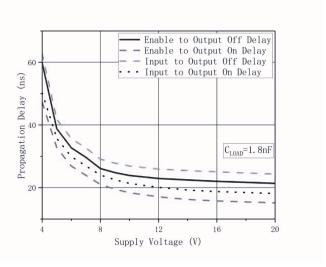


Figure 16. Propagation Delays vs Supply Voltage

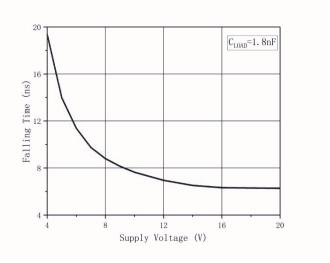


Figure 18. Fall Time vs Supply Voltage

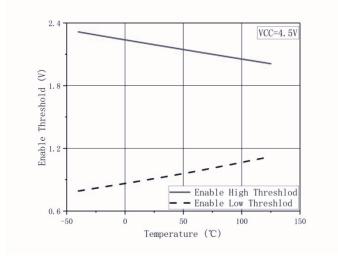
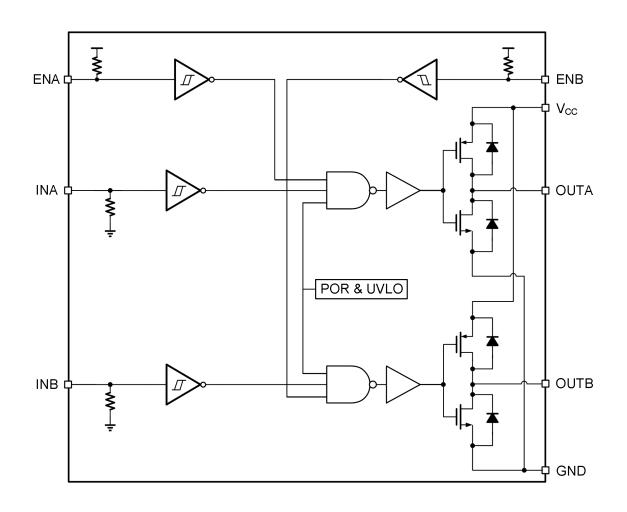


Figure 19. Enable Threshold vs Temperature



Functional Block Diagram



Device Functional Modes

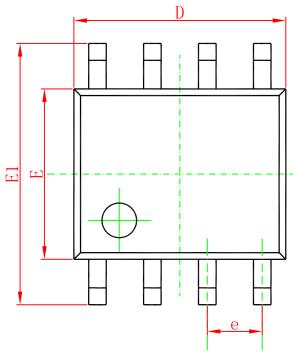
Table 1 Device Logic Table

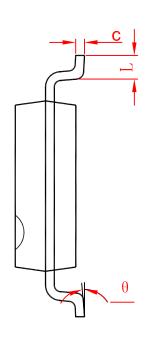
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ENA	ENB	INA	INB	OUTA	OUTB
Н	Н	L	L	L	L
Н	Н	L	Н	L	Н
Н	Н	Н	L	Н	L
Н	Н	Н	Н	Н	Н
L	L	Any	Any	L	L
Any	Any	x ⁽¹⁾	x ⁽¹⁾	L	L
x ⁽¹⁾	x ⁽¹⁾	L	L	L	L
x ⁽¹⁾	x ⁽¹⁾	L	Н	L	Н
x ⁽¹⁾	x ⁽¹⁾	Н	L	Н	Ĺ
x ⁽¹⁾	x ⁽¹⁾	Н	Н	Н	Н

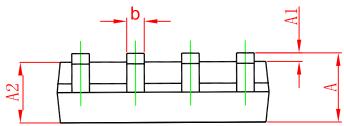
⁽¹⁾ Floating condition.



PACKAGING INFORMATION SOP-8







Cymhal	Dimensions In Millimeters		Dimensions In Inches	
Symbol	Min	Max	Min	Max
Α	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
С	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
е	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



Marking



Ordering information

Order code	Package	Baseqty	Deliverymode
UMW UCC27524DR	SOP-8	2500	Tape and reel