National Semiconductor

August 1998

54ACQ374 • 54ACTQ374
Quiet Series Octal D Flip-Flop with TRI-STATE® Outputs

General Description

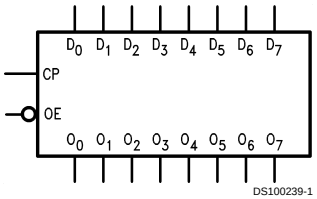
The 'ACQ/'ACTQ374 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops.

The 'ACQ/'ACTQ374 utilizes Quiet Series technology to guarantee quiet output switching and improve dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

Features

- I_{CC} and I_{OZ} reduced by 50%
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Buffered positive edge-triggered clock
- TRI-STATE outputs drive bus lines or buffer memory address registers
- Outputs source/sink 24 mA
- Faster prop delays than the standard 'AC/'ACT374
- 4 kV minimum ESD immunity
- Standard Military Drawing (SMD)
  - — 'ACTQ374: 5962-92189
  - — 'ACQ374: 5962-92179

Logic Symbols



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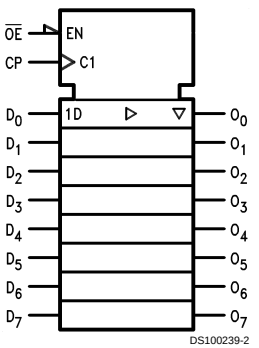
IEEE/IEC



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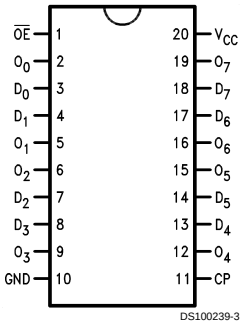
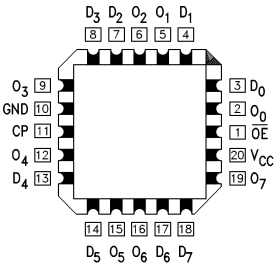
Connection Diagrams

Pin Assignment for DIP and Flatpak



DS100239-3

Pin Assignment for LCC



DS100239-4

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FACT Quiet Series™ is a trademark of Fairchild Semiconductor Corporation.

Connection Diagrams (Continued)

Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	TRI-STATE Output Enable Input
O_0–O_7	TRI-STATE Outputs

Functional Description

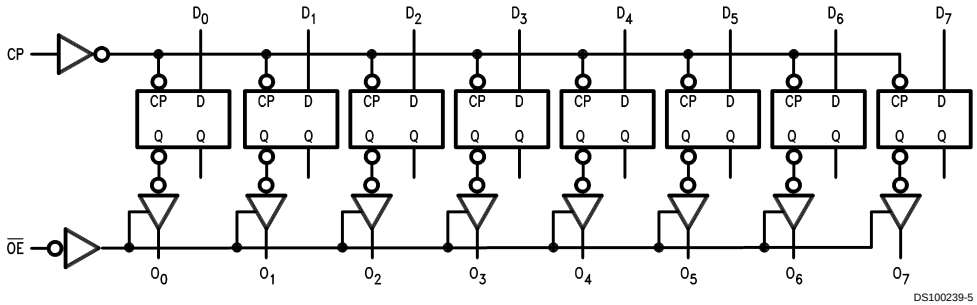
The 'ACQ/'ACTQ374 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Truth Table

Inputs			Outputs
D_n	CP	$\overline{OE}$	O_n
H	⌐	L	H
L	⌐	L	L
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
⌐ = LOW-to-HIGH Transition

Logic Diagram



DS100239-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source	
or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current	
per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65˚C to +150˚C
DC Latch-Up Source or Sink Current	±300 mA
Junction Temperature (T_J)	
CDIP	175˚C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'ACQ	2.0V to 6.0V
'ACTQ	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
54ACQ/ACTQ	−55˚C to +125˚C
Minimum Input Edge Rate ΔV/Δt	
'ACQ Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ΔV/Δt	
'ACTQ devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT® circuits outside databook specifications.

Note 2: All commercial packaging is not recommended for applications requiring greater than 2000 temperature cycles from −40˚C to +125˚C.

DC Characteristics for 'ACQ Family Devices

Symbol	Parameter	V_{CC} (V)	54ACQ T_A = −55˚C to +125˚C Guaranteed Limits	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	3.0	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	3.15		
		5.5	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	1.35		
		5.5	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.9	V	I_{OUT} = −50 μA
		4.5	4.4		
		5.5	5.4		
					(Note 3)
					V_{IN} = V_{IL} or V_{IH}
		3.0	2.4		I_{OH} = −12 mA
		4.5	3.7	V	I_{OH} = −24 mA
		5.5	4.7		I_{OH} = −24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.1	V	I_{OUT} = 50 μA
		4.5	0.1		
		5.5	0.1		
					(Note 3)
		3.0	0.50		I_{OL} = 12 mA
		4.5	0.50	V	I_{OL} = 24 mA
		5.5	0.50		I_{OL} = 24 mA
I_{IN}	Maximum Input Leakage Current	5.5	±1.0	μA	V_I = V_{CC}, GND (Note 5)
I_{OLD}	(Note 4) Minimum Dynamic Output Current	5.5	50	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5	−50	mA	V_{OHD} = 3.85V Min

DC Characteristics for ’ACQ Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	54ACQ T_A = −55˚C to +125˚C Guaranteed Limits	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	5.5	80.0	µA	$V_{IN} = V_{CC}$ or GND (Note 5)
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5	±5.0	µA	V_I(OE) = V_{IL}, V_{IH} $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	1.5	V	(Notes 6, 7)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−1.2	V	(Notes 6, 7)

Note 3: All outputs loaded; thresholds on input associated with output under test.

Note 4: Maximum test duration 2.0 ms, one output loaded at a time.

Note 5: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

I_{CC} for 54ACQ @ 25˚C is identical to 74ACQ @ 25˚C.

Note 6: Plastic DIP Package.

Note 7: Max number of outputs defined as (n). Data inputs are driven 0V to 5V. One output @ GND.

Note 8: Max number of data inputs (n) switching. (n−1) inputs switching 0V to 5V (’ACQ). Input-under-test switching: 5V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

DC Characteristics for ’ACTQ Family Devices

Symbol	Parameter	V_{CC} (V)	54ACTQ T_A = −55˚C to +125˚C Guaranteed Limits	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.4 5.4	V	I_{OUT} = −50 µA
					(Note 9) $V_{IN} = V_{IL}$ or V_{IH}
		4.5 5.5	3.70 4.70	V	I_{OH} = −24 mA I_{OH} = −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.1 0.1	V	I_{OUT} = 50 µA
					(Note 9) $V_{IN} = V_{IL}$ or V_{IH}
		4.5 5.5	0.50 0.50	V	I_{OL} = 24 mA I_{OL} = 24 mA
I_{IN}	Maximum Input Leakage Current	5.5	±1.0	µA	$V_I = V_{CC}$, GND
I_{OZ}	Maximum TRI-STATE Current	5.5	±5.0	µA	$V_I = V_{IL}$, V_{IH} $V_O = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	1.6	mA	$V_I = V_{CC}$ − 2.1V
I_{OLD}	(Note 9) Minimum Dynamic Output Current	5.5	50	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5	−50	mA	V_{OHD} = 3.85V Min

DC Characteristics for 'ACTQ Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	54ACTQ T_A = −55°C to +125°C Guaranteed Limits	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	5.5	80.0	µA	V_{IN} = V_{CC} or GND (Note 11)
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	1.5	V	(Notes 12, 13)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−1.2	V	(Notes 12, 13)

Note 9: All outputs loaded; thresholds on input associated with output under test.

Note 10: Maximum test duration 2.0 ms, one output loaded at a time.

Note 11: I_{CC} for 54ACTQ @ 25°C is identical to 74ACTQ @ 25°C.

Note 12: Plastic DIP package.

Note 13: Max number of outputs defined as (n). Data inputs are driven 0V to 3V. One output @ GND

Note 14: Max number of data inputs (n) switching. (n−1) inputs switching 0V to 3V ('ACTQ). Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V) (Note 15)	54ACQ T_A = −55°C to +125°C C_L = 50 pF Min	54ACQ Max	Units	Fig. No.
f_{max}	Maximum Clock Frequency	3.3	95		MHz	
		5.0	95			
t_{PLH}, t_{PHL}	Propagation Delay CP to O_n	3.3	1.0	16.5	ns	
		5.0	1.0	11.0		
t_{PZL}, t_{PZH}	Output Enable Time	3.3	1.0	16.5	ns	
		5.0	1.0	11.5		
t_{PHZ}, t_{PLZ}	Output Disable Time	3.3	1.0	12.0	ns	
		5.0	1.0	10.5		

Note 15: Voltage Range 5.0 is 5.0V ±0.5V

Voltage Range 3.3 is 3.3V ±0.3V

AC Operating Requirements

Symbol	Parameter	V_{CC} (V) (Note 16)	54ACQ T_A = −55°C to +125°C C_L = 50 pF Guaranteed Minimum	Units	Fig. No.
t_s	Setup Time, HIGH or LOW D_n to CP	3.3	3.0	ns	
		5.0	3.0		
t_h	Hold Time, HIGH or LOW D_n to CP	3.3	2.0	ns	
		5.0	1.5		
t_w	CP Pulse Width, HIGH or LOW	3.3	5.0	ns	
		5.0	5.0		

Note 16: Voltage Range 5.0 is 5.0V ±0.5V

Voltage Range 3.3 is 3.3V ±0.3V

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V) (Note 17)	54ACTQ $T_A = -55^\circ C$ to $+125^\circ C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Max		
f_{max}	Maximum Clock Frequency	5.0	95		MHz	
t_{PLH}, t_{PHL}	Propagation Delay CP to O_n	5.0	2.0	11.5	ns	
t_{PZL}, t_{PZH}	Output Enable Time	5.0	2.0	11.5	ns	
t_{PHZ}, t_{PLZ}	Output Disable Time	5.0	1.5	10.5	ns	

Note 17: Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

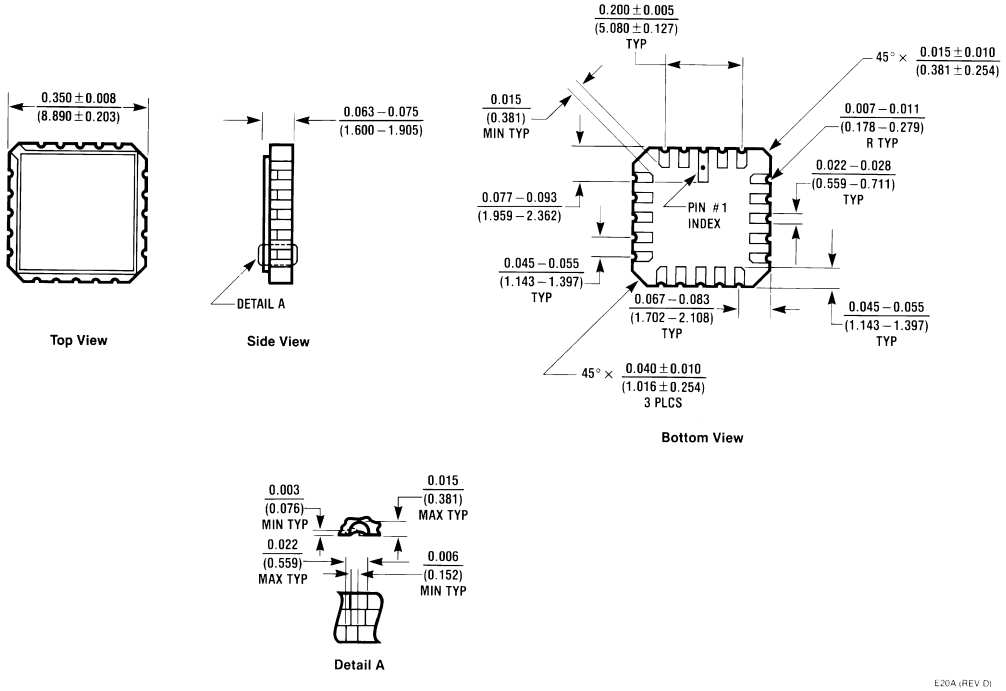
Symbol	Parameter	V_{CC} (V) (Note 18)	54ACTQ $T_A = -55^\circ C$ to $+125^\circ C$ $C_L = 50$ pF Guaranteed Minimum	Units	Fig. No.
t_s	Setup Time, HIGH or LOW D_n to CP	5.0	3.5	ns	
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	2.0	ns	
t_w	CP Pulse Width, HIGH or LOW	5.0	5.0	ns	

Note 18: Voltage Range 5.0 is 5.0V ±0.5V

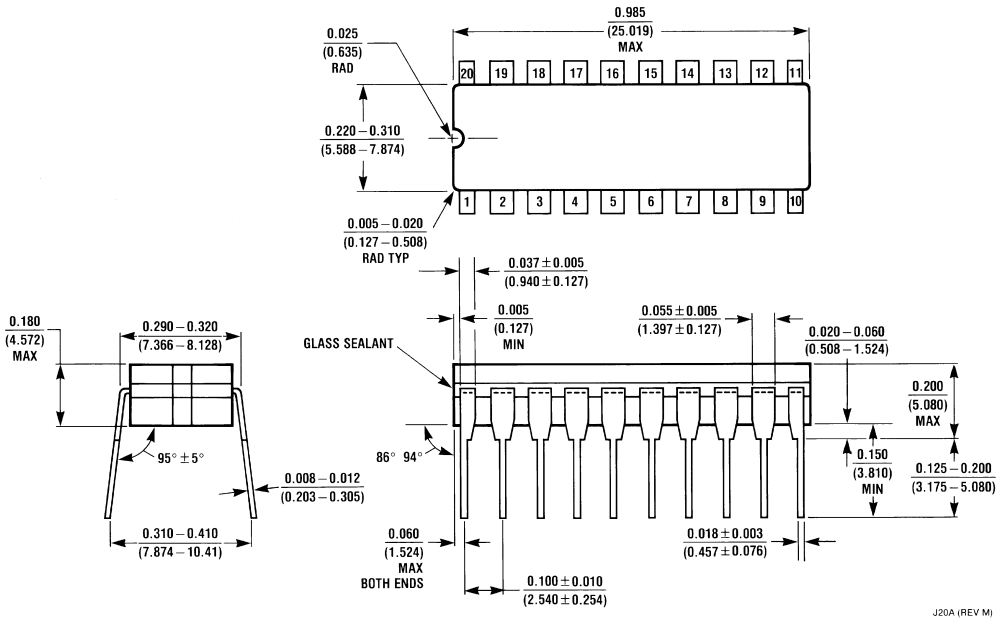
Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = OPEN
C_{PD}	Power Dissipation Capacitance	42.0	pF	V_{CC} = 5.0V

Physical Dimensions inches (millimeters) unless otherwise noted

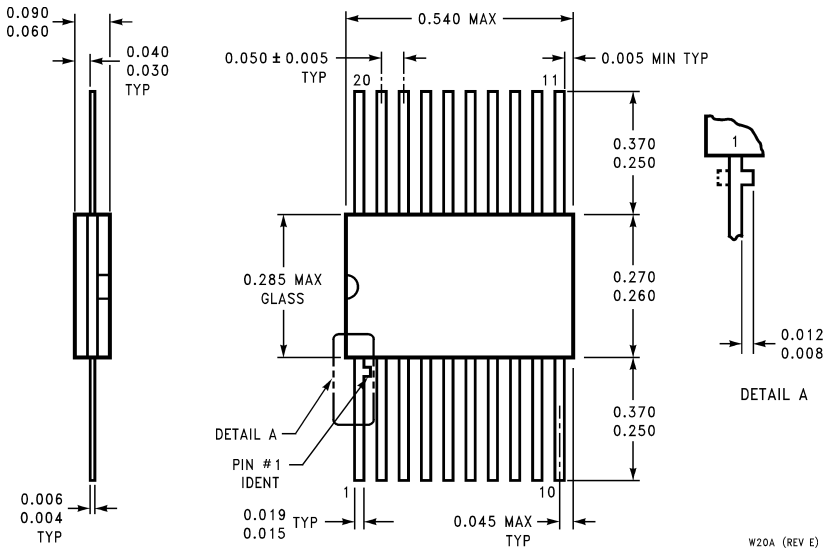


20-Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E20A



20-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J20A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Ceramic Flatpak (F)
NS Package Number W20A

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54ACTQ374 Product Folder

Quiet Series Octal D Flip-Flop with TRI-STATE Outputs

General Description | Features | Datasheet | Package & Models | Samples & Pricing

Datasheet

Title	Size in Kbytes	Date	View Online	Download	Receive via Email
54ACQ374 54ACTQ374 Quiet Series Octal D Flip-Flop with TRI-STATE Outputs	173 Kbytes	4-Sep-98	View Online	Download	Receive via Email
54ACTQ374 Mil-Aero Datasheet MN54ACTQ374-X	17 Kbytes		View Online	Download	Receive via Email
54ACTQ374 Mil-Aero Datasheet MV54ACTQ374-X	22 Kbytes		View Online	Download	Receive via Email

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Package Availability, Models, Samples & Pricing

Part Number	Package			Status	Models		Samples & Electronic Orders	Budgetary Pricing		Std Pack Size	Package Marking
	Type	Pins	MSL		SPICE	IBIS		Qty	$US each		
5962-9218901M2A (54ACTQ374LMQB)	LCC	20	MSL	Full production	N/A	N/A	Buy Now	50+	$9.8000	rail of 50	[logo]¢Z¢S¢4¢A 54ACTQ374 LMQB /Q¢M$E 5962-9218901M2A
5962R9218901M2A (54ACTQ374LMQB-R)	LCC	20	MSL	Full production	N/A	N/A		50+	$70.0000	rail of 50	[logo]¢Z¢S¢4¢A 54ACTQ374 LMQB-R R9218901 M2A Q¢M$E
5962-9218901MRA (54ACTQ374DMQB)	CERDIP	20	MSL	Full production	N/A	N/A	Buy Now	50+	$9.0000	rail of 20	[logo]¢Z¢S¢4¢A$E 54ACTQ374DMQB /Q¢M 5962-9218901MRA
5962R9218901MRA (54ACTQ374DMQB-R)	CERDIP	20	MSL	Full production	N/A	N/A		50+	$75.0000	rail of 20	[logo]¢Z¢S¢4¢A$E 54ACTQ374DMQB-R /Q¢M 5962R9218901MRA
5962-9218901MSA (54ACTQ374FMQB)	CERPACK	20	MSL	Full production	N/A	N/A	Buy Now	50+	$9.8000	rail of 19	[logo]¢Z¢S¢4¢A$E 54ACTQ374FMQB /Q¢M 5962-9218901MSA

5962R9218901MSA (54ACTQ374FMQB-R)	CERPACK	20	MSL	Full production	N/A	N/A		50+	$70.0000	rail of 19	[logo]¢Z¢S¢4¢A$E 54ACTQ374FMQB -R /Q¢M 5962R 9218901MSA
5962R9218901V2A (54ACTQ374ERQMLV)	LCC	20	MSL	Full production	N/A	N/A		50+	$138.0000	rail of 50	[logo]¢Z¢S¢4¢A 54ACTQ374 ERQMLV $E 5962R 9218901V2A
5962R9218901VRA (54ACTQ374JRQMLV)	CERDIP	20	MSL	Full production	N/A	N/A		50+	$138.0000	rail of 20	[logo]¢Z¢S¢4¢A$E 54ACTQ374JRQMLV 5962R9218901VRA
RM54ACTQ374VSA	CERPACK	20	MSL	Preliminary	N/A	N/A				rail of N/A	RM54ACTQ374VSA ¢R WAFER #
5962R9218901VSA (54ACTQ374WRQMLV)	CERPACK	20	MSL	Full production	N/A	N/A		50+	$138.0000	rail of 19	[logo]¢Z¢S¢4¢A$E 54ACTQ374W RQMLV 5962R 9218901VSA

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[Information as of 5-Aug-2002]