

Rochester Electronics Manufactured Components

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Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
 - Class Q Military
 - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
 - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

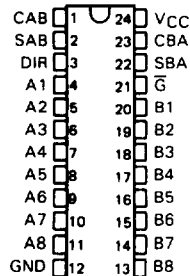
The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

SN74ALS646, SN74ALS648, SN74AS646, SN74AS648
SN54ALS646, SN54ALS648, SN54AS646
OCTAL BUS TRANSCEIVERS AND REGISTERS
 D2681, DECEMBER 1983 - REVISED OCTOBER 1991

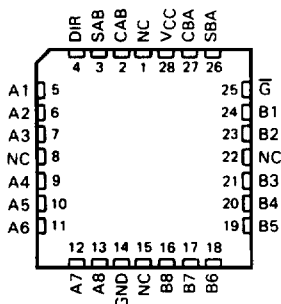
- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data
- Choice of True or Inverting Data Paths
- 3-State Outputs
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

DEVICE	OUTPUT	LOGIC
'ALS646, 'AS646	3-State	True
'ALS648, 'AS648	3-State	Inverting

SN54ALS', SN54AS' . . . JT PACKAGE
 SN74ALS', SN74AS' . . . DW OR NT PACKAGE
 (TOP VIEW)



SN54ALS', SN54AS' . . . FK PACKAGE
 (TOP VIEW)



NC - No internal connection

description

These devices consist of bus transceiver circuits, with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Data on the A or B bus will be clocked into the registers on the low-to-high transition of the appropriate clock pin (CAB or CBA). The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Enable (\bar{G}) and direction (DIR) pins are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select controls (SAB and SBA) can multiplex stored and real-time (transparent mode) data. The circuitry used for select control will eliminate the typical decoding glitch which occurs in a multiplexer during the transition between stored and real-time data. The direction control determines which bus will receive data when enable \bar{G} is active (low). In the isolation mode (control \bar{G} high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

The -1 versions of the SN74ALS' parts are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes.

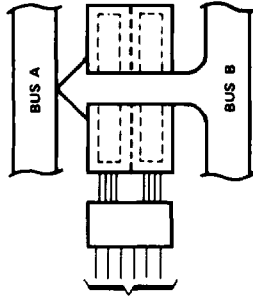
The SN54' family is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



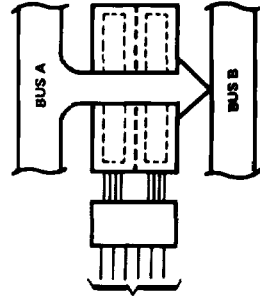
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SN74ALS646, SN74ALS648, SN74AS646, SN74AS648
SN54ALS646, SN54ALS648, SN54AS646
OCTAL BUS TRANSCEIVERS AND REGISTERS



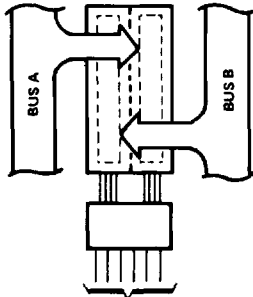
(21)	(3)	(1)	(23)	(2)	(22)
\bar{G}	DIR	CAB	CBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



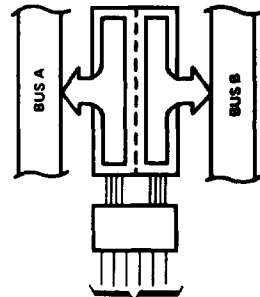
(21)	(3)	(1)	(23)	(2)	(22)
\bar{G}	DIR	CAB	CBA	SAB	SBA
L	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



(21)	(3)	(1)	(23)	(2)	(22)
\bar{G}	DIR	CAB	CBA	SAB	SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B



(21)	(3)	(1)	(23)	(2)	(22)
\bar{G}	DIR	CAB	CBA	SAB	SBA
L	L	X	HorL	X	H
L	H	HorL	X	H	X

TRANSFER
STORED DATA
TO A OR B

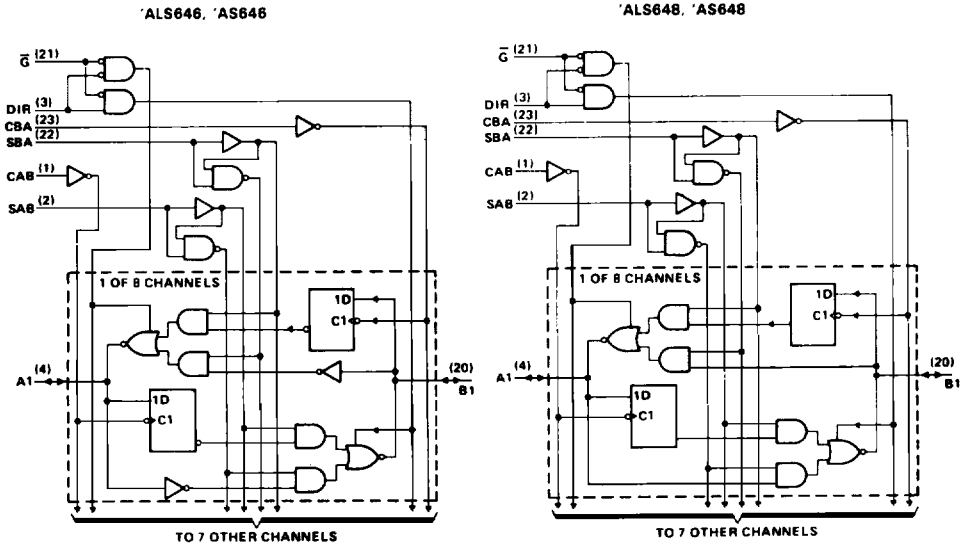
SN74ALS646, SN74ALS648, SN74AS646, SN74AS648
SN54ALS646, SN54ALS648, SN54AS646
OCTAL BUS TRANSCEIVERS AND REGISTERS

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION	
\bar{G}	DIR	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	'ALS646, 'AS646	'ALS648, 'AS648
X	X	↑	X	X	X	Input	Unspecified [†]	Store A, B unspecified [†]	Store A, B unspecified [†]
X	X	X	↑	X	X	Unspecified [†]	Input	Store B, A unspecified [†]	Store B, A unspecified [†]
H	X	↑	↑	X	X	Input	Input	Store A and B Data	Store A and B Data
H	X	H or L	H or L	X	X			Isolation, hold storage	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus	Real-Time \bar{B} Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus	Stored \bar{B} Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus	Real-Time \bar{A} Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus	Stored \bar{A} Data to B Bus

[†]The data output functions may be enabled or disabled by various signals at the \bar{G} and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

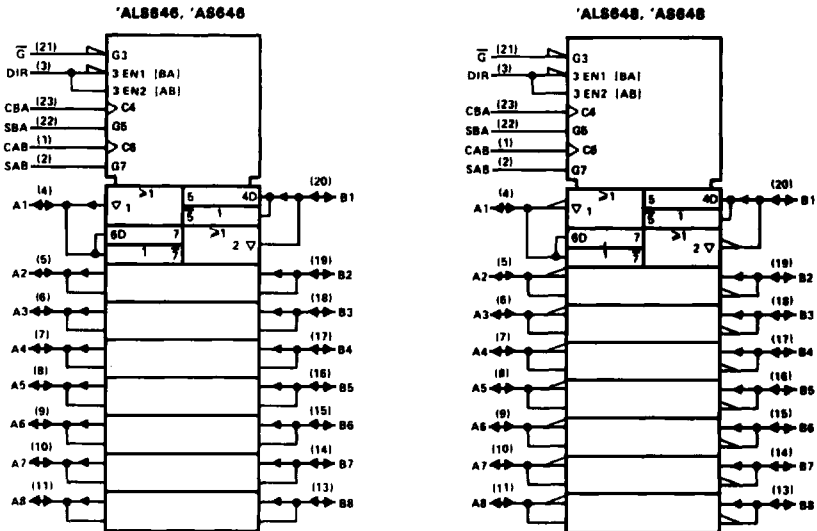
functional block diagrams (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

SN74ALS646, SN74ALS648, SN74AS646, SN74AS648
SN54ALS646, SN54ALS648, SN54AS646
OCTAL BUS TRANSCEIVERS AND REGISTERS

logic symbols†



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, and NT packages.

SN74ALS646, SN54ALS646 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage: Control inputs	7 V
I/O ports	5.5 V
Operating free-air temperature range: SN54ALS646	-55°C to 125°C
SN74ALS646	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SN54ALS646			SN74ALS646			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			-12			-15	mA
I_{OL}	Low-level output current			12			24	mA
							48 [†]	
f_{clock}	Clock frequency	0		35	0		40	MHz
t_w	Pulse duration, clocks high or low	14.5			12.5			ns
t_{su}	Setup time, A before CAB1 or B before CBA1	15			10			ns
t_h	Hold time, A after CAB1 or B after CBA1	1			0			ns
T_A	Operating free-air temperature	-55		125	0		70	°C

[†]The extended condition applies if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS646-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54ALS646		SN74ALS646		UNIT		
			MIN	TYP [‡]	MAX	MIN		TYP [‡]	MAX
V_{IK}		$V_{CC} = 4.5$ V, $I_I = -18$ mA			-1.2		-1.2	V	
V_{OH}		$V_{CC} = 4.5$ V to 5.5 V, $I_{OH} = -0.4$ mA	$V_{CC} - 2$		$V_{CC} - 2$			V	
		$V_{CC} = 4.5$ V, $I_{OH} = -3$ mA	2.4	3.2	2.4	3.2			
		$V_{CC} = 4.5$ V, $I_{OH} = -12$ mA	2						
		$V_{CC} = 4.5$ V, $I_{OH} = -15$ mA			2				
V_{OL}		$V_{CC} = 4.5$ V, $I_{OL} = 12$ mA	0.25	0.4	0.25	0.4		V	
		$V_{CC} = 4.5$ V, $I_{OL} = 24$ mA ($I_{OL} = 48$ mA for -1 version)			0.35	0.5			
I_I	Control inputs	$V_{CC} = 5.5$ V, $V_I = 7$ V			0.1		0.1	mA	
	A or B ports	$V_{CC} = 5.5$ V, $V_I = 5.5$ V			0.1		0.1		
I_{IH}	Control inputs	$V_{CC} = 5.5$ V, $V_I = 2.7$ V			20		20	μ A	
	A or B ports [§]				20		20		
I_{IL}	Control inputs	$V_{CC} = 5.5$ V, $V_I = 0.4$ V			-0.2		-0.2	mA	
	A or B ports [§]				-0.2		-0.2		
I_{OI}		$V_{CC} = 5.5$ V, $V_O = 2.25$ V	-30		-112		-30	-112	mA
I_{CC}		$V_{CC} = 5.5$ V			47	76	47	76	mA
	Outputs high				55	88	55	88	
	Outputs disabled				55	88	55	88	

[‡]All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

[§]For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[†]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

SN74ALS646, SN54ALS646
OCTAL BUS TRANSCEIVERS AND REGISTERS
WITH 3-STATE OUTPUTS

†ALS646 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX				UNIT
			SN54ALS646		SN74ALS646		
			MIN	MAX	MIN	MAX	
t _{max}			35		40		MHz
t _{PLH}	CBA or CAB	A or B	10	36	10	30	ns
t _{PHL}			5	20	5	17	
t _{PLH}	A or B	B or A	5	22	5	20	ns
t _{PHL}			3	15	3	12	
t _{PLH}	SBA or SAB† (with A or B low)	A or B	10	40	15	35	ns
t _{PHL}			5	23	5	20	
t _{PLH}	SBA or SAB† (with A or B high)	A or B	8	30	8	25	ns
t _{PHL}			5	24	5	20	
t _{PZH}	G	A or B	3	20	3	17	ns
t _{PZL}			5	22	5	20	
t _{PHZ}	G	A or B	1	12	1	10	ns
t _{PLZ}			1	20	2	16	
t _{PZH}	DIR	A or B	5	38	8	30	ns
t _{PZL}			5	30	5	25	
t _{PHZ}	DIR	A or B	1	12	1	10	ns
t _{PLZ}			2	21	2	16	

†These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
 NOTE 1: Load circuit and voltage waveforms are shown in Figure 1.

SN74ALS648, SN54ALS648 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage: Control inputs	7 V
I/O ports	5.5 V
Operating free-air temperature range: SN54ALS648	-55°C to 125°C
SN74ALS648	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SN54ALS648			SN74ALS648			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			-12			-15	mA
I_{OL}	Low-level output current			12			24	mA
f_{clock}	Clock frequency			35			40	MHz
t_w	Pulse duration, clocks high or low	14.5			12.5			ns
t_{su}	Setup time, A before $CAB\uparrow$ or B before $CBA\uparrow$	15			10			ns
t_h	Hold time, A after $CAB\downarrow$ or B after $CBA\downarrow$	0			0			ns
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS648			SN74ALS648			UNIT
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IK}	$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$			-1.2			-1.2	V
V_{OH}	$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$, $I_{OH} = -0.4\text{ mA}$	$V_{CC} - 2$			$V_{CC} - 2$			V
	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -3\text{ mA}$	2.4	3.2		2.4	3.2		
	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -12\text{ mA}$	2						
	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -15\text{ mA}$				2			
V_{OL}	$V_{CC} = 4.5\text{ V}$, $I_{OL} = 12\text{ mA}$		0.25	0.4		0.25	0.4	V
	$V_{CC} = 4.5\text{ V}$, $I_{OL} = 24\text{ mA}$ ($I_{OL} = 48\text{ mA}$ for -1 version)					0.35	0.5	
I_I	Control inputs	$V_{CC} = 5.5\text{ V}$, $V_I = 7\text{ V}$			0.1			mA
	A or B ports	$V_{CC} = 5.5\text{ V}$, $V_I = 5.5\text{ V}$			0.1			
I_{IH}	Control inputs	$V_{CC} = 5.5\text{ V}$, $V_I = 2.7\text{ V}$			20			μA
	A or B ports [§]				20			
I_{IL}	Control inputs	$V_{CC} = 5.5\text{ V}$, $V_I = 0.4\text{ V}$			-0.2			mA
	A or B ports [§]				-0.2			
I_O^f	$V_{CC} = 5.5\text{ V}$, $V_O = 2.25\text{ V}$	-30		-112	-30		-112	mA
I_{CC}	$V_{CC} = 5.5\text{ V}$	Outputs high	47	76	47	76	mA	
		Outputs low	57	88	57	88		
		Outputs disabled	57	88	57	88		

[‡]All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

[§]For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

^fThe output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

SN74ALS648, SN54ALS648
OCTAL BUS TRANSCEIVERS AND REGISTERS
WITH 3-STATE OUTPUTS

ALS648 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX				UNIT
			SN54ALS648		SN74ALS648		
			MIN	MAX	MIN	MAX	
f _{max}			35		40		MHz
t _{PLH}	CBA or CAB	A or B	8	39	8	33	ns
t _{PHL}			5	23	5	20	
t _{PLH}	A or B	B or A	3	20	3	17	ns
t _{PHL}			2	12	2	10	
t _{PLH}	SBA or SAB [†] (with A or B low)	A or B	5	44	5	39	ns
t _{PHL}			4	26	4	22	
t _{PLH}	SBA or SAB [†] (with A or B high)	A or B	6	30	6	25	ns
t _{PHL}			6	25	6	21	
t _{PZH}	G	A or B	4	25	4	22	ns
t _{PZL}			4	25	4	22	
t _{PHZ}	G	A or B	1	12	1	10	ns
t _{PLZ}			2	21	2	15	
t _{PZH}	DIR	A or B	4	35	4	27	ns
t _{PZL}			3	25	3	19	
t _{PHZ}	DIR	A or B	1	17	1	14	ns
t _{PLZ}			2	22	2	15	

[†]These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
 NOTE 1: Load circuit and voltage waveforms are shown in Figure 1.

SN74AS646, SN74AS648, SN54AS646 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage: Control inputs	7 V
I/O ports	5.5 V
Operating free-air temperature range: SN54AS646	-55°C to 125°C
SN74AS646, SN74AS648	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SN54AS646			SN74AS646			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage		0.8			0.8		V
I_{OH}	High-level output current			-12			-15	mA
I_{OL}	Low-level output current			32			48	mA
f_{clock}	Clock frequency	0	75		0	90		MHz
t_w	Pulse duration	Clock high	6		5			ns
		Clock low	7		6			
t_{su}	Setup time, A before CAB† or B before CBA†	7			6			ns
t_h	Hold time, A after CAB† or B after CBA†	0			0			ns
T_A	Operating free-air temperature	-55	125		0	70		°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS646			SN74AS646			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$			-1.2			-1.2	V
V_{OH}	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $I_{OH} = -2\text{ mA}$	$V_{CC} - 2$			$V_{CC} - 2$			V
	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -3\text{ mA}$	2.4	3.2		2.4	3.2		
	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -12\text{ mA}$	2						
	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -15\text{ mA}$				2			
V_{OL}	$V_{CC} = 4.5\text{ V}$, $I_{OL} = 32\text{ mA}$		0.25	0.50				V
	$V_{CC} = 4.5\text{ V}$, $I_{OL} = 48\text{ mA}$				0.35	0.50		
I_I	Control inputs	$V_{CC} = 5.5\text{ V}$, $V_I = 7\text{ V}$			0.1			mA
	A or B ports	$V_{CC} = 5.5\text{ V}$, $V_I = 5.5\text{ V}$			0.1			
I_{IH}	Control inputs	$V_{CC} = 5.5\text{ V}$, $V_I = 2.7\text{ V}$			20			μA
	A or B ports [‡]				70			
I_{IL}	Control inputs	$V_{CC} = 5.5\text{ V}$, $V_I = 0.4\text{ V}$			-0.5			mA
	A or B ports [‡]				-0.75			
I_{O}^{\S}	$V_{CC} = 5.5\text{ V}$, $V_O = 2.25\text{ V}$	-30		-112	-30		-112	mA
I_{CC}	'AS646	$V_{CC} = 5.5\text{ V}$	Outputs high	120	196	120	195	mA
			Outputs low	130	211	130	211	
			Outputs disabled	130	211	130	211	

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

SN74AS646, SN54AS646
OCTAL BUS TRANSCEIVERS AND REGISTERS
WITH 3-STATE OUTPUTS

'AS646 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC = 4.5 V to 5.5 V, CL = 50 pF, R1 = 500 Ω, R2 = 500 Ω, TA = MIN to MAX				UNIT
			SN54AS646		SN74AS646		
			MIN	MAX	MIN	MAX	
fmax			75		90		MHz
tPLH	CBA or CAB	A or B	2	9.5	2	8.5	ns
tPHL			2	10	2	9	
tPLH	A or B	B or A	2	11.5	2	9	ns
tPHL			1	8	1	7	
tPLH	SBA or SAB†	A or B	2	13.5	2	11	ns
tPHL			2	11	2	9	
tPZH	G	A or B	2	11	2	9	ns
tPZL			3	15	3	14	
tPHZ	G	A or B	2	11	2	9	ns
tPLZ			2	11	2	9	
tPZH	DIR	A or B	3	21	3	16	ns
tPZL			3	24	3	18	
tPHZ	DIR	A or B	2	12	2	10	ns
tPLZ			2	12	2	10	

SN74AS648
OCTAL BUS TRANSCEIVERS AND REGISTERS
WITH 3-STATE OUTPUTS

recommended operating conditions

		SN74AS648			UNIT
		MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			V
V _{IL}	Low-level input voltage			0.8	V
I _{QH}	High-level output current			-15	mA
I _{QL}	Low-level output current			48	mA
f _{clock}	Clock frequency	0		90	MHz
t _w	Pulse duration	Clock high		5	ns
		Clock low		6	
t _{su}	Setup time, A before CAB _i or B before CBA _i	6			ns
t _h	Hold time, A after CAB _i or B after CBA _i	0			ns
T _A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN74AS648			UNIT
				MIN	TYP [†]	MAX	
V _{IK}		V _{CC} = 4.5 V, I _I = -18 mA			-1.2	V	
V _{OH}		V _{CC} = 4.5 V to 5.5 V, I _{QH} = -2 mA	V _{CC} -2			V	
		V _{CC} = 4.5 V, I _{QH} = -3 mA	2.4	3.2			
		V _{CC} = 4.5 V, I _{QH} = -12 mA					
		V _{CC} = 4.5 V, I _{QH} = -15 mA		2			
V _{OL}		V _{CC} = 4.5 V, I _{QL} = 32 mA				V	
		V _{CC} = 4.5 V, I _{QL} = 48 mA		0.35	0.50		
I _I	Control inputs	V _{CC} = 5.5 V, V _I = 7 V			0.1	mA	
	A or B ports	V _{CC} = 5.5 V, V _I = 5.5 V			0.1		
I _{IH}	Control inputs	V _{CC} = 5.5 V, V _I = 2.7 V			20	μA	
	A or B ports [‡]				70		
I _{IL}	Control inputs	V _{CC} = 5.5 V, V _I = 0.4 V			-0.5	mA	
	A or B ports [‡]				-0.75		
I _{O[§]}		V _{CC} = 5.5 V, V _O = 2.25 V	-30		-112	mA	
I _{CC}	V _{CC} = 5.5 V	Outputs high		110	185	mA	
		Outputs low		120	195		
		Outputs disabled		120	195		

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[‡] For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[§] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

SN74AS648
OCTAL BUS TRANSCEIVERS AND REGISTERS
WITH 3-STATE OUTPUTS

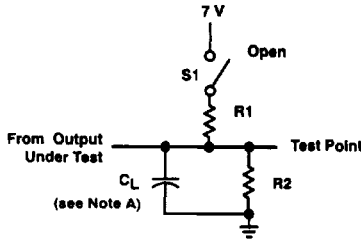
switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX		UNIT
			SN74AS648		
			MIN	MAX	
f _{max}			90		MHz
t _{PLH}	CBA or CAB	A or B	2	8.5	ns
t _{PHL}			2	9	
t _{PLH}	A or B	B or A	2	8	ns
t _{PHL}			1	7	
t _{PLH}	SBA or SAB†	A or B	2	11	ns
t _{PHL}			2	9	
t _{PZH}	0	A or B	2	9	ns
t _{PZL}			3	15	
t _{PHZ}	0	A or B	2	9	ns
t _{PLZ}			2	9	
t _{PZH}	DIR	A or B	3	16	ns
t _{PZL}			3	18	
t _{PHZ}	DIR	A or B	2	10	ns
t _{PLZ}			2	10	

†These parameters are measured with the internal output state of the storage register opposite of that of the bus input.
 NOTE 1: Load circuit and voltage waveforms are shown in Figure 1.

**SN74ALS646, SN74ALS648, SN74AS646, SN74AS648
SN54ALS646, SN54ALS648, SN54AS646
OCTAL BUS TRANSCEIVERS AND REGISTERS**

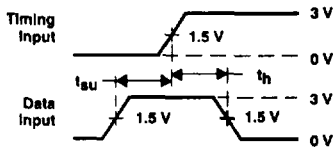
PARAMETER MEASUREMENT INFORMATION



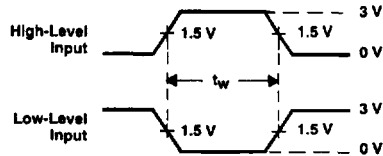
SWITCH POSITION TABLE

TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed

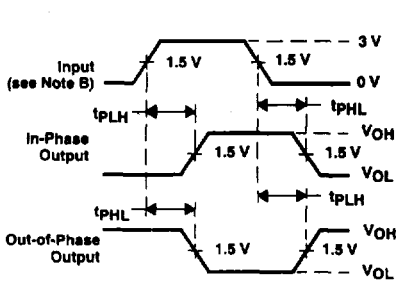
LOAD CIRCUIT FOR 3-STATE OUTPUTS



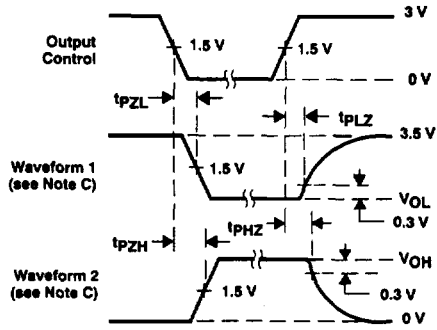
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

- Notes: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_0 = 50 \Omega$, $t_r \leq 2$ ns, $t_f \leq 2$ ns.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms