National Semiconductor

DS3883A BTL 9-Bit Data Transceiver

General Description

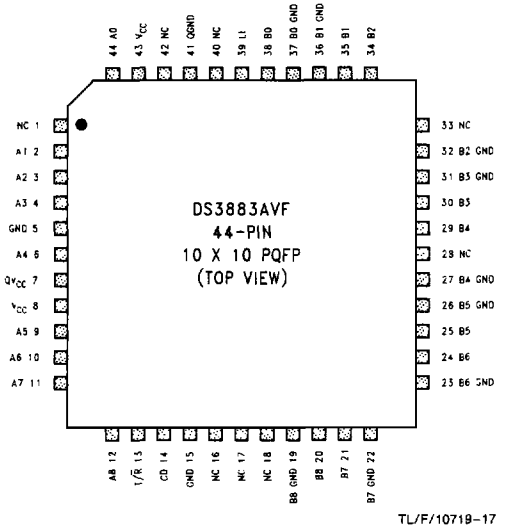
The DS3883A is one in a series of transceivers designed specifically for the implementation of high performance Futurebus+ and proprietary bus interfaces. The DS3883A, is a BTL 9-bit Transceiver designed to conform to IEEE 1194.1 (Backplane Transceiver Logic—BTL) as specified in the IEEE 896.2 Futurebus+ specification. Utilization of the DS3883A simplifies the implementation of byte wide address/data with parity lines and also may be used for the Futurebus+ status, tag and command lines.

The DS3883A driver output configuration is an NPN open collector which allows Wired-OR connection on the bus. Each driver output incorporates a Schottky diode in series with its collector to isolate the transistor output capacitance from the bus thus reducing the bus loading in the inactive state. The combined output capacitance of the driver and receiver input is less than 5 pF. The driver also has high sink current capability to comply with the bus loading requirements defined within IEEE 1194.1 BTL specification.
(Continued)

Features

- 9-bit Inverting BTL transceiver meets IEEE 1194.1 standard on Backplane Transceiver Logic (BTL)
- Supports live insertion
- Glitch free power-up/down protection
- Typically less than 5 pF bus-port capacitance
- Low bus-port voltage swing (typically 1V) at 80 mA
- Open collector bus-port output allows Wired-OR connection
- Controlled rise and fall time to reduce noise coupling to adjacent lines
- TTL compatible driver and control inputs
- Built in bandgap reference with separate QV_{CC} and QGND pins for precise receiver thresholds
- Exceeds 2 kV ESD (Human Body Model)
- Individual bus-port ground pins minimize ground bounce
- Product offered in PLCC and PQFP package styles
- 7 x 7 PQFP requires 50% less PCB space than 10 x 10 PQFP
- Tight skew (1 ns typical)

Connection Diagrams



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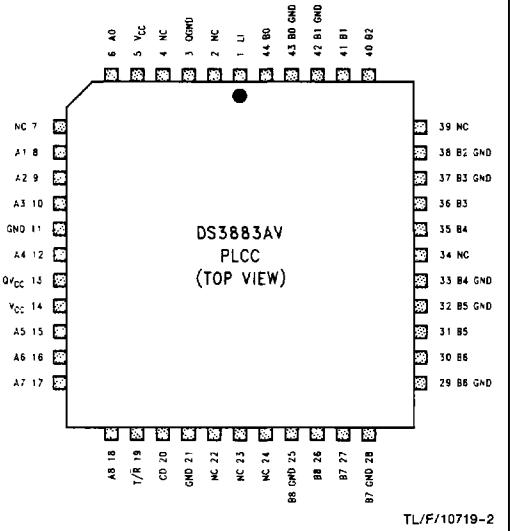

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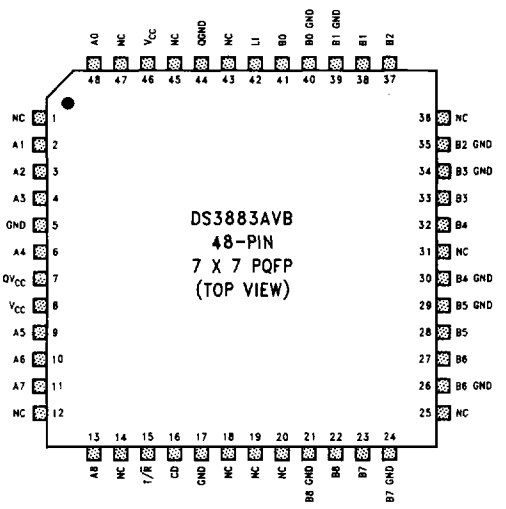
Connection Diagrams (Continued)



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(Note: NC = No Connect)

Order Number DS3883AV, DS3883AVF or DS3883AVB
See NS Package Number V44A, VF44B orVBH48A

General Description (Continued)

Backplane Transceiver Logic (BTL) is a signaling standard that was invented and first introduced by National Semiconductor, then developed by the IEEE to enhance the performance of backplane buses. BTL compatible transceivers feature low output capacitance drivers to minimize bus loading, a 1V nominal signal swing for reduced power consumption and receivers with precision thresholds for maximum noise immunity. BTL eliminates settling time delays that severely limit TTL bus performance, and thus provide significantly higher bus transfer rates. The backplane bus is intended to be operated with termination resistors (selected to match the bus impedance) connected to 2.1V at both ends. The low voltage is typically 1V.

Separate ground pins are provided for each BTL output to minimize induced ground noise during simultaneous switching.

The unique driver circuitry meets the maximum slew rate of 0.5 V/ns which allows controlled rise and fall times to reduce noise coupling to adjacent lines.

The transceiver's control and driver inputs are designed with high impedance PNP input structures and are fully TTL compatible.

The receiver is a high speed comparator that utilizes a bandgap reference for precision threshold control allowing maximum noise immunity to the BTL 1V signaling level. Separate QV_{CC} and QGND pins are provided to minimize the effects of high current switching noise. The output is TRI-STATE® and fully TTL compatible.

The DS3883A supports live insertion as defined in 896.2 through the LI (Live Insertion) pin. To implement live insertion the LI pin should be connected to the live insertion power connector. If this function is not supported the LI pin must be tied to the V_{CC} pin. The DS3883A also provides glitch free power up/down protection during power sequencing.

The DS3883A has two types of power connections in addition to the LI pin. They are the Logic V_{CC} (V_{CC}) and the Quiet V_{CC} (QV_{CC}). There are two logic V_{CC} pins on the DS3883 that provide the supply voltage for the logic and control circuitry. Multiple power pins reduce the effects of package inductance and thereby minimize switching noise. As these pins are common to the V_{CC} bus internal to the device, a voltage delta should never exist between these pins and the voltage difference between V_{CC} and QV_{CC} should never exceed ±0.5V because of ESD circuitry.

Additionally, the ESD circuitry between the V_{CC} pins and all other pins except for BTL I/O's and LI pins requires that any voltage on these pins should not exceed the voltage on V_{CC} + 0.5V.

There are three different types of ground pins on the DS3883A. They are the logic ground (GND), BTL grounds (B0GND–B8GND) and the Bandgap reference ground (QGND). All of these ground reference pins are isolated within the chip to minimize the effects of high current switching transients. For optimum performance the QGND should be returned to the connector through a quiet channel that does not carry transient switching current. The GND and B0GND–B8GND should be connected to the nearest backplane ground pin with the shortest possible path.

Since many different grounding schemes could be implemented and ESD circuitry exists on the DS3883, it is important to note that any voltage difference between ground pins, QGND, GND or B0GND–B8GND should not exceed ±0.5V including power-up/down sequencing.

When CD (Chip Disable) is high, An and Bn are in a high impedance state. To transmit data (An to Bn) the T/$\overline{R}$ signal is high. To receive data (Bn to An) the T/$\overline{R}$ signal is low.

Additional transceivers included in the Futurebus+ family are the DS3884A BTL Handshake Transceiver featuring selectable Wired-OR glitch filtering; the DS3885 BTL Arbitration Transceiver with arbitration competition logic for the AB<7:0>/$\overline{ABP}$ signal lines; and the DS3886A BTL 9-bit Latching Data Transceiver featuring edge triggered latches in the driver which may be bypassed during a fall-through mode and a transparent latch in the receiver.

The DS3875 Arbitration Controller included in the Futurebus+ family supports all the required and optional modes for Futurebus+ arbitration protocol. It is designed to be used in conjunction with the DS3884A and DS3885 transceivers.

The Logical Interface Futurebus+ Engine (LIFE) is a high performance Futurebus+ Protocol Controller designed for IEEE P896.1. The LIFE will handle all handshaking signals between the Futurebus+ and the local bus interface. The LIFE supports the Futurebus+ compelled mode data transfer as both master and slave. The LIFE can be configured to operate in compliance to IEEE 896.2 Profile B mode. The LIFE incorporates a DMA controller and 64-bit FIFO's for fast queuing. The DS3883A is offered in 44-pin PLCC, 44-pin PQFP, and 48-pin PQFP high density package styles.

The 48-pin PQFP is a 7 x 7 space savings package that requires 50% less PCB space than the 44-pin 10 x 10 PQFP package.

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage		6.5V
Control Input Voltage		6.5V
Driver Input and Receiver Output		5.5V
Receiver Input Current		±15 mA
Bus Termination Voltage		2.4V
Power Dissipation at 25°C	PLCC (V44A)	2.5W
	PQFP (VF44B)	1.3W
	PQFP (VBH48A)	1.59W

Derate PLCC Package (V44A)	20 mW/°C
Derate PQFP Package (VF44A)	11.1 mW/°C
Derate PQFP Package (VBH48A)	12.8 mW/°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.5	5.5	V
Bus Termination Voltage (V_T)	2.06	2.14	V
Operating Free Air Temperature	0	70	°C

DC Electrical Characteristics (Notes 2 and 3) T_A = 0°C to +70°C, V_{CC} = 5V ±10%

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER AND CONTROL INPUT (CD, T/$\overline{R}$, An)						
V_{IH}	Minimum Input High Voltage		2.0			V
V_{IL}	Maximum Input Low Voltage				0.8	V
I_I	Input Leakage Current	$V_{IN} = V_{CC} = 5.5V$			250	μA
I_{IH}	Input High Current	$V_{IN} = 2.4V$, AN = CD = 0.5V, T/$\overline{R}$ = 2.4V			40	μA
I_{IL}	Input Low Current	$V_{IN} = 0.5V$, AN = CD = 0.5V, T/$\overline{R}$ = 2.4V			−100	μA
V_{CL}	Input Diode Clamp Voltage	I_{CLAMP} = −12 mA			−1.2	V
DRIVER OUTPUT/RECEIVER INPUT (Bn)						
V_{OLB}	Output Low Bus Voltage (Note 5)	An = T/$\overline{R}$ = 2.4V, CD = 0.5V, I_{OL} = 80 mA	0.75	1.0	1.1	V
I_{OFF}	Output Off Low Current	An = 0.5V, T/$\overline{R}$ = 2.4V, Bn = 0.75V, CD = 0.5V			−200	μA
	Output Off High Current	An = 0.5V, T/$\overline{R}$ = 2.4V, Bn = 2.1V, CD = 0.5V			200	μA
	Output Off Low Current—Chip Disabled	An = 0.5V, T/$\overline{R}$ = CD = 2.4V, Bn = 0.75V			−50	μA
	Output Off Low Current—Chip Disabled	An = 0.5V, T/$\overline{R}$ = CD = 2.4V, Bn = 2.1V			50	μA
V_{TH}	Receiver Input Threshold	T/$\overline{R}$ = CD = 0.5V	1.47	1.55	1.62	V
V_{CLP}	Positive Clamp Voltage	V_{CC} = Max or 0V, I_{Bn} = 1 mA, CD = T/$\overline{R}$ = 0V, An = 0V	2.4	3.4	4.5	V
		V_{CC} = Max or 0V, I_{Bn} = 10 mA, CD = T/$\overline{R}$ = 0V, An = 0V	2.9	3.9	5.0	V
V_{CLN}	Negative Clamp Voltage	I_{CLAMP} = −12 mA, CD = T/$\overline{R}$ = 0.5V			−1.2	V
RECEIVER OUTPUT (An)						
V_{OH}	Voltage Output High	Bn = 1.1V, T/$\overline{R}$ = CD = 0.5V, I_{OH} = −2 mA	2.4	3.2		V
V_{OL}	Voltage Output Low	T/$\overline{R}$ = CD = 0.5V, Bn = 2.1V, I_{OL} = 24 mA		0.35	0.5	V
		T/$\overline{R}$ = CD = 0.5V, Bn = 2.1V, I_{OL} = 8 mA		0.35	0.4	V
I_{OZ}	TRI-STATE® Leakage Current	An = 2.4V, CD = 2.4V, T/$\overline{R}$ = 0.5V			10	μA
		An = 0.5V, CD = 2.4V, T/$\overline{R}$ = 0.5V			−10	μA
I_{OS}	Output Short Circuit Current	Bn = 1.1V, T/$\overline{R}$ = CD = 0.5V (Note 4)	−40	−70	−100	mA
SUPPLY CURRENT						
I_{CC}	Supply Current: Includes V_{CC}, QV_{CC} and LI	T/$\overline{R}$ = All An Inputs = 2.4V, CD = 0.5V			62	mA
		CD = T/$\overline{R}$ = 0.5V, All Bn Inputs = 2.1V			53	mA

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DC Electrical Characteristics (Notes 2 and 3) T_A = 0°C to +70°C, V_{CC} = 5V ±10% (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SUPPLY CURRENT (Continued)						
I_{LI}	Live Insertion Current	T/$\overline{R}$ = CD = An = 0.5V, Bn = Open, V_{CC} = QV_{CC} = 5.5V			2.2	mA
		T/$\overline{R}$ = All An = 2.4V, CD = 0.5V, Bn = Open V_{CC} = QV_{CC} = 5.5V			4.5	mA

Note 1: "Absolute Maximum Ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All input and/or output pins shall not exceed V_{CC} + 0.5V and shall not exceed the absolute maximum rating at any time, including power-up and power-down. This prevents the ESD structure from being damaged due to excessive currents flowing from the input and/or output pins to QV_{CC} and V_{CC}. There is a diode between each input and/or output to V_{CC} which is forward biased when incorrect sequencing is applied. LI and Bn pins do not have power sequencing requirements with respect to V_{CC} and QV_{CC}.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified. All typical values are specified under these conditions: V_{CC} = 5V and T_A = 25°C, unless otherwise stated.

Note 4: Only one output should be shorted at a time, and duration of the short should not exceed one second.

Note 5: Referenced to appropriate signal ground. Do not exceed maximum power dissipation of package.

AC Electrical Characteristics T_A = 0°C to +70°C, V_{CC} = 5V ±10% (Note 6)

This AC table applies to DS3883AVF (10 x 10 PQFP) and DS3883AV (PLCC) only.

Symbol	Parameter		Conditions	Min	Typ	Max	Units
DRIVER							
t_{PHL}	An to Bn	Propagation Delay	CD = 0V, T/$\overline{R}$ = 3V (*Figures 1* and *2*)	1	3.5	6	ns
t_{PLH}				1	3.5	6	ns
t_{PHL}	CD to Bn	Enable Time	T/$\overline{R}$ = An = 3V (*Figures 1* and *3*)	3	6	9	ns
t_{PLH}		Disable Time		2.5	5	8	ns
t_{PHL}	T/$\overline{R}$ to Bn	Enable Time	(*Figures 8* and *9*) CD = 0V	9	13.5	18	ns
t_{PLH}		Disable Time		2	6	10	ns
t_r	Transition Time—Rise/Fall 20% to 80%		(*Figures 1* and *2*) CD = 0V, T/$\overline{R}$ = 3V (Note 10)	1	2.5	4.5	ns
t_f				1	2	4.5	ns
SR	Slew Rate is Calculated from from 1.3V to 1.8V		(*Figures 1* and *2*) (Note 10) CD = 0V T/$\overline{R}$ = 3V			0.5	V/ns
t_{SKEW}	An to Bn Skew (Same Package)		(Note 7)		1	3.5	ns
RECEIVER							
t_{PHL}	Bn to An		CD = T/$\overline{R}$ = 0V (*Figures 4* and *5*)	2	4	7	ns
t_{PLH}				1.5	4.5	7.5	ns
t_{PLZ}	CD to An	Disable Time	Bn = 2.1V, T/$\overline{R}$ = 0V (*Figures 6* and *7*)	4	8	12	ns
t_{PZL}		Enable Time		2.5	6	9	ns
t_{PHZ}		Disable Time	Bn = 1.1V, T/$\overline{R}$ = 0V (*Figures 6* and *7*)	3	6.5	10	ns
t_{PZH}		Enable Time		2	6	10	ns
t_{PLZ}	T/$\overline{R}$ to An	Disable Time	CD = 0V Bn = 2.1V (*Figures 8* and *9*)	3	7	12	ns
t_{PZL}		Enable Time		4	10	16	ns
t_{PHZ}		Disable Time	Bn = 1.1V, CD = 0V (*Figures 6* and *7*)	2	6.5	10	ns
t_{PZH}		Enable Time		3	7	11	ns
t_{SKEW}	Bn to An Skew (Same Package)		(Note 7)		1	3.5	ns
PARAMETERS NOT TESTED							
C_{output}	BTL Output Capacitance		(Note 8)		5		pF
t_{NR}	Noise Rejection		(Note 9)		1		ns

AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$ (Note 6)

This AC table applies to DS3883AVB (7 x 7 PQFP) only.

Symbol	Parameter		Conditions	Min	Typ	Max	Units
DRIVER							
t_{PHL}	An to Bn	Propagation Delay	CD = 0V, T/$\overline{R}$ = 3V (*Figures 1* and *2*)	0.5	2	5.5	ns
t_{PLH}				0.5	3	5.5	ns
t_{PHL}	CD to Bn	Enable Time	T/$\overline{R}$ = An = 3V (*Figures 1* and *3*)	2	5	9	ns
t_{PLH}		Disable Time		2	4	7.5	ns
t_{PHL}	T/$\overline{R}$ to Bn	Enable Time	(*Figures 8* and *9*) CD = 0V	9.5	12	17	ns
t_{PLH}		Disable Time		0.5	5	10	ns
t_r	Transition Time—Rise/Fall 20% to 80%		(*Figures 1* and *2*) CD = 0V, T/$\overline{R}$ = 3V (Note 10)	0.5	1.5	4.5	ns
t_f				0.5	1.5	4.5	ns
SR	Slew Rate is Calculated from from 1.3V to 1.8V		(*Figures 1* and *2*) (Note 10) CD = 0V T/$\overline{R}$ = 3V		0.4	0.85	V/ns
t_{SKEW}	An to Bn Skew (Same Package)		(Note 7)		1	3.5	ns
RECEIVER							
t_{PHL}	Bn to An		CD = T/$\overline{R}$ = 0V (*Figures 4* and *5*)	1.5	4	7	ns
t_{PLH}				1.5	4	7.5	ns
t_{PLZ}	CD to An	Disable Time	Bn = 2.1V, T/$\overline{R}$ = 0V (*Figures 6* and *7*)	5	7	12	ns
t_{PZL}		Enable Time		1	5	9	ns
t_{PHZ}		Disable Time	Bn = 1.1V, T/$\overline{R}$ = 0V (*Figures 6* and *7*)	2.5	6.5	10	ns
t_{PZH}		Enable Time		1.5	4.5	10	ns
t_{PLZ}	T/$\overline{R}$ to An	Disable Time	CD = 0V Bn = 2.1V (*Figures 8* and *9*)	3.5	6.5	12	ns
t_{PZL}		Enable Time		6	10	16	ns
t_{PHZ}		Disable Time	Bn = 1.1V, CD = 0V (*Figures 6* and *7*)	1	6	11	ns
t_{PZH}		Enable Time		2	5	11	ns
t_{SKEW}	Bn to An Skew (Same Package)		(Note 7)		0	3.5	ns
PARAMETERS NOT TESTED							
C_{output}	BTL Output Capacitance		(Note 8)		5		pF
t_{NR}	Noise Rejection		(Note 9)		1		ns

Note 6: Input waveforms shall have a rise/fall time of 3 ns. Propagation delays are measured with a single output switching.

Note 7: t_{SKEW} is an absolute value defined as differences seen in propagation delays between drivers in the same package with identical load conditions.

Note 8: The parameter is tested using TDR techniques described in 1194.0 BTL backplane Design Guide.

Note 9: This parameter is tested during device characterization. The measurement revealed that the part will reject 1 ns pulse widths.

Note 10: Futurebus+ transceivers are required to limit bus signal rise and fall times to no faster than 0.5 V/ns, measured between 1.3V and 1.8V (approximately 20% to 80% of nominal voltage swing). The rise and fall times are measured with a transceiver loading equivalent to 12.5Ω tied to +2.1V DC.

Pin Description

Pin Name	Number of Pins	Input/ Output	Description
A0–A8	9	I/O	TTL TRI-STATE receiver output and driver input
B0–B8	9	I/O	BTL receiver input and driver output
B0GND–B8GND	9	NA	Parallel driver grounds reduce ground bounce due to high current switching of driver outputs. (Note 11)
CD	1	I	Chip Disable
GND	2	NA	Ground for switching circuits. (Note 11)
LI	1	NA	Power supply for live insertion. Boards that require live insertion should connect LI to the live insertion pin on the connector. (Note 12)
NC	8	NA	No Connect
QGND	1	NA	Ground for receiver input bandgap reference and non-switching circuits. (Note 11)
QV_{CC}	1	NA	V_{CC} supply for bandgap reference and non-switching circuits. (Note 12)
T/$\overline{R}$	1	I	Transmit/$\overline{\text{Receive}}$—transmit (An to Bn), receive (Bn to An)
V_{CC}	2	NA	V_{CC} supply for switching circuits. (Note 12)

Note 11: The multiplicity of parallel ground paths reduces the effective inductance of bonding wires and leads, which then reduces the noise caused by transients on the ground path. The various ground pins can be tied together provided that the external ground has low inductance. (i.e., ground plane with power pins and many signal pins connected to the backplane ground.) If the external ground floats considerably during transients, precautionary steps should be taken to prevent QGND from moving with reference to the backplane ground. The receiver threshold should have the same ground reference as the signal coming from the backplane. A voltage offset between their grounds will degrade the noise margin.

Note 12: The same considerations for ground are used for V_{CC} in reducing lead inductance (see Note 11). QV_{CC} and V_{CC} should be tied together externally. If live insertion is not supported, the LI pin can be tied together with QV_{CC} and V_{CC}.

Truth Table

CD	T/$\overline{R}$	An	Bn (BTL)
H	X	Z	H
L	L	L	H
L	L	H	L
L	H	H	L
L	H	L	H

X = High or low logic state

Z = High impedance state

L = Low state

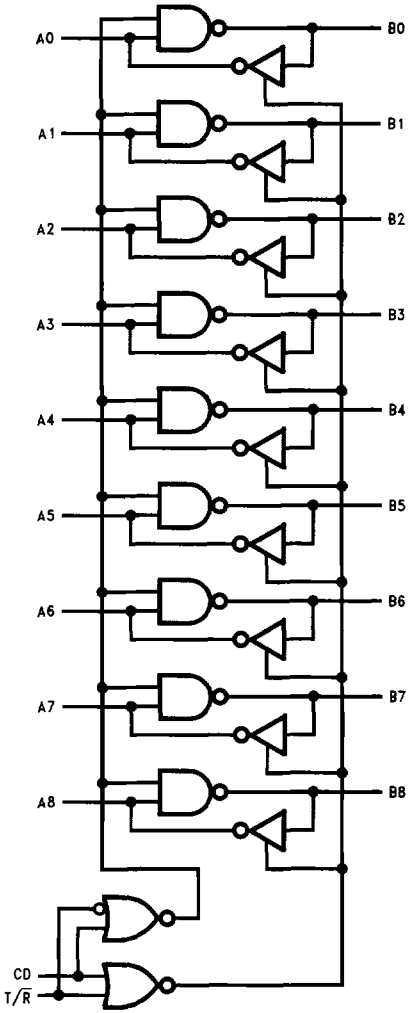
H = High state

Package Thermal Characteristics

Linear Feet per Minute Air Flow (LFPM)	θ_{JA} (°C/W)		
	44-Pin PQFP	48-Pin PQFP	44-Pin PLCC
0	82	76	45
225	68	60	35
500	60	54	30
900	53	48	26

Note: The above values are typical values and are different from the Absolute Maximum Rating values, which include guardbands.

Logic Diagram



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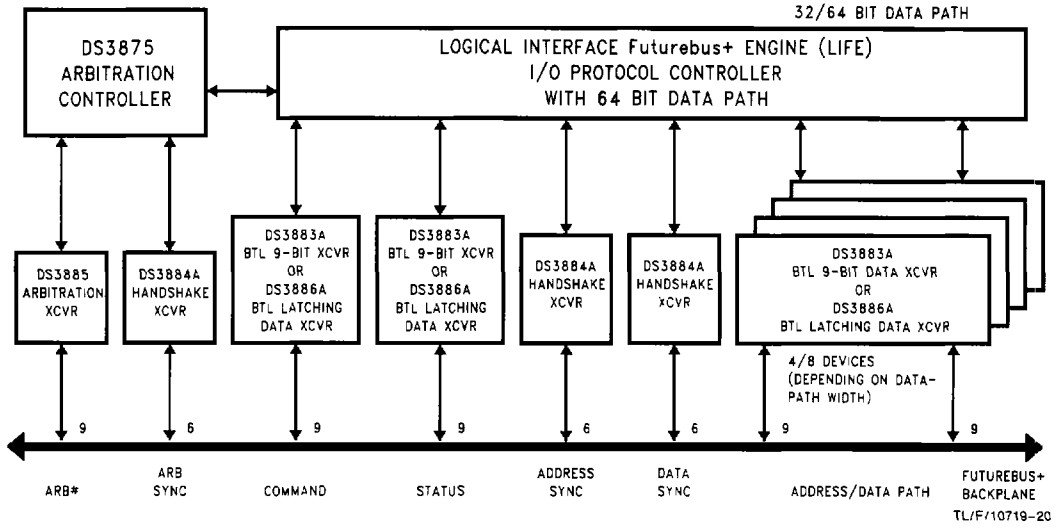
Typical Application



Test Circuit and Timing Waveforms

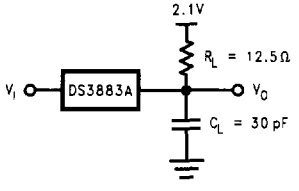


FIGURE 1. Driver Propagation Delay Set-Up

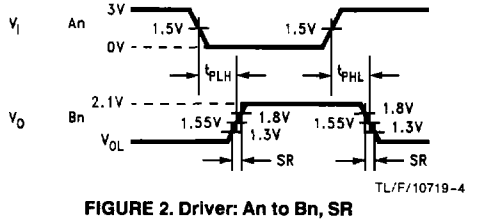


FIGURE 2. Driver: An to Bn, SR

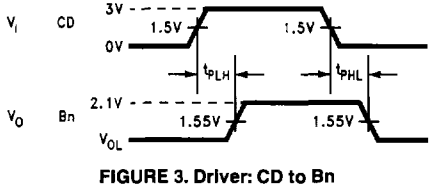
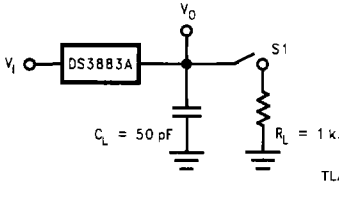


FIGURE 3. Driver: CD to Bn



Switch Position

	t_{PLH}	t_{PHL}
S1	Open	Close

FIGURE 4. Receiver Propagation Delay Set-Up

Test Circuit and Timing Waveforms (Continued)

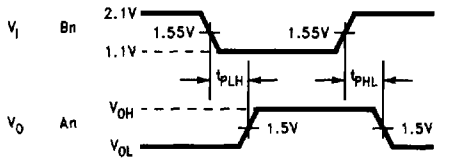


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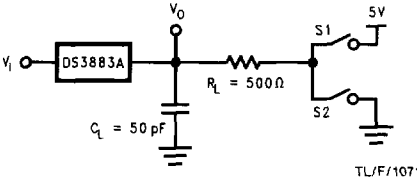
FIGURE 5. Receiver: Bn to An



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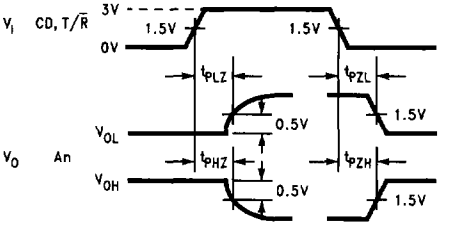
Switch Position

	t_{PZL} t_{PLZ}	t_{PZH} t_{PHZ}
S1	Close	Open
S2	Open	Close

FIGURE 6. Receiver Enable/Disable Set-Up



TL/F/10719–9

FIGURE 7. Receiver: CD to An, $T/\overline{R}$ to An (t_{PHZ} and t_{PZH} only)

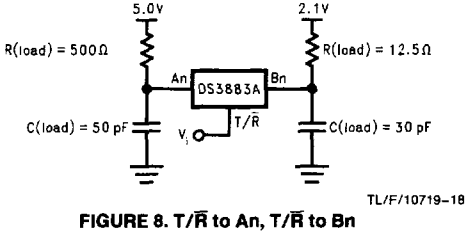


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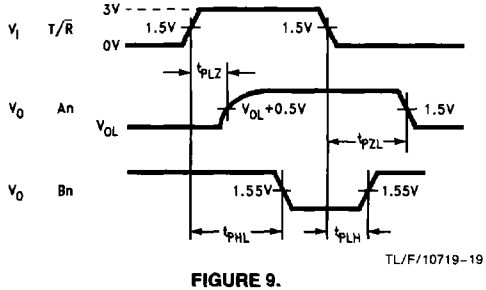
FIGURE 8. $T/\overline{R}$ to An, $T/\overline{R}$ to Bn



TL/F/10719–19

FIGURE 9.
$T/\overline{R}$ to Bn (t_{PHL} and t_{PLH} only),
$T/\overline{R}$ to An (t_{PZL} and t_{PLZ} only)

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