1. DESCRIPTION

The XD3140 and XL3140 are integrated circuit operational amplifiers that combine the advantages of high voltage PMOS transistors with high voltage bipolar transistors on a single monolithic chip.

The XD3140 and XL3140 BiMOS operational amplifiers feature gate protected MOSFET (PMOS) transistors in the input circuit to provide very high input impedance, very low input current, and high speed performance. The XD3140 and XL3140 operate at supply voltage from 4V to 36V (either single or dual supply). These operational amplifiers are internally phase compensated to achieve stable operation in unity gain follower operation, and additionally, have access terminal for a supplementary external capacitor if additional frequency roll-off is desired. Terminals are also provided for use in applications requiring input offset voltage nulling. The use of PMOS field effect transistors in the input stage results in common mode input voltage capability down to 0.5V below the negative supply terminal, an important attribute for single supply applications. The output stage uses bipolar transistors and includes built-in protection against damage from load terminal short circuiting to either supply rail or to ground.

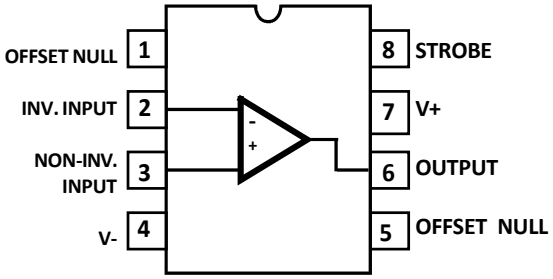
The XD3140 and XL3140 are intended for operation at supply voltages up to 36V (± 18V).

2. FEATURES

- MOSFET Input Stage
  - Very High Input Impedance (ZIN) -1.5TΩ (Typ)
  - Very Low Input Current (I_I) -10pA (Typ) at ±15V
  - Wide Common Mode Input Voltage Range (V_{ICR}) - Can be Swung 0.5V Below Negative Supply Voltage Rail
  - Output Swing Complements Input Common Mode Range
- Directly Replaces Industry Type 741 in Most Applications

3. PIN CONFIGURATIONS AND FUNCTIONS

XL3140
XD3140

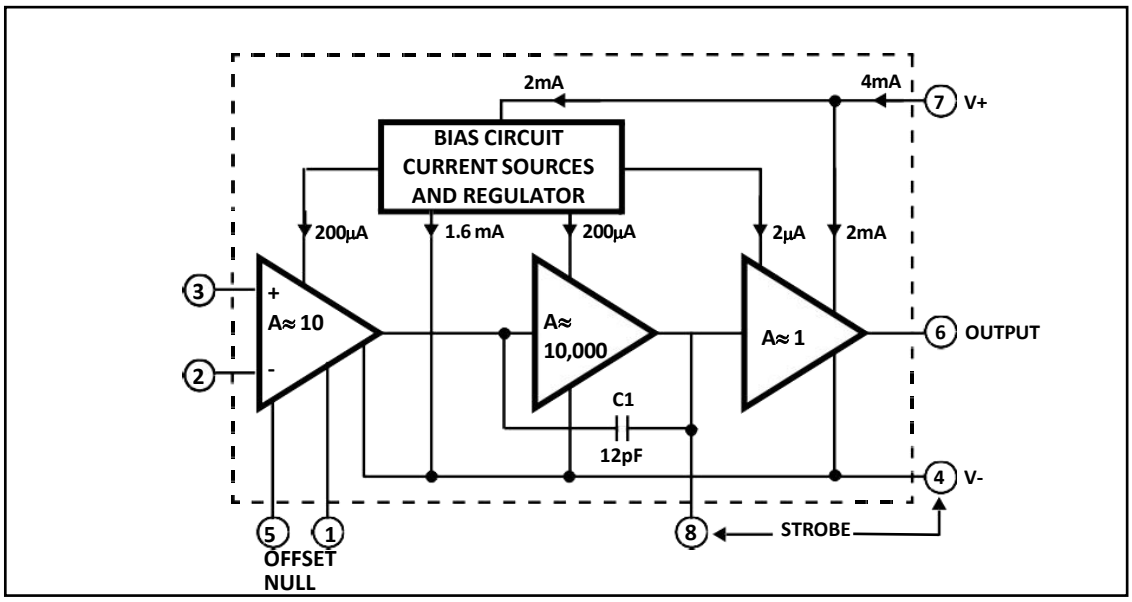


(Top View)

Pin Functions

Pin	SYMBOL	Description
1	OFFSET NULL	Used to adjust offset error
2	INV. INPUT	Inverting pin of the op-amp
3	NON-INV. INPUT	Non-inverting pin of op-amp
4	V-	Ground
5	OFFSET NULL	Used to adjust offset error
6	OUTPUT	Output Pin
7	V+	Voltage Supply
8	STROBE	This pin is employed for phase compensation or to turn off the output stage.

4. BLOCK DIAGRAM



5. SPECIFICATIONS

5.1. Absolute Maximum Ratings

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
V_{CC}	DC Supply Voltage	Between V+ and V- Terminals	-	36	V
V_{IN}	Differential Mode Input Voltage		-	8	V
V_{DC}	DC Input Voltage		V- -0.5	V+ +8	V
I_{IK}	Input Terminal Current		-	1	mA
I_{OK}	Output Short Circuit Duration∞ (Note 2)	Indefinite Operating Conditions	-	-20	mA
Ttg	Temperature Range		-40	80	℃

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

[1] θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air.

[2] Short circuit may be applied to ground or to either supply.

5.2. Thermal Resistance Characteristics

Thermal Resistance	θ_{JA}(Typical)	θ_{JC}	UNIT
DIP Package (XD3140)	115	N/A	℃/W
SOP Package (XL3140)	165	N/A	
Maximum Junction Temperature		150	
Maximum Storage Temperature Range		-45 to 125	
Maximum Lead Temperature (Soldering 10s)		300	

5.3. Electrical Characteristics

V_{SUPPLY} = ±15V, TA = 25℃ for XL3140, XD3140.

PARAMETER	SYMBOL	TEST CONDITIONS		TYPICAL VALUES	UNITS
Input Offset Voltage Adjustment Resistor		Typical Value of Resistor Between Terminals 4 and 5 or 4 and 1 to Adjust Max V_{IO}		4.7	kΩ
Input Resistance	R_I			1.5	TΩ
Input Capacitance	C_I			4	pF
Output Resistance	R_O			60	Ω
Equivalent Wideband Input Noise Voltage (See Figure 25)	e_N	BW = 140kHz, R_S = 1MΩ		48	μV
Equivalent Input Noise Voltage (See Figure 33)	e_N	R_S = 100Ω	f = 1kHz	40	$nV/\sqrt{Hz}$
			f = 10kHz	12	$nV/\sqrt{Hz}$
Short Circuit Current to Opposite Supply	I_{OM^+}		Source	40	mA
	I_{OM^-}		Sink	18	mA
Gain-Bandwidth Product, (See Figures 6, 28)	f_T			4.5	MHz
Slew Rate, (See Figure 29)	SR			9	V/μs
Sink Current From Terminal 8 To Terminal 4 to Swing Output Low				220	μA
Transient Response (See Figure 26)	t_r	R_L = 2kΩ C_L = 100pF	Rise Time	0.08	μs
	OS		Overshoot	10	%
Settling Time at $10V_{P-P}$, (See Figure 5)	t_S	R_L = 2kΩ C_L = 100pF Voltage Follower	To 1mV	4.5	μs
			To 10mV	1.4	μs

Electrical Specifications

For Equipment Design, at VSUPPLY = ±15V, TA = 25℃, Unless Otherwise Specified.

PARAMETER	SYMBOL	XL3140, XD3140			UNITS
		MIN	TYP	MAX	
Input Offset Voltage	$\|V_{IO}\|$	-	5	15	mV
Input Offset Current	$\|I_{IO}\|$	-	0.5	30	pA
Input Current	I_I	-	10	50	pA
Large Signal Voltage Gain (Note 3) (See Figures 6, 27)	A_{OL}	20 86	100 100	- -	kV/V dB
Common Mode Rejection Ratio (See Figure 32)	CMRR	-	32	320	μV/V
		70	90	-	dB
Common Mode Input Voltage Range (See Figure 8)	V_{ICR}	-15	-15.5 to +12.5	11	V
Power-Supply Rejection Ratio, $\Delta V_{IO}/\Delta V_S$ (See Figure 34)	PSRR	-	100	150	μV/V
		76	80	-	dB
Max Output Voltage (Note 4) (See Figures 2, 8)	$V_{OM}+$	+12	13	-	V
	$V_{OM}-$	-14	-14.4	-	V
Supply Current (See Figure 30)	I+	-	4	6	mA
Device Dissipation	P_D	-	120	180	mW
Input Offset Voltage Temperature Drift	$\Delta V_{IO}/\Delta T$	-	8	-	μV/°C

NOTES:

[3] At V_O = 26V_{P-P}, +12V, -14V and RL = 2kΩ.

[4] At R_L = 2k

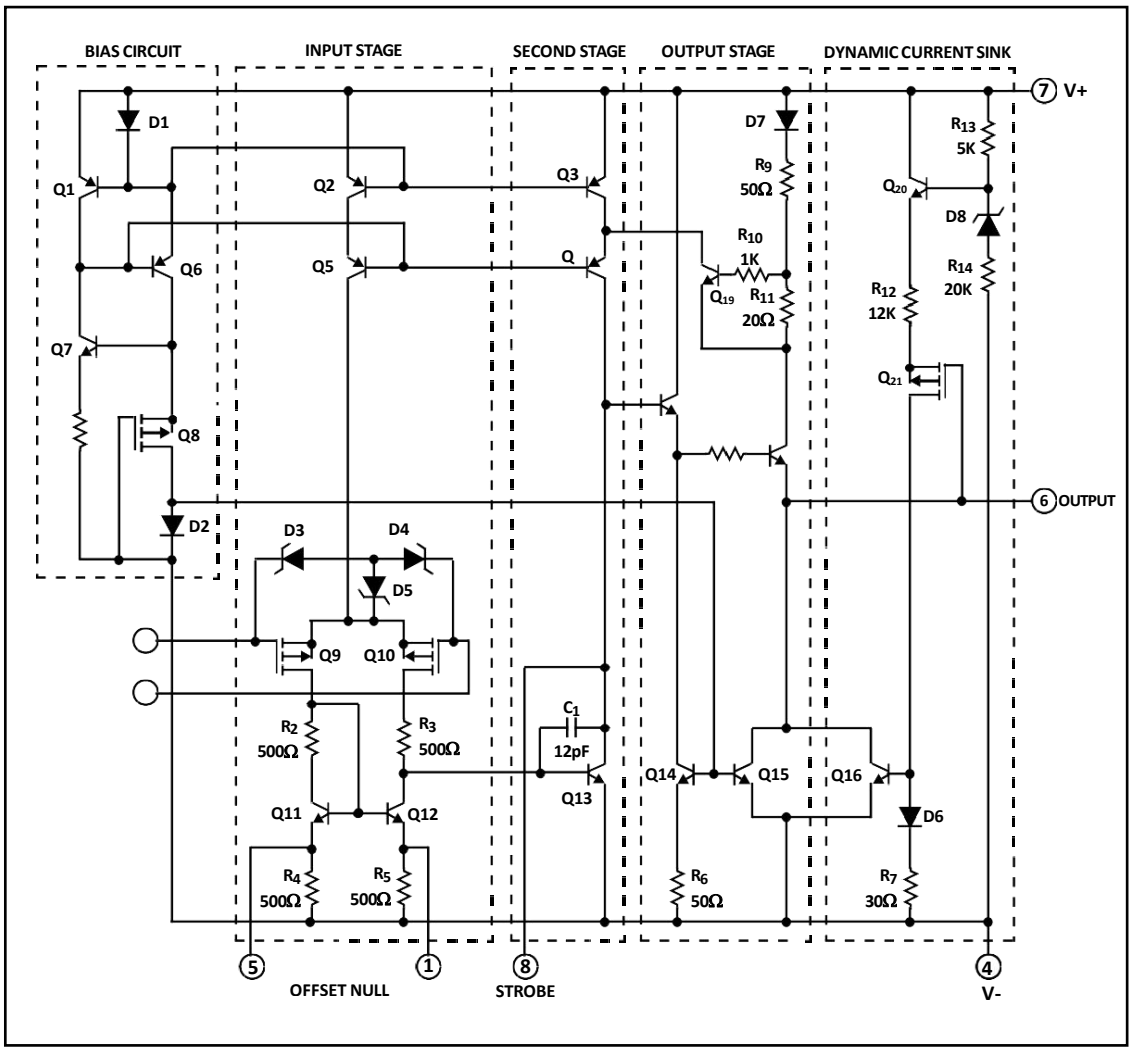
Electrical Specifications

For Design Guidance At V+ = 5V, V- = 0V, TA = 25℃ for XL3140, XD3140.

PARAMETER		SYMBOL	TYPICAL VALUES	UNITS
Input Offset Voltage		$\|V_{IO}\|$	5	mV
Input Offset Current		$\|I_{IO}\|$	0.1	pA
Input Current		I_I	2	pA
Input Resistance		R_I	1	TΩ
Large Signal Voltage Gain (See Figures 6, 27)		A_{OL}	100	kV/V
			100	dB
Common Mode Rejection Ratio		CMRR	32	μV/V
			90	dB
Common Mode Input Voltage Range (See Figure 8)		V_{ICR}	-0.5	V
			2.6	V
Power Supply Rejection Ratio		PSRR $\Delta V_{IO}/\Delta V_S$	100	μV/V
			80	dB
Maximum Output Voltage (See Figures 2, 8)		$V_{OM}+$	3	V
		$V_{OM}-$	0.13	V
Maximum Output Current:	Source	$I_{OM}+$	10	mA
	Sink	$I_{OM}-$	1	mA
Slew Rate (See Figure 29)		SR	7	V/μs
Gain-Bandwidth Product (See Figure 28)		f_T	3.7	MHz
Supply Current (See Figure 30)		I+	1.6	mA
Device Dissipation		P_D	8	mW
Sink Current from Terminal 8 to Terminal 4 to Swing Output Low			200	μA

6. Application Information

6.1. Circuit Description



As shown in the block diagram, the input terminals may be operated down to 0.5V below the negative supply rail. Two class A amplifier stages provide the voltage gain, and a unique class AB amplifier stage provides the current gain necessary to drive low-impedance loads.

A biasing circuit provides control of cascoded constant current flow circuits in the first and second stages. The XL/XD3140 includes an on chip phase compensating capacitor that is sufficient for the unity gain voltage follower configuration.

6.1.1. Input Stage

The schematic diagram consists of a differential input stage using PMOS field-effect transistors (Q9, Q10) working into a mirror pair of bipolar transistors (Q11, Q12) functioning as load resistors together with resistors R2 through R5. The mirror pair transistors also function as a differential-to-single-ended converter to provide base current drive to the second stage bipolar transistor (Q13). Offset nulling, when desired, can be effected with a 10kΩ potentiometer connected across Terminals 1 and 5 and with its slider arm connected to Terminal 4. Cascode-connected bipolar transistors Q2, Q5 are the constant current source for the input stage. The base biasing circuit for the constant current source is described subsequently. The small diodes D3, D4, D5 provide gate oxide protection against high voltage transients, e.g., static electricity.

6.1.2. Second Stage

Most of the voltage gain in the XL/XD3140 is provided by the second amplifier stage, consisting of bipolar transistor Q13 and its cascode connected load resistance provided by bipolar transistors Q3, Q4. On-chip phase compensation, sufficient for a majority of the applications is provided by C1. Additional Miller-Effect compensation (roll off) can be accomplished, when desired, by simply connecting a small capacitor between Terminals 1 and 8. Terminal 8 is also used to strobe the output stage into quiescence. When terminal 8 is tied to the negative supply rail (Terminal 4) by mechanical or electrical means, the output Terminal 6 swings low, i.e., approximately to Terminal 4 potential.

6.1.3. Output Stage

The XL/XD3140 circuits employ a broad band output stage that can sink loads to the negative supply to complement the capability of the PMOS input stage when operating near the negative rail. Quiescent current in the emitter-follower cascade circuit (Q17, Q18) is established by transistors (Q14, Q15) whose base currents are “mirrored” to current flowing through diode D2 in the bias circuit section. When the XL/XD3140 is operating such that output Terminal 6 is sourcing current, transistor Q18 functions as an emitter-follower to source current from the V+ bus (Terminal 7), via D7, R9, and R11. Under these conditions, the collector potential of Q13 is sufficiently high to permit the necessary flow of base current to emitter follower Q17 which, in turn, drives Q18.

When the XL/XD3140 is operating such that output Terminal 6 is sinking current to the V- bus, transistor Q16 is the current sinking element. Transistor Q16 is mirror connected to D6, R7, with current fed by way of Q21, R12, and Q20. Transistor Q20, in turn, is biased by current flow through R13, zener D8, and R14. The dynamic current sink is controlled by voltage level sensing. For purposes of explanation, it is assumed that output Terminal 6 is quiescently established at the potential midpoint between the V+ and V- supply rails. When output current sinking mode operation is required, the collector potential of transistor Q13 is driven below its quiescent level, thereby causing Q17, Q18 to decrease the output voltage at Terminal 6. Thus, the gate terminal of PMOS transistor Q21 is displaced toward the V- bus, thereby reducing the channel resistance of Q21. As a consequence, there is an incremental increase in current flow through Q20, R12, Q21, D6, R7, and the base of Q16. As a result, Q16 sinks current from Terminal 6 in direct response to the incremental change in output voltage caused by Q18.

This sink current flows regardless of load; any excess current is internally supplied by the emitter-follower Q18. Short circuit protection of the output circuit is provided by Q19, which is driven into conduction by the high voltage drop developed across R11 under output short circuit conditions. Under these conditions, the collector of Q19 diverts current from Q4 so as to reduce the base current drive from Q17, thereby limiting current flow in Q18 to the short circuited load terminal.

6.1.4. Bias Circuit

Quiescent current in all stages (except the dynamic current sink) of the XL/XD3140 is dependent upon bias current flow in R1. The function of the bias circuit is to establish and maintain constant current flow through D1, Q6, Q8 and D2. D1 is a diode connected transistor mirror connected in parallel with the base emitter junctions of Q1, Q2, and Q3. D1 may be considered as a current sampling diode that senses the emitter current of Q6 and automatically adjusts the base current of Q6 (via Q1) to maintain a constant current through Q6, Q8, D2. The base currents in Q2, Q3 are also determined by constant current flow D1. Furthermore, current in diode connected transistor Q2 establishes the currents in transistors Q14 and Q15.

6.1.5. Typical Applications

Wide dynamic range of input and output characteristics with the most desirable high input impedance characteristics is achieved in the XL/XD3140 by the use of an unique design based upon the PMOS Bipolar process. Input common mode voltage range and output swing capabilities are complementary, allowing operation with the single supply down to 4V.

The wide dynamic range of these parameters also means that this device is suitable for many single supply applications, such as, for example, where one input is driven below the potential of Terminal 4 and the phase sense of the output signal must be maintained – a most important consideration in comparator applications.

6.1.6. Output Circuit Considerations

Excellent interfacing with TTL circuitry is easily achieved with a single 6.2V zener diode connected to Terminal 8 as shown in Figure 1. This connection assures that the maximum output signal swing will not go more positive than the zener voltage minus two base-to-emitter voltage drops within the XL/XD3140. These voltages are independent of the operating supply voltage.

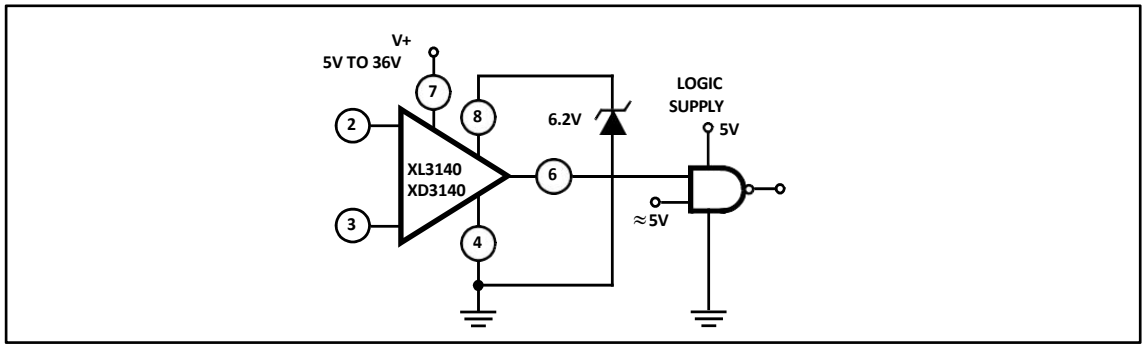


FIGURE 1. ZENER CLAMPING DIODE CONNECTED TO TERMINALS 8 AND 4 TO LIMIT XL/XD3140 OUTPUT SWING TO TTL LEVELS

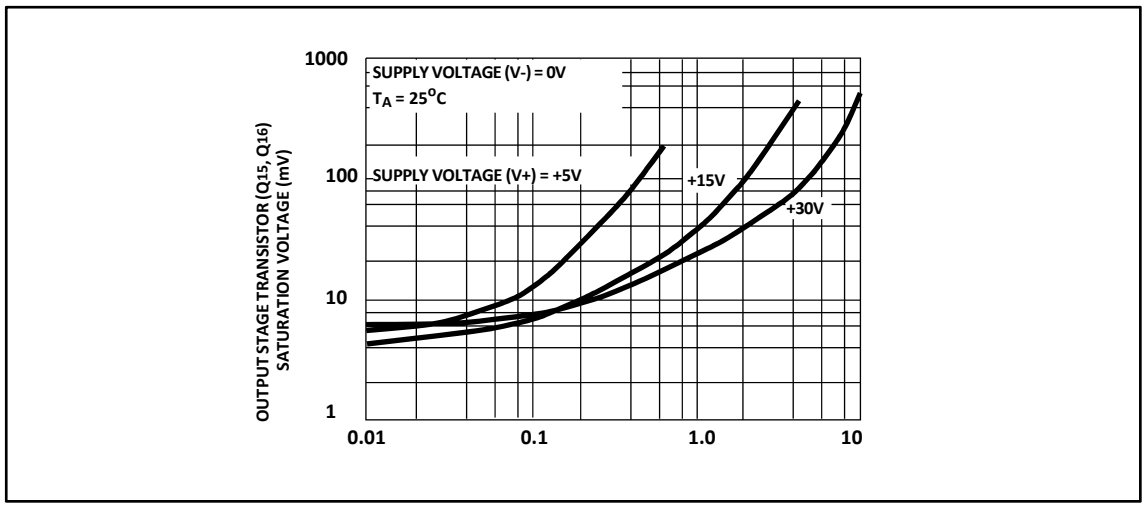


FIGURE 2. VOLTAGE ACROSS OUTPUT TRANSISTORS (Q15 AND Q16) vs LOAD CURRENT

Figure 2 shows output current sinking capabilities of the XL/XD3140 at various supply voltages. Output voltage swing to the negative supply rail permits this device to operate both power transistors and thyristors directly without the need for level shifting circuitry usually associated with the 741 series of operational amplifiers.

Figure 4 shows some typical configurations. Note that a series resistor, RL, is used in both cases to limit the drive available to the driven device. Moreover, it is recommended that a series diode and shunt diode be used at the thyristor input to prevent large negative transient surges that can appear at the gate of thyristors, from damaging the integrated circuit.

6.2. Offset Voltage Nulling

The input offset voltage can be nulled by connecting a 10k potentiometer between Terminals 1 and 5 and returning its wiper arm to terminal 4, see Figure 3A. This technique, however, gives more adjustment range than required and therefore, a considerable portion of the potentiometer rotation is not fully utilized. Typical values of series resistors (R) that may be placed at either end of the potentiometer, see Figure 3B, to optimize its utilization range are given in the Electrical Specifications table.

An alternate system is shown in Figure 3C. This circuit uses only one additional resistor of approximately the value shown in the table. For potentiometers, in which the resistance does not drop to 0Ω at either end of rotation, a value of resistance 10% lower than the values shown in the table should be used.

6.3. Low Voltage Operation

Operation at total supply voltages as low as 4V is possible with the XL/XD3140. A current regulator based upon the PMOS threshold voltage maintains reasonable constant operating current and hence consistent performance down to these lower voltages.

The low voltage limitation occurs when the upper extreme of the input common mode voltage range extends down to the voltage at Terminal 4. This limit is reached at a total supply voltage just below 4V. The output voltage range also begins to extend down to the negative supply rail, but is slightly higher than that of the input. Figure 8 shows these characteristics and shows that with 2V dual supplies, the lower extreme of the input common mode voltage range is below ground potential.

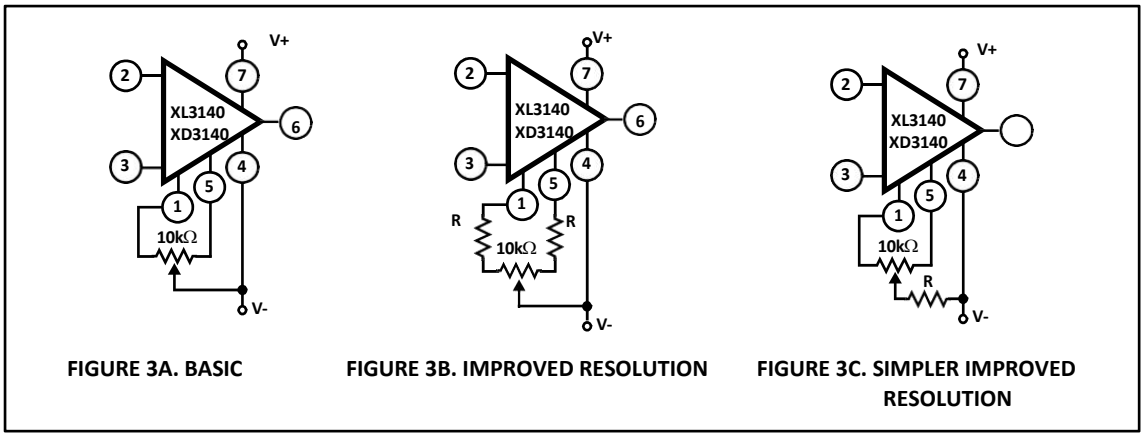


FIGURE 3A. BASIC FIGURE 3B. IMPROVED RESOLUTION FIGURE 3C. SIMPLER IMPROVED RESOLUTION

FIGURE 3. THREE OFFSET VOLTAGE NULLING METHODS

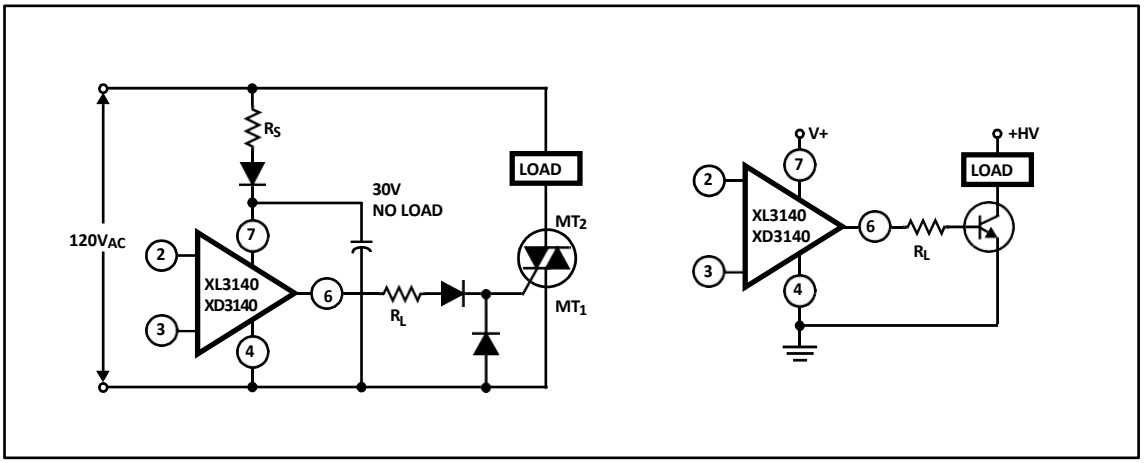


FIGURE 4. METHODS OF UTILIZING THE VCE(SAT) SINKING CURRENT CAPABILITY OF THE XL/XD3140 SERIES

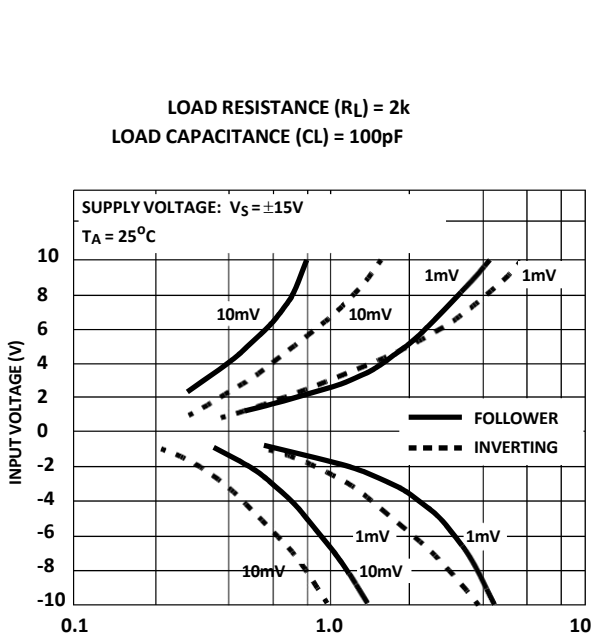


FIGURE 5A. WAVEFORM

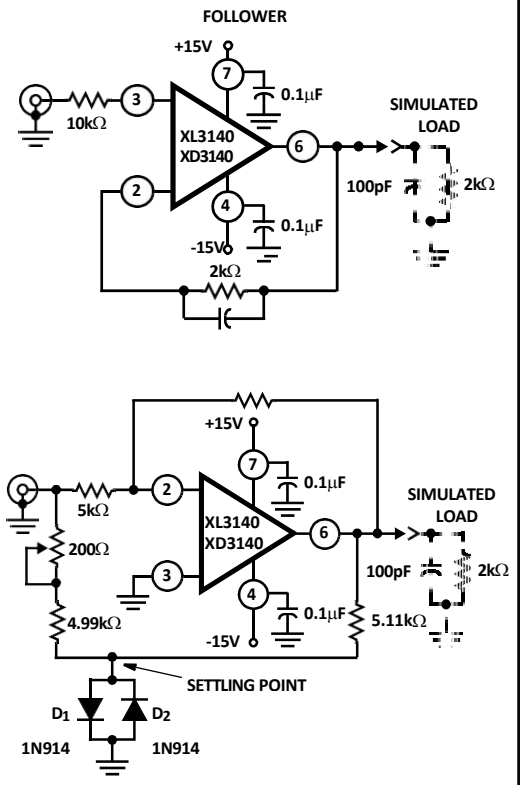


FIGURE 5B. TEST CIRCUITS

FIGURE 5. SETTLING TIME vs INPUT VOLTAGE

6.4. Bandwidth and Slew Rate

For those cases where bandwidth reduction is desired, for example, broadband noise reduction, an external capacitor connected between Terminals 1 and 8 can reduce the open loop -3dB bandwidth. The slew rate will, however, also be proportionally reduced by using this additional capacitor.

Thus, a 20% reduction in bandwidth by this technique will also reduce the slew rate by about 20%.

Figure 5 shows the typical settling time required to reach 1mV or 10mV of the final value for various levels of large signal inputs for the voltage follower and inverting unity gain amplifiers.

The exceptionally fast settling time characteristics are largely due to the high combination of high gain and wide bandwidth of the XL/XD3140; as shown in Figure 6.

6.4.1. Input Circuit Considerations

As mentioned previously, the amplifier inputs can be driven below the Terminal 4 potential, but a series current limiting resistor is recommended to limit the maximum input terminal current to less than 1mA to prevent damage to the input protection circuitry.

Moreover, some current limiting resistance should be provided between the inverting input and the output when the XL/XD3140 is used as a unity gain voltage follower. This resistance prevents the possibility of extremely large input signal transients from forcing a signal through the input protection network and directly driving the internal constant current source which could result in positive feedback via the output terminal. A 3.9kΩ resistor is sufficient.

The typical input current is on the order of 10pA when the inputs are centered at nominal device dissipation. As the output supplies load current, device dissipation will increase, raising the chip temperature and resulting in increased input current. Figure 7 shows typical input terminal current versus ambient temperature for the XL/XD3140.

It is well known that MOSFET devices can exhibit slight changes in characteristics (for example, small changes in input offset voltage) due to the application of large differential input voltages that are sustained over long periods at elevated temperatures.

Both applied voltage and temperature accelerate these changes. The process is reversible and offset voltage shifts of the opposite polarity reverse the offset. Figure 9 shows the typical offset voltage change as a function of various stress voltages at the maximum rating of 125oC (for metal can); at lower temperatures (metal can and plastic), for example, at 85oC, this change in voltage is considerably less. In typical linear applications, where the differential voltage is small and symmetrical, these incremental changes are of about the same magnitude as those encountered in an operational amplifier employing a bipolar transistor input stage.

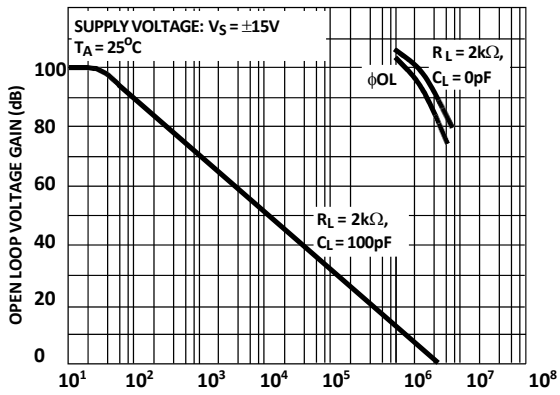


FIGURE 6. OPEN LOOP VOLTAGE GAIN AND PHASE vs FREQUENCY

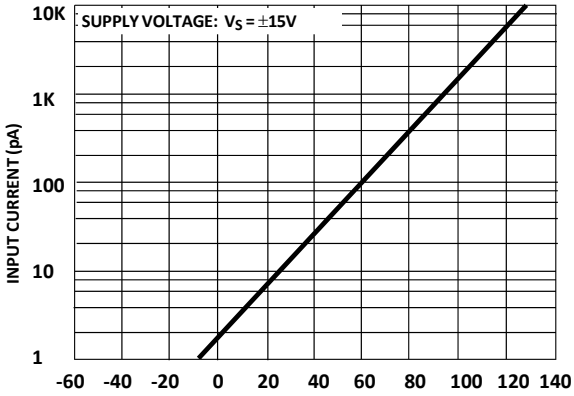


FIGURE 7. INPUT CURRENT vs TEMPERATURE

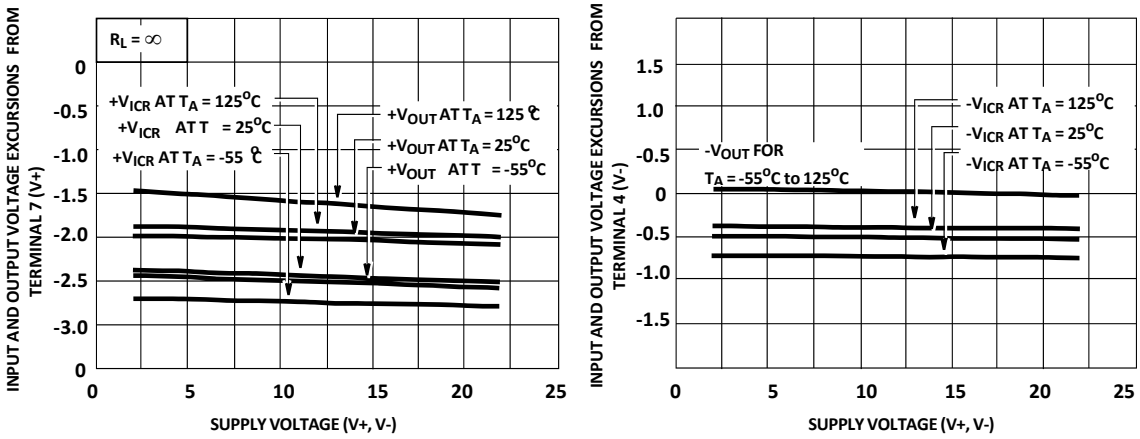


FIGURE 8. OUTPUT VOLTAGE SWING CAPABILITY AND COMMON MODE INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE

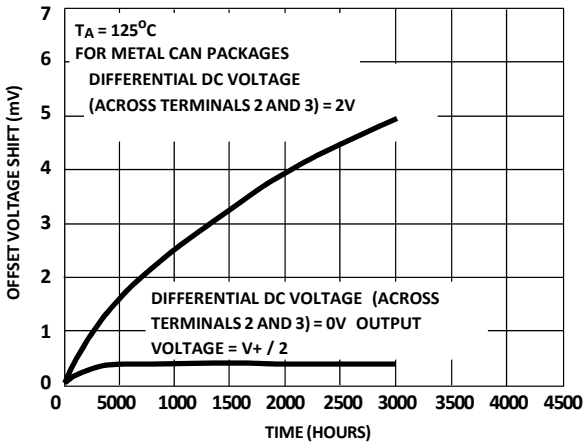
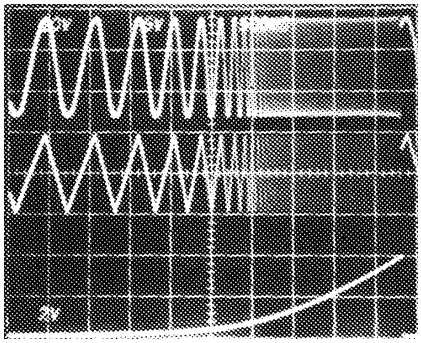


FIGURE 9. TYPICAL INCREMENTAL OFFSET VOLTAGE SHIFT vs OPERATING LIFE

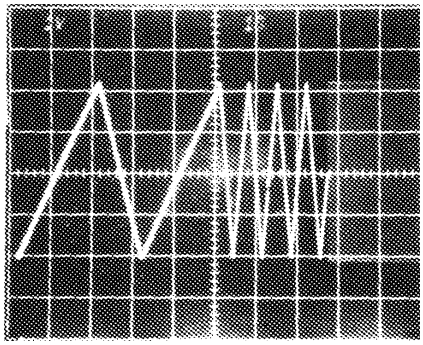


Top Trace: Output at junction of 2.7Ω and 51Ω resistors; 5V/Div., 500ms/Div.

Center Trace: External output of triangular function generator; 2V/Div., 500ms/Div.

Bottom Trace: Output of "Log" generator; 10V/Div., 500ms/Div.

FIGURE 10B. FIGURE FUNCTION GENERATOR SWEEPING



Three tone test signals, highest frequency ≥0.5MHz. Note the slight asymmetry at the three second/cycle signal.

FIGURE 10C. FUNCTION GENERATOR WITH FIXED FREQUENCIES

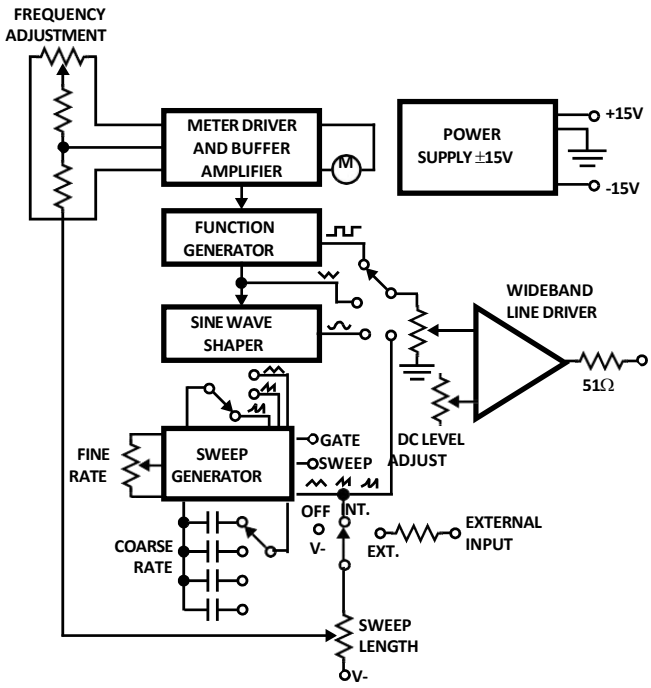


FIGURE 10D. INTERCONNECTIONS

FIGURE 10. FUNCTION GENERATOR

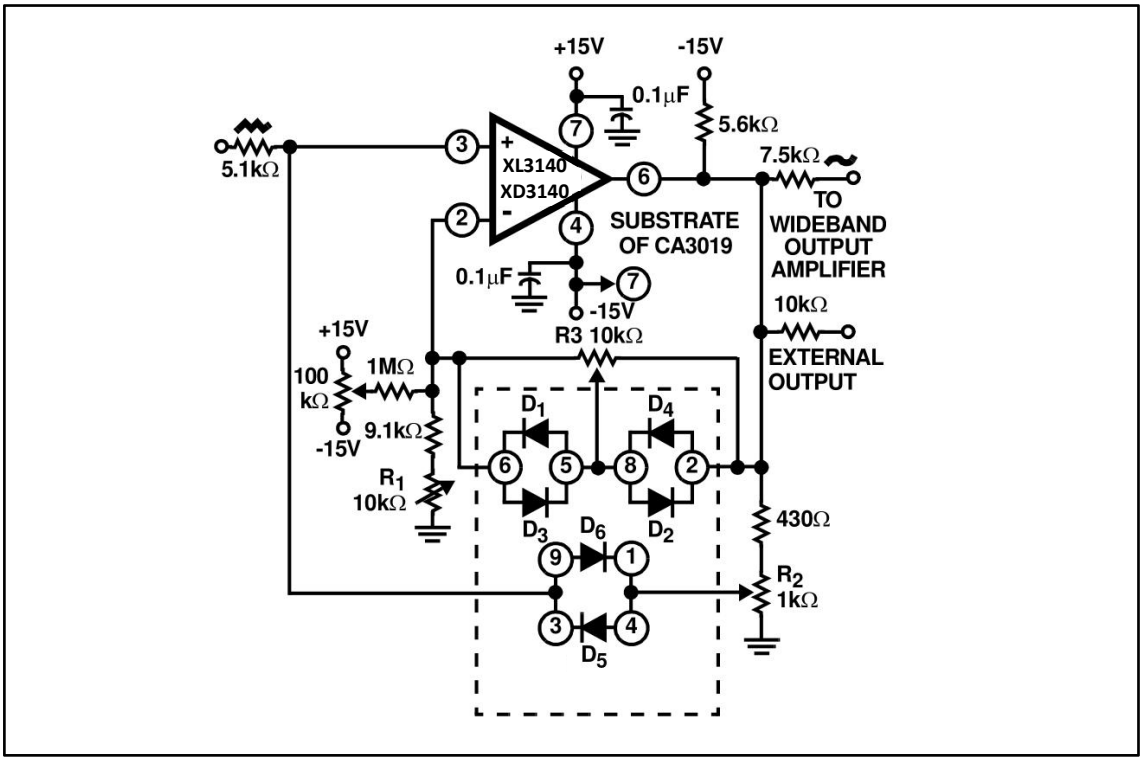


FIGURE 11. SINE WAVE SHAPER

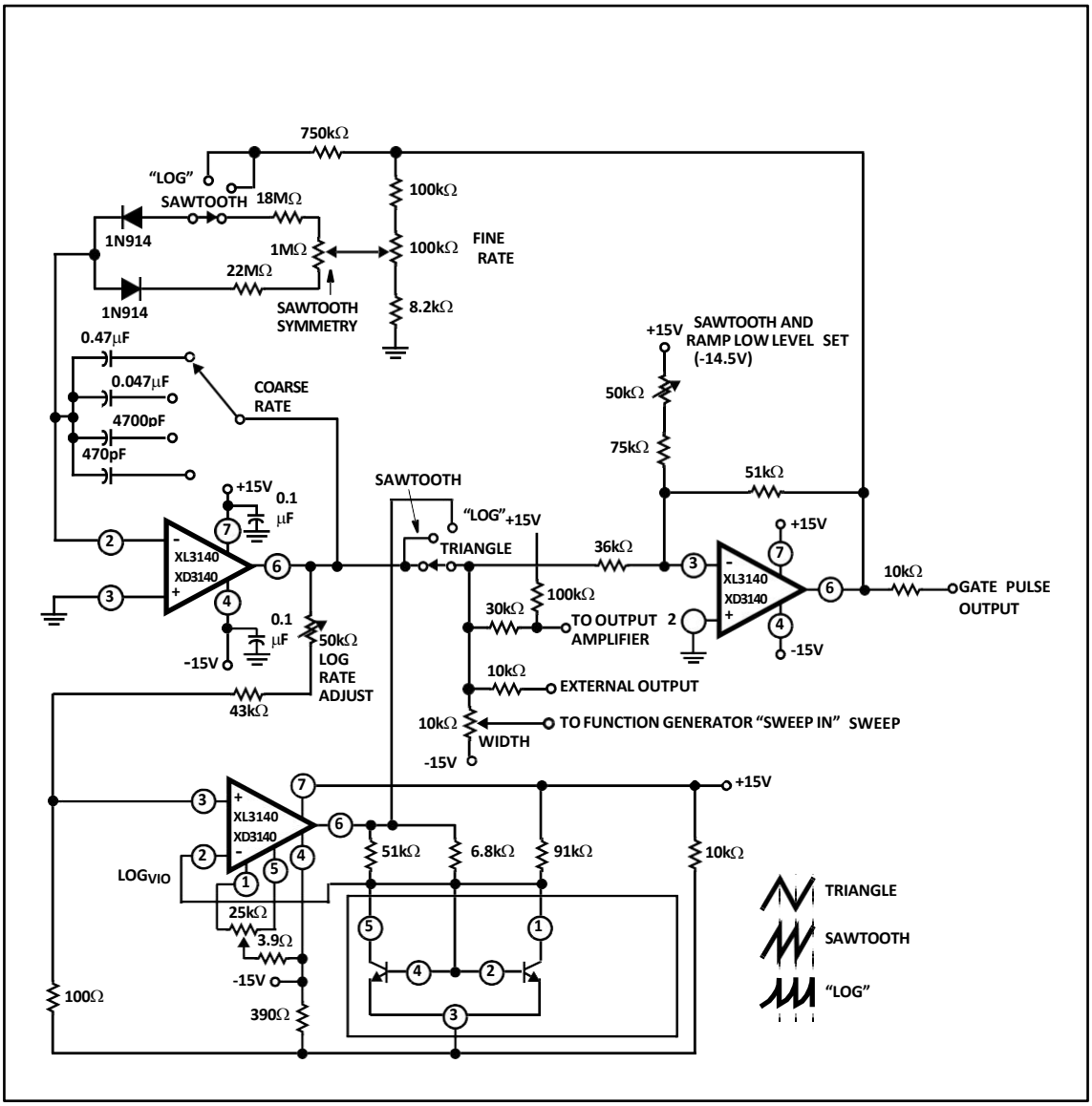


FIGURE 12. SWEEPING GENERATOR

This circuit can be adjusted most easily with a distortion analyzer, but a good first approximation can be made by comparing the output signal with that of a sine wave generator. The initial slope is adjusted with the potentiometer R1, followed by an adjustment of R2. The final slope is established by adjusting R3, thereby adding additional segments that are contributed by these diodes. Because there is some interaction among these controls, repetition of the adjustment procedure may be necessary.

6.5. Sweeping Generator

Figure 12 shows a sweeping generator. Three XL/XD3140s are used in this circuit. One XL/XD3140 is used as an integrator, a second device is used as a hysteresis switch that determines the starting and stopping points of the sweep. A third XL/XD3140 is used as a logarithmic shaping network for the log function. Rates and slopes, as well as sawtooth, triangle, and logarithmic sweeps are generated by this circuit.

6.6. Wideband Output Amplifier

Figure 13 shows a high slew rate, wideband amplifier suitable for use as a 50Ω transmission line driver. This circuit, when used in conjunction with the function generator and sine wave shaper circuits shown in Figures 10 and 11 provides 18VP-P output open circuited, or 9VP-P output when terminated in 50Ω. The slew rate required of this amplifier is 28V/μs (18VP-P x π x 0.5MHz).

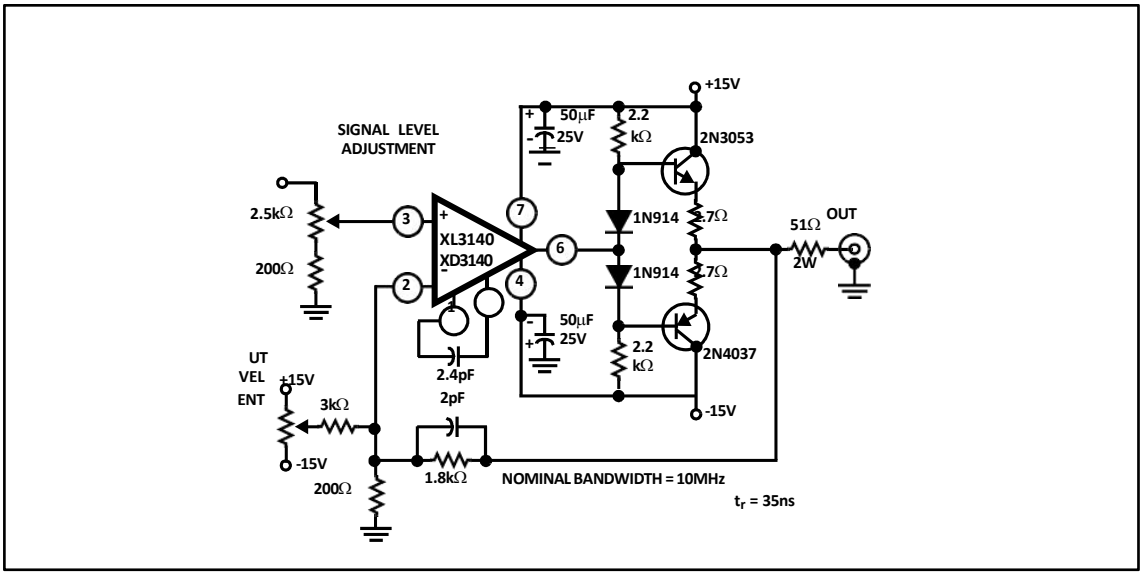


FIGURE 13. WIDEBAND OUTPUT AMPLIFIER

6.6.1. Power Supplies

High input impedance, common mode capability down to the negative supply and high output drive current capability are key factors in the design of wide range output voltage supplies that use a single input voltage to provide a regulated output voltage that can be adjusted from essentially 0V to 24V.

Unlike many regulator systems using comparators having a bipolar transistor input stage, a high impedance reference voltage divider from a single supply can be used in connection with the XL/XD3140 (see Figure 14).

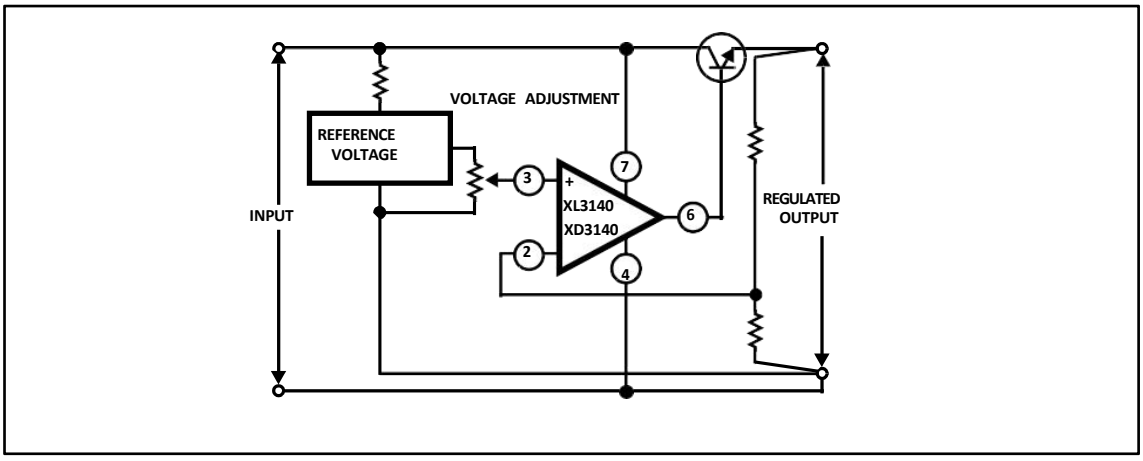


FIGURE 14. BASIC SINGLE SUPPLY VOLTAGE REGULATOR SHOWING VOLTAGE FOLLOWER CONFIGURATION

Essentially, the regulators, shown in Figures 15 and 16, are connected as non inverting power operational amplifiers with a gain of 3.2. An 8V reference input yields a maximum output voltage slightly greater than 25V. As a voltage follower, when the reference input goes to 0V the output will be 0V. Because the offset voltage is also multiplied by the 3.2 gain factor, a potentiometer is needed to null the offset voltage.

Series pass transistors with high ICBO levels will also prevent the output voltage from reaching zero because there is a finite voltage drop (VCESAT) across the output of the XL/XD3140 (see Figure 2). This saturation voltage level may indeed set the lowest voltage obtainable.

The high impedance presented by Terminal 8 is advantageous in effecting current limiting. Thus, only a small signal transistor is required for the current-limit sensing amplifier. Resistive decoupling is provided for this transistor to minimize damage to it or the XL/XD3140 in the event of unusual input or output transients on the supply rail.

Figures 15 and 16, show circuits in which a D2201 high speed diode is used for the current sensor. This diode was chosen for its slightly higher forward voltage drop characteristic, thus giving greater sensitivity. It must be emphasized that heat sinking of this diode is essential to minimize variation of the current trip point due to internal heating of the diode. That is, 1A at 1V forward drop represents one watt which can result in significant regenerative changes in the current trip point as the diode temperature rises. Placing the small signal reference amplifier in the proximity of the current sensing diode also helps minimize the variability in the trip level due to the negative temperature coefficient of the diode. In spite of those limitations, the current limiting point can easily be adjusted over the range from 10mA to 1A with a single adjustment potentiometer. If the temperature stability of the current limiting system is a serious consideration, the more usual current sampling resistor type of circuitry should be employed.

A power Darlington transistor (in a metal can with heatsink), is used as the series pass element for the conventional current limiting system, Figure 15, because high power Darlington dissipation will be encountered at low output voltage and high currents.

A small heat sink VERSAWATT transistor is used as the series pass element in the fold back current system, Figure 16, since dissipation levels will only approach 10W. In this system, the D2201 diode is used for current sampling.

Foldback is provided by the 3kΩ and 100kΩ divider network connected to the base of the current sensing transistor.

Both regulators provide better than 0.02% load regulation. Because there is constant loop gain at all voltage settings, the regulation also remains constant. Line regulation is 0.1% per volt. Hum and noise voltage is less than 200μV as read with a meter having a 10MHz bandwidth.

Figure 17A shows the turn ON and turn OFF characteristics of both regulators. The slow turn on rise is due to the slow rate of rise of the reference voltage. Figure 17B shows the transient response of the regulator with the switching of a 20Ω load at 20V output.

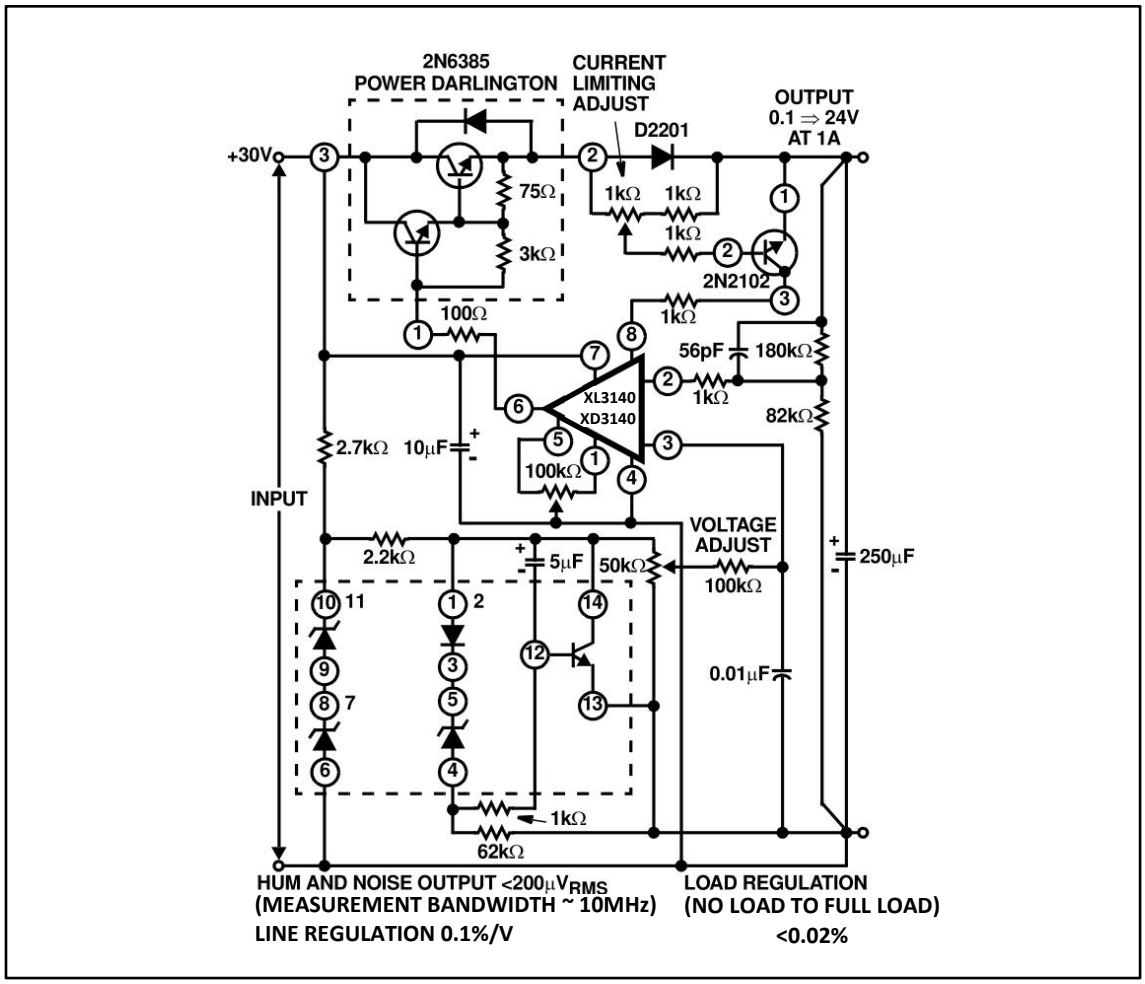


FIGURE 15. REGULATED POWER SUPPLY

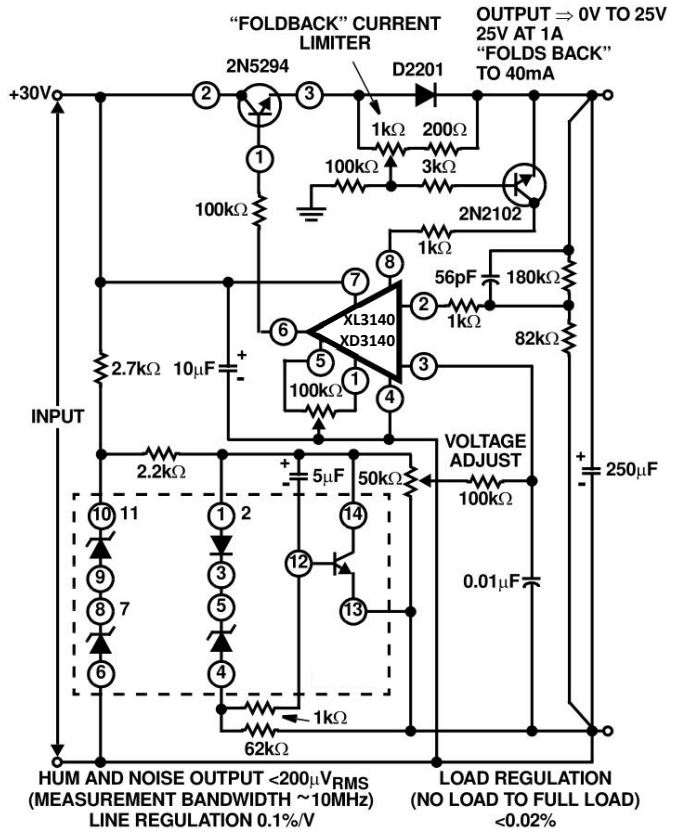
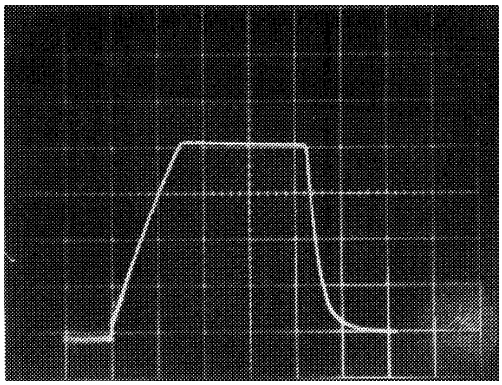
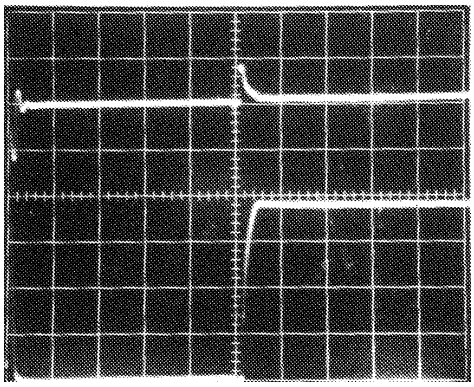


FIGURE 16. REGULATED POWER SUPPLY WITH "FOLDBACK" CURRENT LIMITING



5V/Div., 1s/Div.

FIGURE 17A. SUPPLY TURN-ON AND TURNOFF CHARACTERISTIC



Top Trace: Output Voltage;
200mV/Div., 5μs/Div.
Bottom Trace: Collector of load switching transistor,
load = 1A; 5V/Div., 5μs/Div.

FIGURE 17B. TRANSIENT RESPONSE

FIGURE 17. WAVEFORMS OF DYNAMIC CHARACTERISTICS OF POWER SUPPLY CURRENTS SHOWN IN FIGURES 15 AND 16

6.7. Tone Control Circuits

High slew rate, wide bandwidth, high output voltage capability and high input impedance are all characteristics required of tone control amplifiers. Two tone control circuits that exploit these characteristics of the XL/XD3140 are shown in Figures 18 and 19.

The first circuit, shown in Figure 20, is the Baxandall tone control circuit which provides unity gain at midband and uses standard linear potentiometers. The high input impedance of the XL/XD3140 makes possible the use of low- cost, low-value, small size capacitors, as well as reduced load of the driving stage.

Bass treble boost and cut are ±15dB at 100Hz and 10kHz, respectively. Full peak-to-peak output is available up to at least 20kHz due to the high slew rate of the XL/XD3140. The amplifier gain is 3dB down from its “flat” position at 70kHz.

Figure 18 shows another tone control circuit with similar boost and cut specifications. The wideband gain of this circuit is equal to the ultimate boost or cut plus one, which in this case is a gain of eleven. For 20dB boost and cut, the input loading of this circuit is essentially equal to the value of the resistance from Terminal No. 3 to ground. A detailed analysis of this circuit is given in “An IC Operational Transconductance Amplifier (OTA) With Power Capability” by L. Kaplan and H. Wittlinger, IEEE Transactions on Broadcast and Television Receivers, Vol. BTR-18, No. 3, August, 1972.

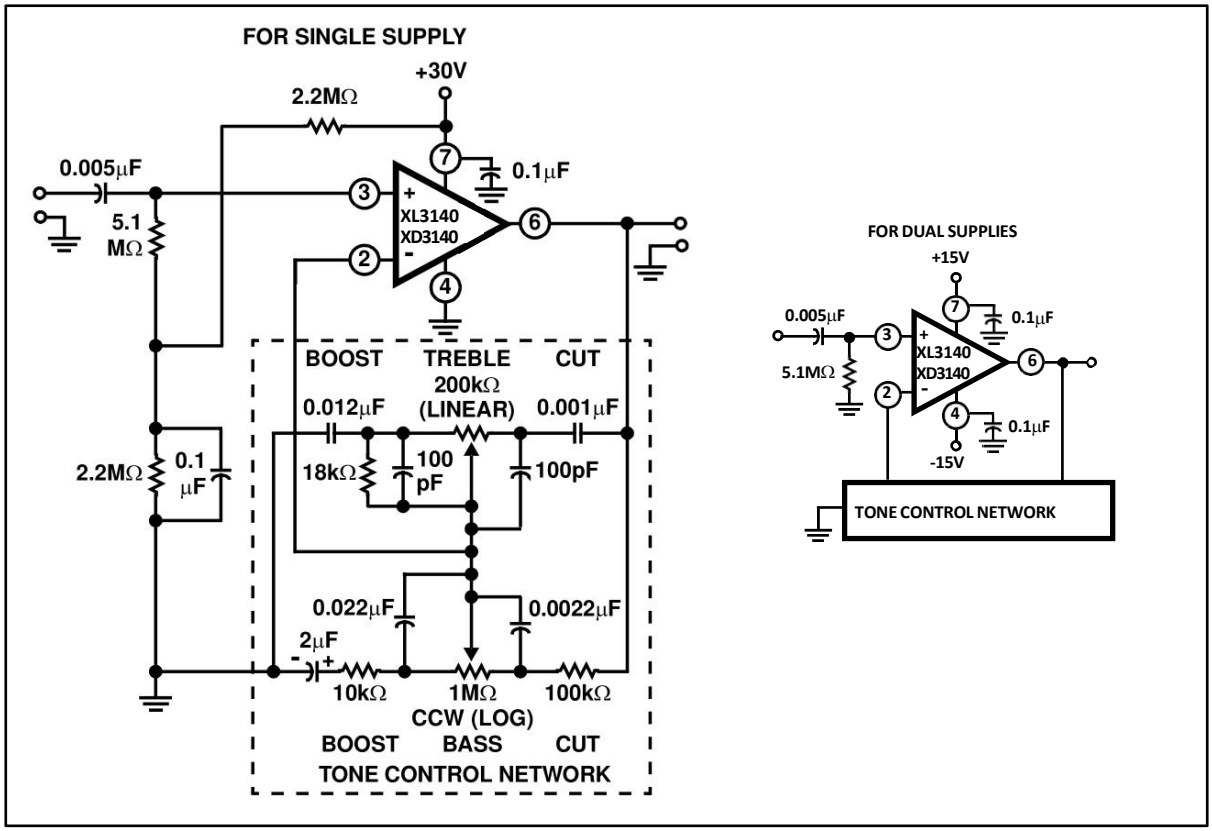


FIGURE 18. TONE CONTROL CIRCUIT (20dB MIDBAND GAIN)

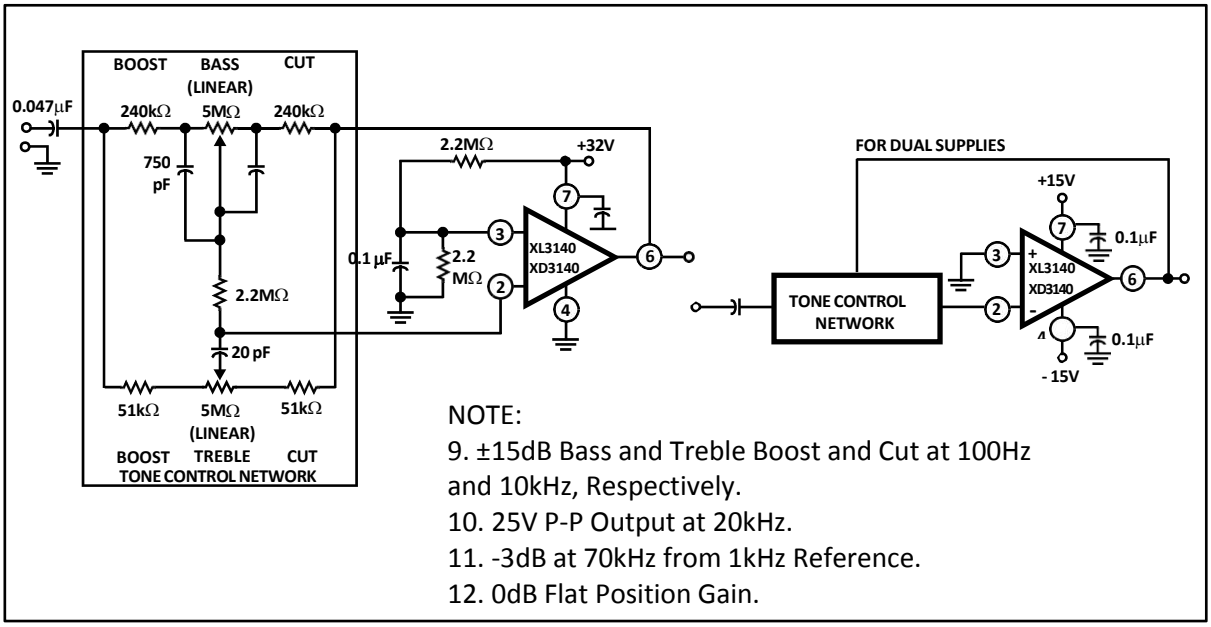


FIGURE 19. BAXANDALL TONE CONTROL CIRCUIT USING XL/XD3140

6.8. Wien Bridge Oscillator

Another application of the XL/XD3140 that makes excellent use of its high input impedance, high slew rate, and high voltage qualities is the Wien Bridge sine wave oscillator. A basic Wien Bridge oscillator is shown in Figure 20. When R1 = R2 = R and C1 = C2 = C, the frequency equation reduces to the familiar f = 1/(2πRC) and the gain required for oscillation, AOSC is equal to 3. Note that if C2 is increased by a factor of four and R2 is reduced by a factor of four, the gain required for oscillation becomes 1.5, thus permitting a potentially higher operating frequency closer to the gain bandwidth product of the XL/XD3140.

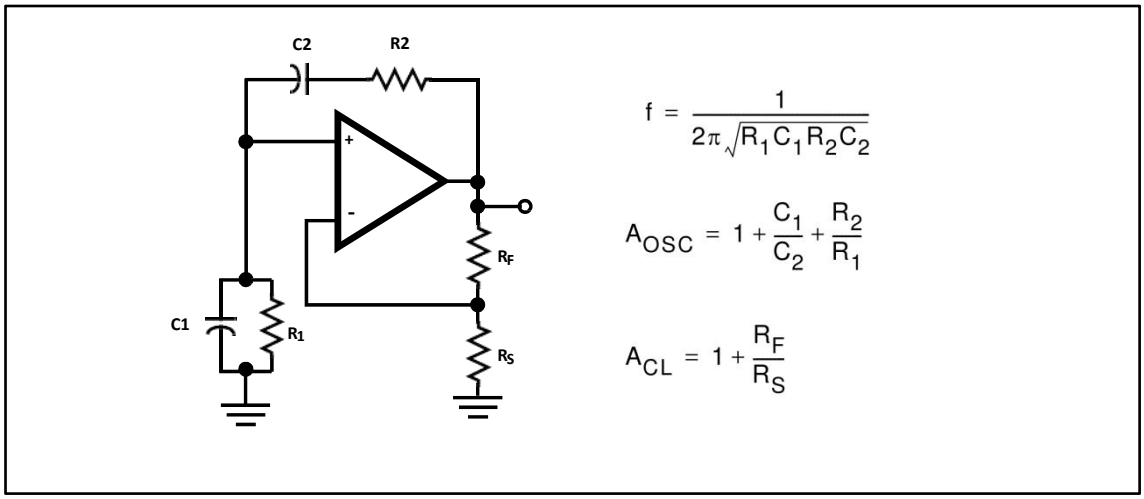


FIGURE 20. BASIC WIEN BRIDGE OSCILLATOR CIRCUIT USING AN OPERATIONAL AMPLIFIER

Oscillator stabilization takes on many forms. It must be precisely set, otherwise the amplitude will either diminish or reach some form of limiting with high levels of distortion. The element, RS , is commonly replaced with some variable resistance element. Thus, through some control means, the value of RS is adjusted to maintain constant oscillator output. A FET channel resistance, a thermistor, a lamp bulb, or other device whose resistance increases as the output amplitude is increased are a few of the elements often utilized. Figure 21 shows another means of stabilizing the oscillator with a zener diode shunting the feedback resistor (RF of Figure 20). As the output signal amplitude increases, the zener diode impedance decreases resulting in more feedback with consequent reduction in gain; thus stabilizing the amplitude of the output signal. Furthermore, this combination of a monolithic zener diode and bridge rectifier circuit tends to provide a zero temperature coefficient for this regulating system. Because this bridge rectifier system has no time constant, i.e., thermal time constant for the lamp bulb, and RC time constant for filters often used in detector networks, there is no lower frequency limit. For example, with 1μF polycarbonate capacitors and 22MΩ for the frequency determining network, the operating frequency is 0.007Hz.

As the frequency is increased, the output amplitude must be reduced to prevent the output signal from becoming slew- rate limited. An output frequency of 180kHz will reach a slew rate of approximately 9V/μs when its amplitude is 16VP-P.

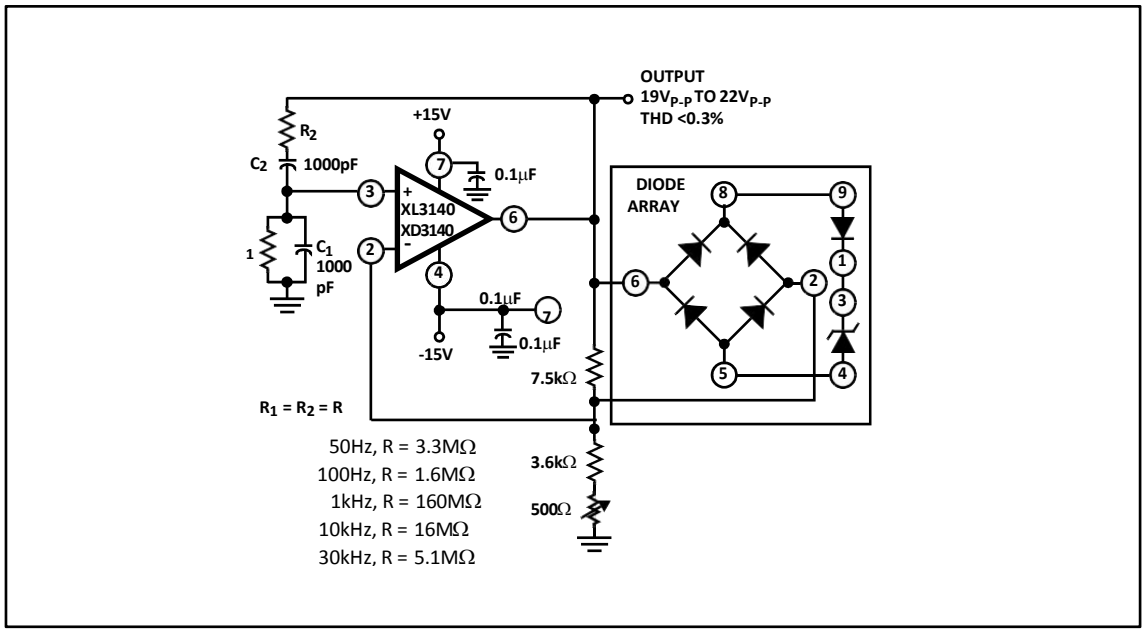
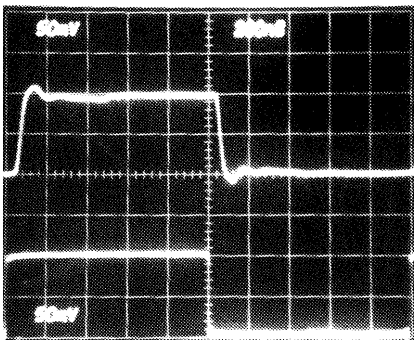
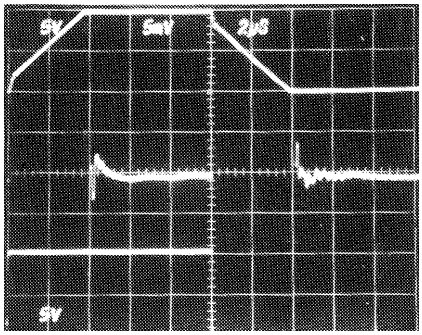


FIGURE 21.Simple Sample-and-Hold System

Pulse “droop” during the hold interval is 170pA/200pF which is 0.85μV/μs; (i.e., 170pA/200pF). If C1 were increased to 2000pF, the “hold-droop” rate will decrease to 0.085μV/μs, but the slew rate would decrease to 0.25V/μs. Figure 22 shows dynamic characteristic waveforms of this sample-and-hold system.

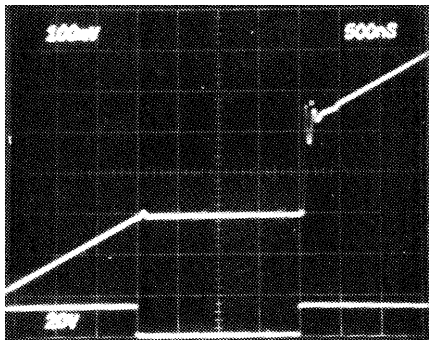


Top Trace: Output; 50mV/Div., 200ns/Div.
Bottom Trace: Input; 50mV/Div., 200ns/Div.



Top Trace: Output Signal; 5V/Div, 2μs/Div.
Center Trace: Difference of Input and Output Signals through Tektronix Amplifier 7A13; 5mV/Div., 2μs/Div.
Bottom Trace: Input Signal; 5V/Div., 2μs/Div.

LARGE SIGNAL RESPONSE AND SETTLING TIME



SAMPLING RESPONSE

Top Trace: Output; 100mV/Div., 500ns/Div.
Bottom Trace: Input; 20V/Div., 500ns/Div.

FIGURE 22. SAMPLE AND HOLD SYSTEM DYNAMIC CHARACTERISTICS WAVEFORMS

6.9. Current Amplifier

The low input terminal current needed to drive the XL/XD3140 makes it ideal for use in current amplifier applications such as the one shown in Figure 23 (see Note 14). In this circuit, low current is supplied at the input potential as the power supply to load resistor RL. This load current is increased by the multiplication factor R2/R1, when the load current is monitored by the power supply meter M. Thus, if the load current is 100nA, with values shown, the load current presented to the supply will be 100μA; a much easier current to measure in many systems.

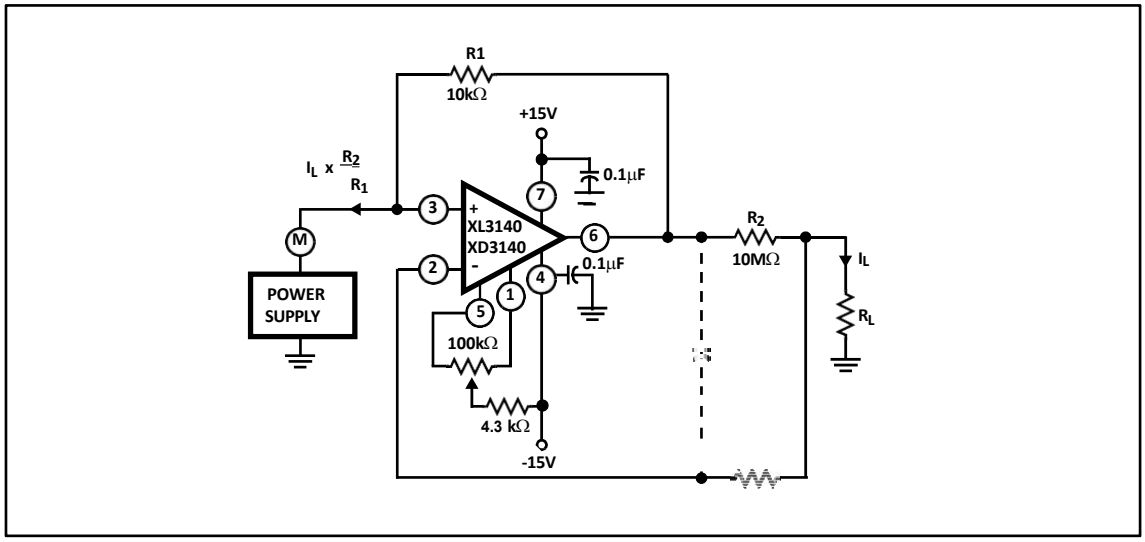


FIGURE 23. BASIC CURRENT AMPLIFIER FOR LOW CURRENT MEASUREMENT SYSTEMS

Note that the input and output voltages are transferred at the same potential and only the output current is multiplied by the scale factor.

The dotted components show a method of decoupling the circuit from the effects of high output load capacitance and the potential oscillation in this situation. Essentially, the necessary high frequency feedback is provided by the capacitor with the dotted series resistor providing load decoupling.

6.10. Full Wave Rectifier

Figure 24 shows a single supply, absolute value, ideal full- wave rectifier with associated waveforms. During positive excursions, the input signal is fed through the feedback network directly to the output. Simultaneously, the positive excursion of the input signal also drives the output terminal (No. 6) of the inverting amplifier in a negative going excursion such that the 1N914 diode effectively disconnects the amplifier from the signal path. During a negative going excursion of the input signal, the XL/XD3140 functions as a normal inverting amplifier with a gain equal to -R2/R1. When the equality of the two equations shown in Figure 26 is satisfied, the full wave output is symmetrical.

NOTE:"Operational Amplifiers Design and Applications", J. G. Graeme, McGraw-Hill Book Company, page 308, "Negative Immittance Converter Circuits".

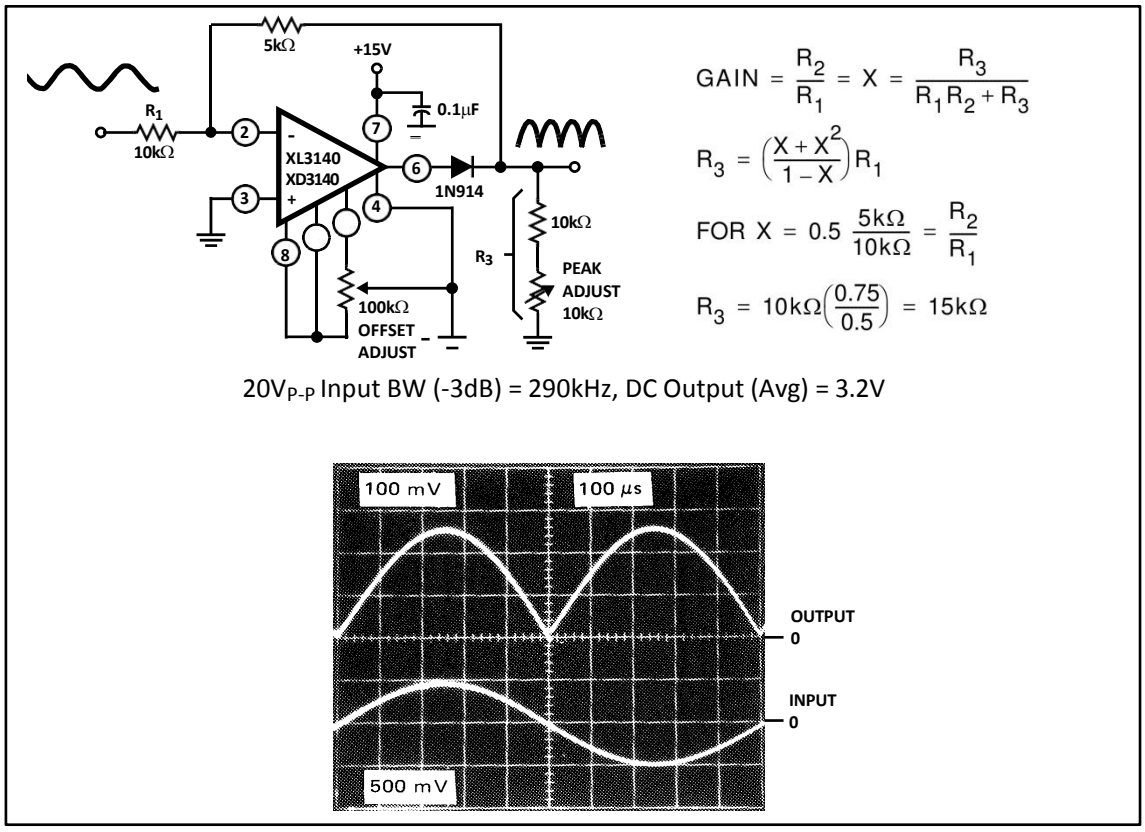


FIGURE 24. SINGLE SUPPLY, ABSOLUTE VALUE, IDEAL FULL WAVE RECTIFIER WITH ASSOCIATED WAVEFORMS

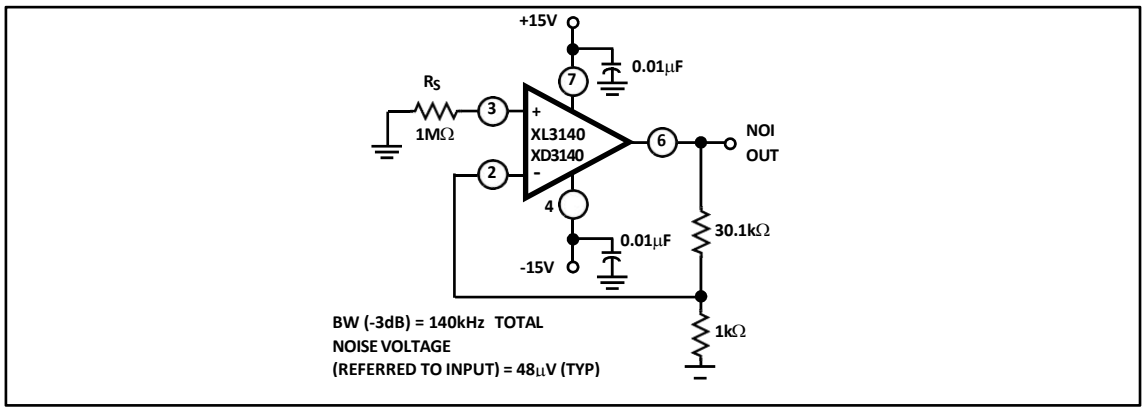


FIGURE 25. TEST CIRCUIT AMPLIFIER (30dB GAIN) USED FOR WIDEBAND NOISE MEASUREMENT

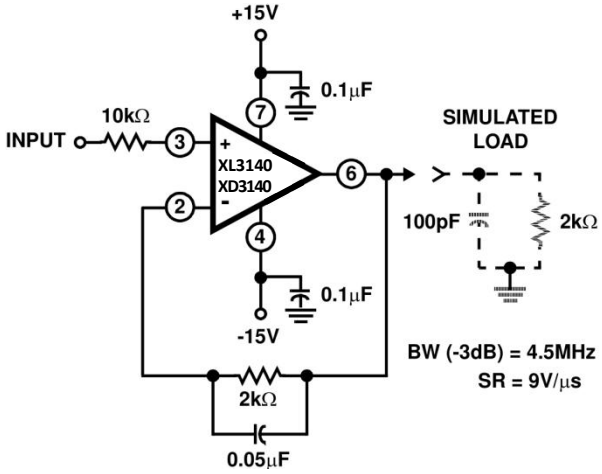
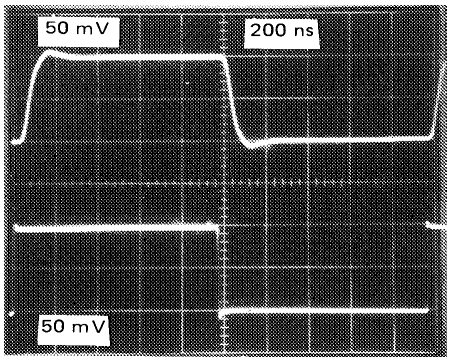
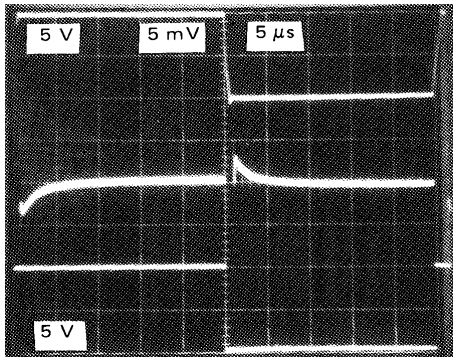


FIGURE 26A. TEST CIRCUIT



Top Trace: Output; 50mV/Div., 200ns/Div.
Bottom Trace: Input; 50mV/Div., 200ns/Div.

FIGURE 26B. SMALL SIGNAL RESPONSE



(Measurement made with Tektronix 7A13 differential amplifier.)
Top Trace: Output Signal; 5V/Div., 5μs/Div.
Center Trace: Difference Signal; 5mV/Div., 5μs/Div.
Bottom Trace: Input Signal; 5V/Div., 5μs/Div.

FIGURE 26C. INPUT-OUTPUT DIFFERENCE SIGNAL SHOWING SETTLING TIME

FIGURE 26. SPLIT SUPPLY VOLTAGE FOLLOWER TEST CIRCUIT AND ASSOCIATED WAVEFORMS

7. Typical Performance Curves

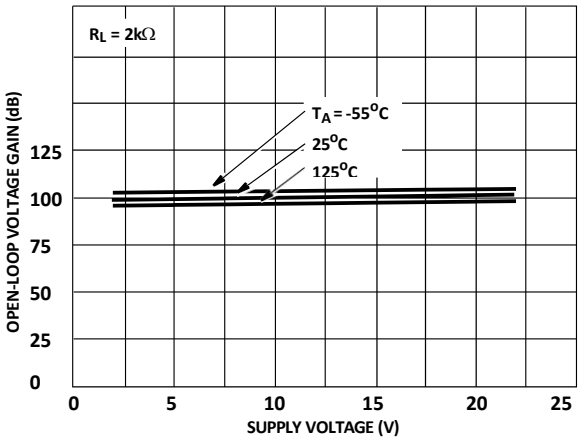


FIGURE 27. OPEN-LOOP VOLTAGE GAIN vs SUPPLY VOLTAGE AND TEMPERATURE

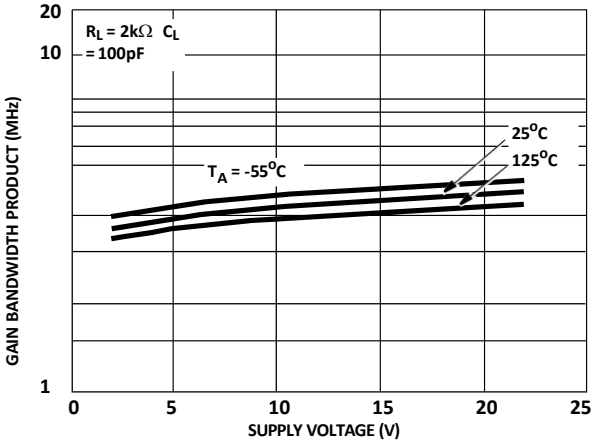


FIGURE 28. GAIN BANDWIDTH PRODUCT vs SUPPLY VOLTAGE AND TEMPERATURE

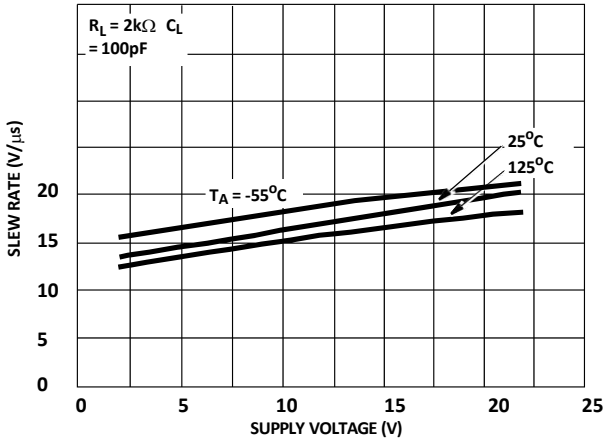


FIGURE 29. SLEW RATE vs SUPPLY VOLTAGE AND TEMPERATURE

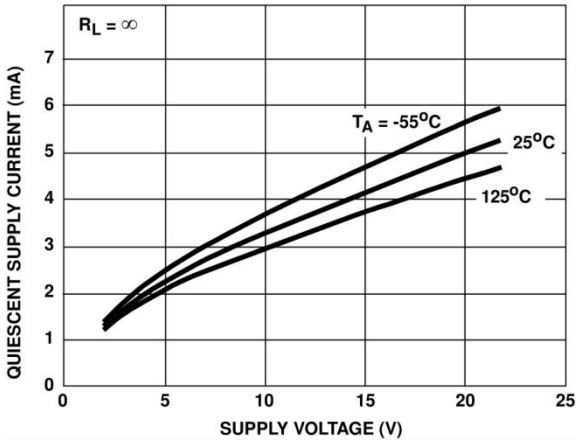


FIGURE 30. QUIESCENT SUPPLY CURRENT vs SUPPLY VOLTAGE AND TEMPERATURE

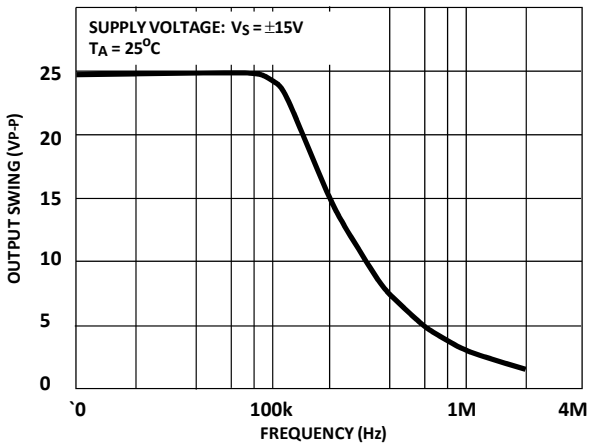


FIGURE 31. MAXIMUM OUTPUT VOLTAGE SWING vs FREQUENC

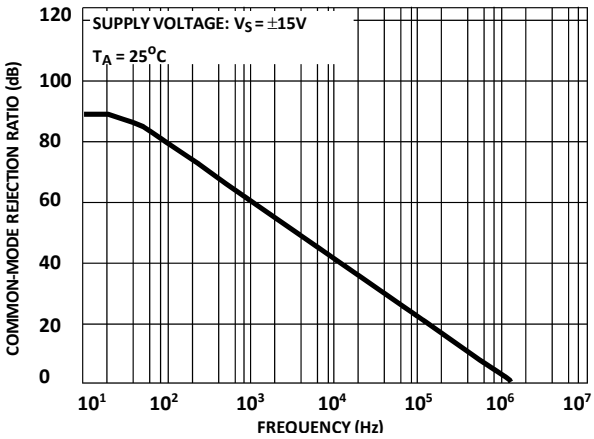


FIGURE 32. COMMON MODE REJECTION RATIO vs FREQUENCY

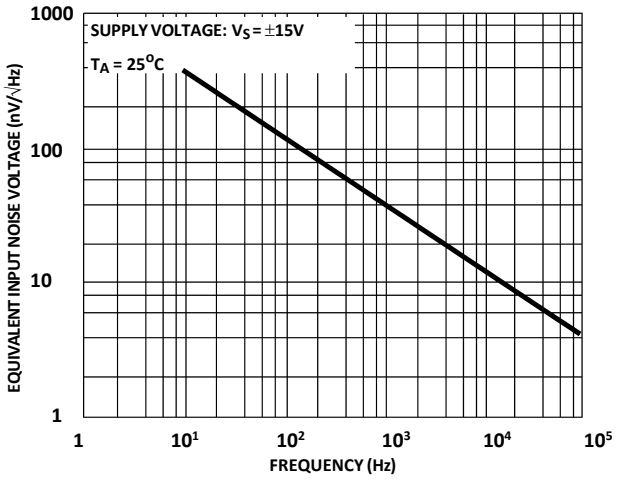


FIGURE 33. EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

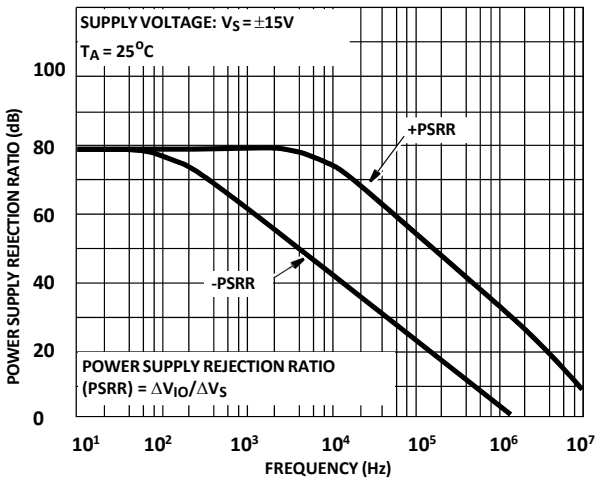


FIGURE 34. POWER SUPPLY REJECTION RATIO vs FREQUENCY

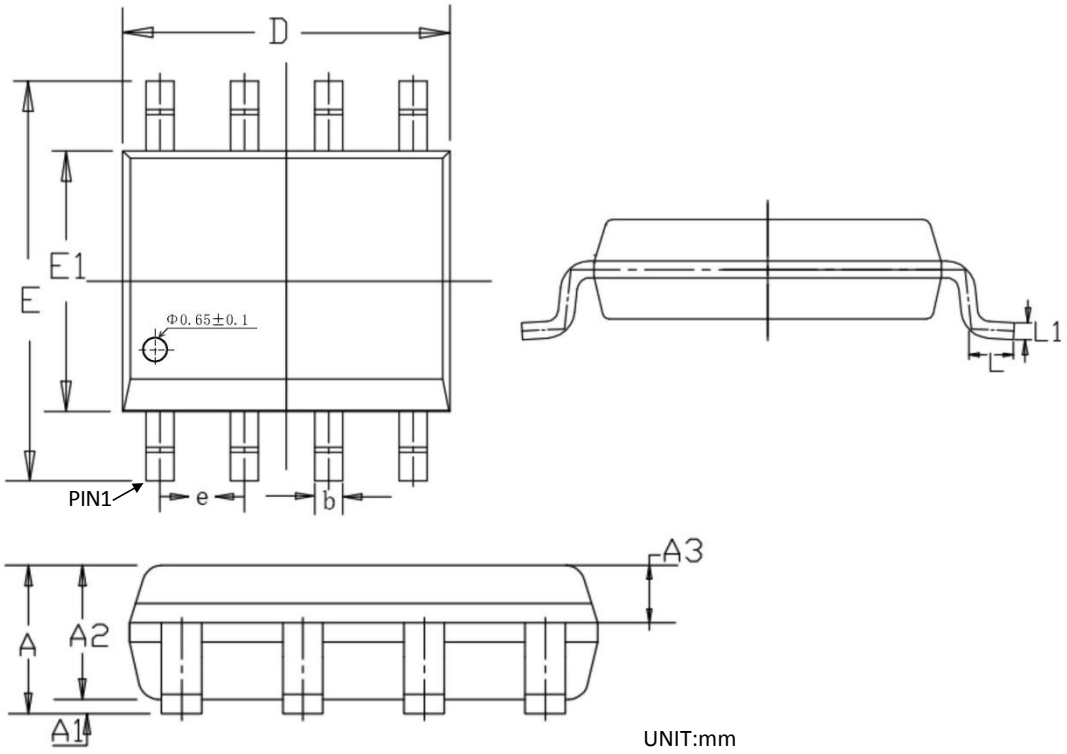
8. ORDERING INFORMATION

Ordering Information

Part Number	Device Marking	Package Type	Body size (mm)	Temperature (°C)	MSL	Transport Media	Package Quantity
XL3140	XL3140	SOP8	4.90 * 3.90	-40 to +85	MSL3	T&R	2500
XD3140	XD3140	DIP8	9.25 * 6.38	-40 to +85	MSL3	Tube 50	2000

9. DIMENSIONAL DRAWINGS

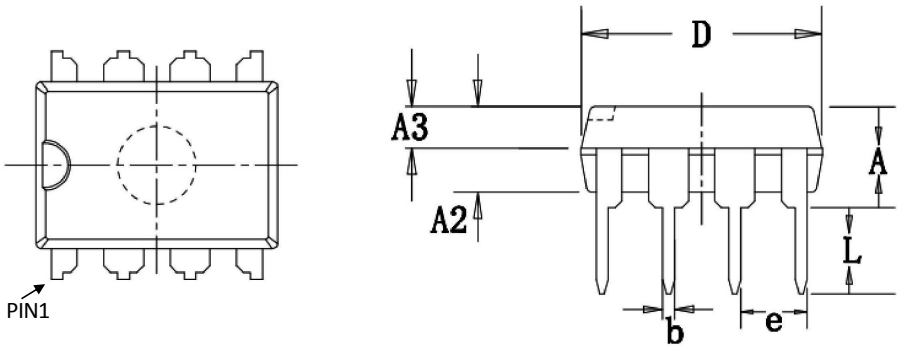
SOP8

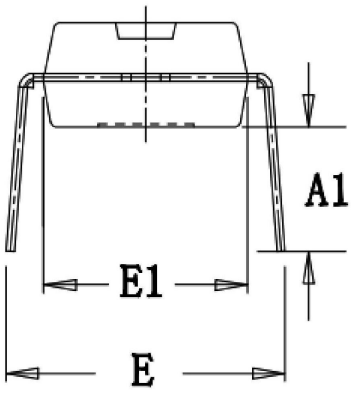


UNIT:mm

	MIN	NOM	MAX
A	1.450	1.550	1.650
A1	0.100	0.150	0.200
A2	1.300	1.400	1.500
A3	0.600	0.650	0.700
b	0.380	–	0.510
e	1.240	1.270	1.300
D	4.800	4.900	5.000
E	5.800	6.000	6.200
E1	3.800	3.900	4.000
L	0.450	0.600	0.750
L1	—	0.25BSC	—

DIP8





UNIT:mm

	MIN	NOM	MAX
A	3.600	3.800	4.000
A1	3.786	3.886	3.986
A2	3.200	3.300	3.400
A3	1.550	1.600	1.650
b	0.440	–	0.490
e	2.510	2.540	2.570
D	9.150	9.250	9.350
E	7.800	8.500	9.200
E1	6.280	6.380	6.480
L	3.000	–	–