# MC74HC4851A, MC74HC4852A

## Analog Multiplexers/ Demultiplexers with Injection Current Effect Control

### Automotive Customized

These devices are pin compatible to standard HC405x and MC1405xB analog mux/demux devices, but feature injection current effect control. This makes them especially suited for usage in automotive applications where voltages in excess of normal logic voltage are common.

The injection current effect control allows signals at disabled analog input channels to exceed the supply voltage range without affecting the signal of the enabled analog channel. This eliminates the need for external diode/resistor networks typically used to keep the analog channel signals within the supply voltage range.

The devices utilize low power silicon gate CMOS technology. The Channel Select and Enable inputs are compatible with standard CMOS outputs.

### Features

- Injection Current Cross−Coupling Less than 1 mV/mA (See Figure 10)
- Pin Compatible to HC405X and MC1405XB Devices
- Power Supply Range ($V_{CC}$ − GND) = 2.0 to 6.0 V
- In Compliance With the Requirements of JEDEC Standard No. 7 A
- Chip Complexity: 154 FETs or 36 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
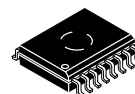- These Devices are Pb−Free, Halogen Free and are RoHS Compliant
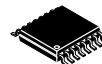
## ON Semiconductor®

www.onsemi.com
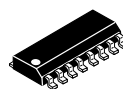
**SOIC−16**
D SUFFIX
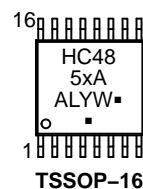CASE 751B

**SOIC−16 WIDE**
DW SUFFIX
CASE 751G

**TSSOP−16**
DT SUFFIX
CASE 948F

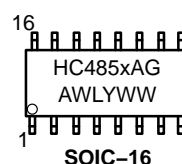**QFN16**
MN SUFFIX
CASE 485AW

### MARKING DIAGRAMS

```
16
HC485xAG
AWLYWW
1
```
**SOIC−16**

```
16
HC4851A
AWLYWWG
1
```
**SOIC−16 WIDE**

```
16
HC48
5xA
ALYW▪
1
```
**TSSOP−16**

```
4851
ALYW▪
```
**QFN16***
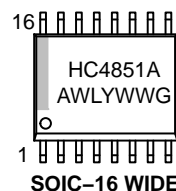
*V4851 marking used for NLV74HC4851AMN1TWG

| | |
|---|---|
| x | = 1 or 2 |
| A | = Assembly Location |
| WL, L | = Wafer Lot |
| YY, Y | = Year |
| WW, W | = Work Week |
| G or ▪ | = Pb−Free Package |

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.
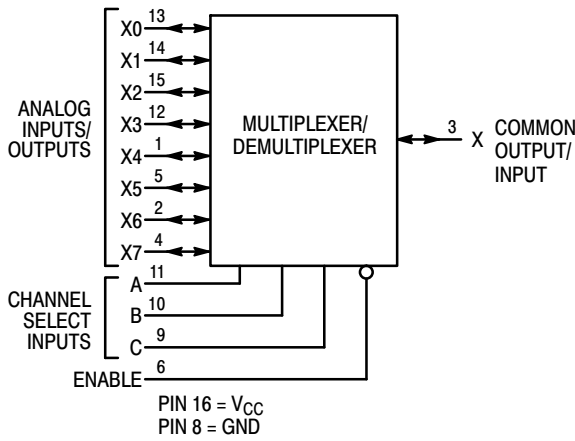
# MC74HC4851A, MC74HC4852A



**Figure 1. MC74HC4851A Logic Diagram**
**Single−Pole, 8−Position Plus Common Off**

### FUNCTION TABLE − MC74HC4851A

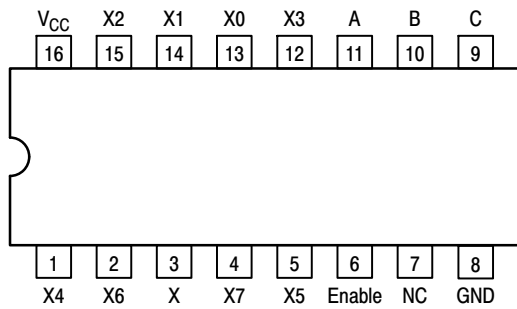| Control Inputs | | | | |
| --- | --- | --- | --- | --- |
| | Select | | | |
| Enable | C | B | A | ON Channels |
| L | L | L | L | X0 |
| L | L | L | H | X1 |
| L | L | H | L | X2 |
| L | L | H | H | X3 |
| L | H | L | L | X4 |
| L | H | L | H | X5 |
| L | H | H | L | X6 |
| L | H | H | H | X7 |
| H | X | X | X | NONE |



**Figure 2. MC74HC4851A 16−Lead Pinout** (Top View)
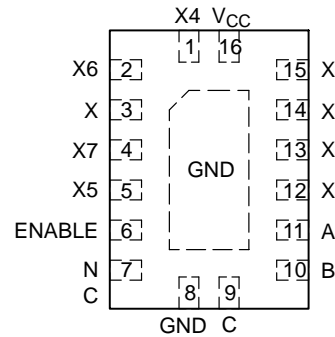


**Figure 3. MC74HC4851A QFN Pinout**

### FUNCTION TABLE − MC74HC4852A

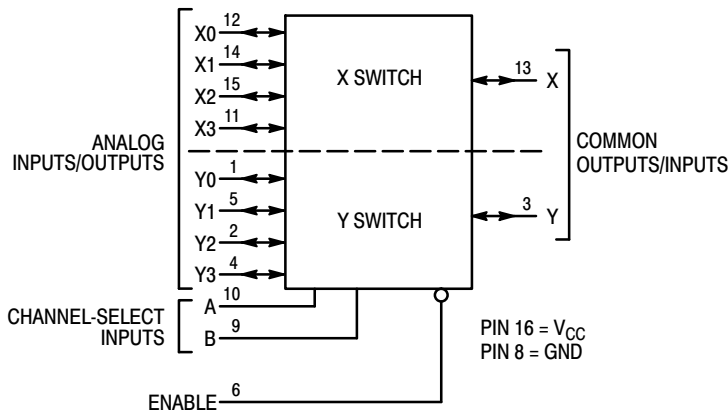| Control Inputs | | | | |
| --- | --- | --- | --- | --- |
| | Select | | | |
| Enable | B | A | ON Channels | |
| L | L | L | Y0 | X0 |
| L | L | H | Y1 | X1 |
| L | H | L | Y2 | X2 |
| L | H | H | Y3 | X3 |
| H | X | X | NONE | |

X = Don't Care



**Figure 4. MC74HC4852A Logic Diagram**
**Double−Pole, 4−Position Plus Common Off**
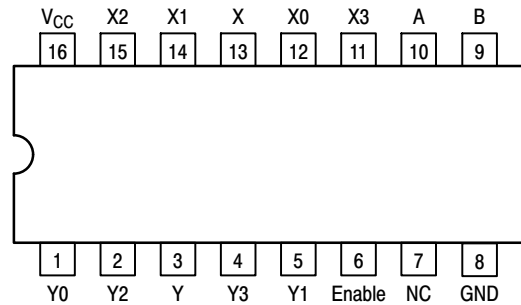


**Figure 5. MC74HC4852A 16−Lead Pinout** (Top View)

# MC74HC4851A, MC74HC4852A

## MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|--------|-----------|-------|------|
| $V_{CC}$ | Positive DC Supply Voltage          (Referenced to GND) | −0.5 to +7.0 | V |
| $V_{in}$ | DC Input Voltage (Any Pin)          (Referenced to GND) | −0.5 to $V_{CC}$ + 0.5 | V |
| I | DC Current, Into or Out of Any Pin | ±25 | mA |
| $P_D$ | Power Dissipation in Still Air,          SOIC Package†          TSSOP Package† | 500 450 | mW |
| $T_{stg}$ | Storage Temperature Range | −65 to +150 | °C |
| $T_L$ | Lead Temperature, 1 mm from Case for 10 Seconds          SOIC or TSSOP Package | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
†Derating: SOIC Package: −7 mW/°C from 65° to 125°C
          TSSOP Package: −6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range GND $\leq$ ($V_{in}$ or $V_{out}$) $\leq$ $V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or $V_{CC}$). Unused outputs must be left open.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | | Min | Max | Unit |
|--------|-----------|---|-----|-----|------|
| $V_{CC}$ | Positive DC Supply Voltage | (Referenced to GND) | 2.0 | 6.0 | V |
| $V_{in}$ | DC Input Voltage (Any Pin) | (Referenced to GND) | GND | $V_{CC}$ | V |
| $V_{IO}$* | Static or Dynamic Voltage Across Switch | | 0.0 | 1.2 | V |
| $T_A$ | Operating Temperature Range, All Package Types | | −55 | +125 | °C |
| $t_r$, $t_f$ | Input Rise/Fall Time    (Channel Select or Enable Inputs) | $V_{CC}$ = 2.0 V  $V_{CC}$ = 4.5 V  $V_{CC}$ = 6.0 V | 0 0 0 | 1000 500 400 | ns |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
*For voltage drops across switch greater than 1.2 V (switch on), excessive $V_{CC}$ current may be drawn; i.e., the current out of the switch may contain both $V_{CC}$ and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

## DC CHARACTERISTICS — Digital Section (Voltages Referenced to GND) $V_{EE}$ = GND, Except Where Noted

| Symbol | Parameter | Condition | $V_{CC}$ V | Guaranteed Limit | | | Unit |
|--------|-----------|-----------|------|-----------------|---|---|------|
| | | | | −55 to 25°C | ≤85°C | ≤125°C | |
| $V_{IH}$ | Minimum High−Level Input Voltage, Channel−Select or Enable Inputs | $R_{on}$ = Per Spec | 2.0 3.0 4.5 6.0 | 1.50 2.10 3.15 4.20 | 1.50 2.10 3.15 4.20 | 1.50 2.10 3.15 4.20 | V |
| $V_{IL}$ | Maximum Low−Level Input Voltage, Channel−Select or Enable Inputs | $R_{on}$ = Per Spec | 2.0 3.0 4.5 6.0 | 0.50 0.90 1.35 1.80 | 0.50 0.90 1.35 1.80 | 0.50 0.90 1.35 1.80 | V |
| $I_{in}$ | Maximum Input Leakage Current on Digital Pins (Enable/A/B/C) | $V_{in}$ = $V_{CC}$ or GND | 6.0 | ±0.1 | ±1.0 | ±1.0 | µA |
| $I_{CC}$ | Maximum Quiescent Supply Current (per Package) | $V_{in(digital)}$ = $V_{CC}$ or GND  $V_{in(analog)}$ = GND | 6.0 | 2 | 20 | 40 | µA |

### DC CHARACTERISTICS — Analog Section

| Symbol | Parameter | Condition | $V_{CC}$ | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | −55 to 25°C | ≤85°C | ≤125°C | |
| $R_{on}$ | Maximum "ON" Resistance | $V_{in} = V_{IL}$ or $V_{IH}$; $V_{IS} = V_{CC}$ to GND (Note 1); $I_S \leq 2.0$ mA (Note 2) | 2.0<br>3.0<br>4.5<br>6.0 | 1700<br>1100<br>550<br>400 | 1750<br>1200<br>650<br>500 | 1800<br>1300<br>750<br>600 | Ω |
| $\Delta R_{on}$ | Delta "ON" Resistance | $V_{in} = V_{IL}$ or $V_{IH}$; $V_{IS} = V_{CC}/2$ (Note 1); $I_S \leq 2.0$ mA (Note 2) | 2.0<br>3.0<br>4.5<br>6.0 | 300<br>160<br>80<br>60 | 400<br>200<br>100<br>80 | 500<br>240<br>120<br>100 | Ω |
| $I_{off}$ | Maximum Off–Channel Leakage Current, Any One Channel <br> Common Channel | $V_{in} = V_{CC}$ or GND | 6.0 | ±0.1<br>±0.1 | ±0.1<br>±0.1 | ±0.1<br>±0.1 | µA |
| $I_{on}$ | Maximum On–Channel Leakage Channel–to–Channel | $V_{in} = V_{CC}$ or GND | 6.0 | ±0.1 | ±0.1 | ±0.1 | µA |

1. $V_{IS}$ is the input voltage of an analog I/O pin.
2. $I_S$ is the currebnt flowing in or out of analog I/O pin.

### AC CHARACTERISTICS ($C_L$ = 50 pF, Input $t_r = t_f$ = 6 ns)

| Symbol | Parameter | $V_{CC}$ | −55 to 25°C | ≤85°C | ≤125°C | Unit |
|---|---|---|---|---|---|---|
| $t_{PHL}$, $t_{PLH}$ | Maximum Propagation Delay, Analog Input to Analog Output | 2.0<br>3.0<br>4.5<br>6.0 | 160<br>80<br>40<br>30 | 180<br>90<br>45<br>35 | 200<br>100<br>50<br>40 | ns |
| $t_{PHL}$, $t_{PHZ,PZH}$ $t_{PLH}$, $t_{PLZ,PZL}$ | Maximum Propagation Delay, Enable or Channel–Select to Analog Output | 2.0<br>3.0<br>4.5<br>6.0 | 260<br>160<br>80<br>78 | 280<br>180<br>90<br>80 | 300<br>200<br>100<br>80 | ns |
| $C_{in}$ | Maximum Input Capacitance      Digital Pins<br>(All Switches Off)      Any Single Analog Pin<br>(All Switches Off)      Common Analog Pin | | 10<br>35<br>40 | 10<br>35<br>40 | 10<br>35<br>40 | pF |
| $C_{PD}$ | Power Dissipation Capacitance      Typical | 5.0 | 20 | | | pF |

### INJECTION CURRENT COUPLING SPECIFICATIONS ($V_{CC}$ = 5V, $T_A$ = −55°C to +125°C)

| Symbol | Parameter | Condition | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V\Delta_{out}$ | Maximum Shift of Output Voltage of Enabled Analog Channel | $I_{in}^* \leq 1$ mA, $R_S \leq 3,9$ kΩ<br>$I_{in}^* \leq 10$ mA, $R_S \leq 3,9$ kΩ<br>$I_{in}^* \leq 1$ mA, $R_S \leq 20$ kΩ<br>$I_{in}^* \leq 10$ mA, $R_S \leq 20$ kΩ | 0.1<br>1.0<br>0.5<br>5.0 | 1.0<br>5.0<br>2.0<br>20 | mV |

* $I_{in}$ = Total current injected into all disabled channels.
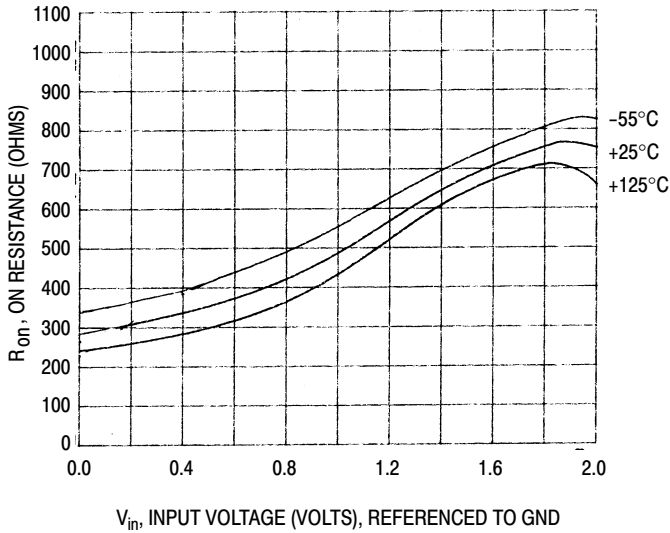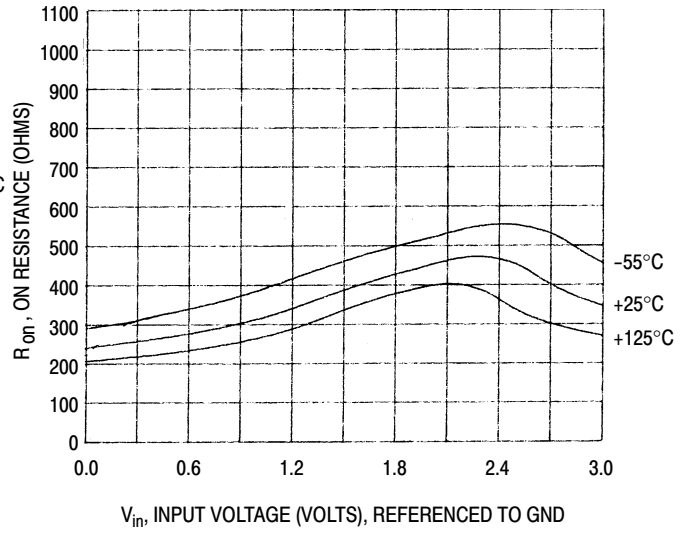
**Figure 6. Typical On Resistance $V_{CC}$ = 2V**
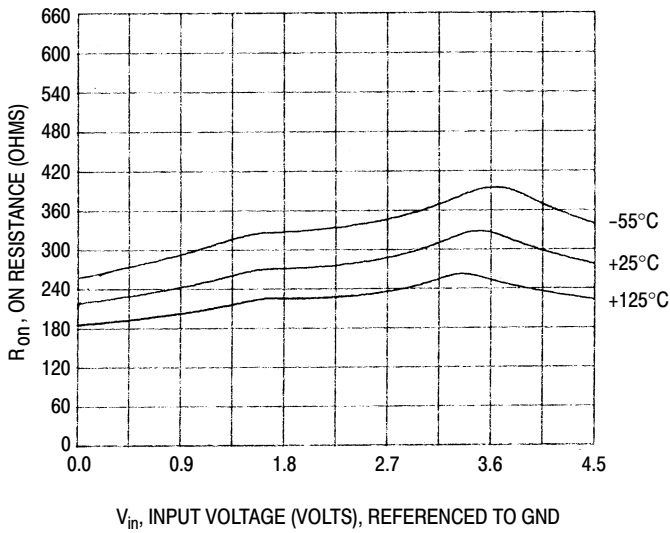


**Figure 7. Typical On Resistance $V_{CC}$ = 3V**
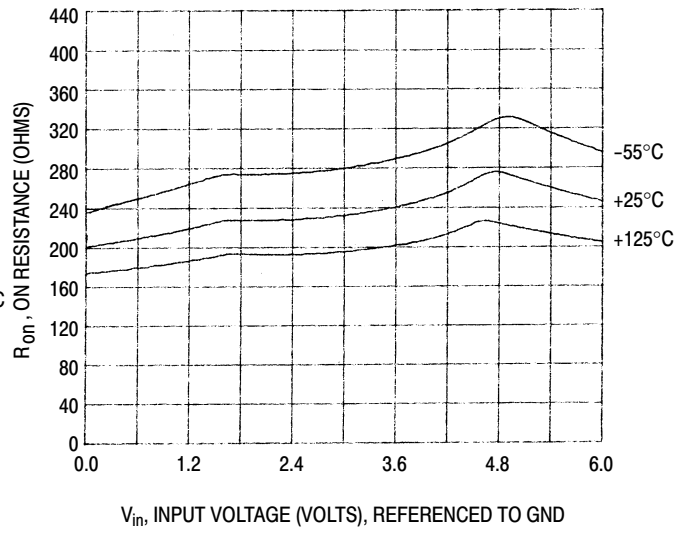


**Figure 8. Typical On Resistance $V_{CC}$ = 4.5V**



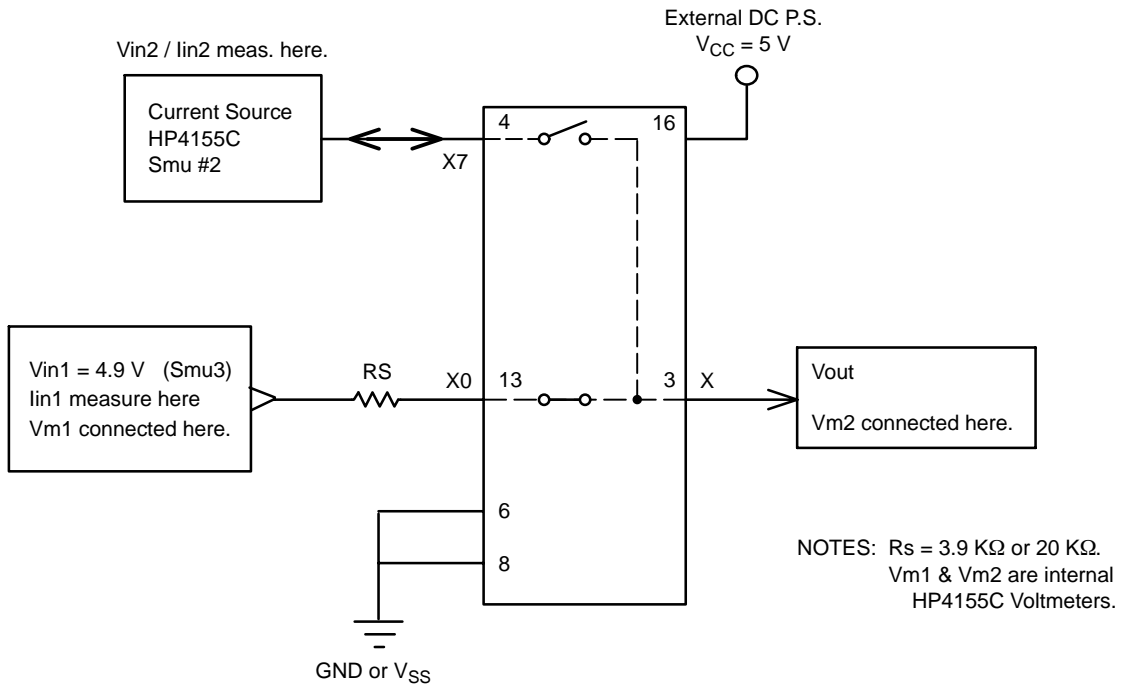**Figure 9. Typical On Resistance $V_{CC}$ = 6V**

# MC74HC4851A, MC74HC4852A

Vin2 / Iin2 meas. here.

External DC P.S.
$V_{CC}$ = 5 V

Current Source
HP4155C
Smu #2

X7    4        16

Vin1 = 4.9 V   (Smu3)
Iin1 measure here
Vm1 connected here.

RS    X0    13        3    X

Vout

Vm2 connected here.

6

8

NOTES:  Rs = 3.9 KΩ or 20 KΩ.
Vm1 & Vm2 are internal
HP4155C Voltmeters.

GND or $V_{SS}$

**Figure 10. Injection Current Coupling Specification**
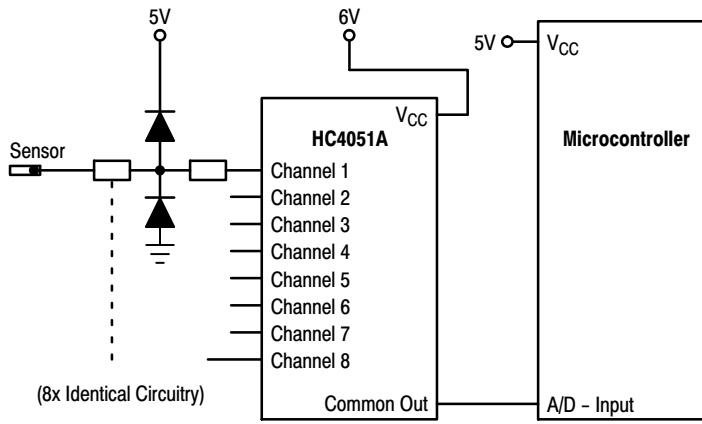
**Figure 11. Actual Technology**
Requires 32 passive components and one extra 6V regulator
to suppress injection current into a standard HC4051 multiplexer
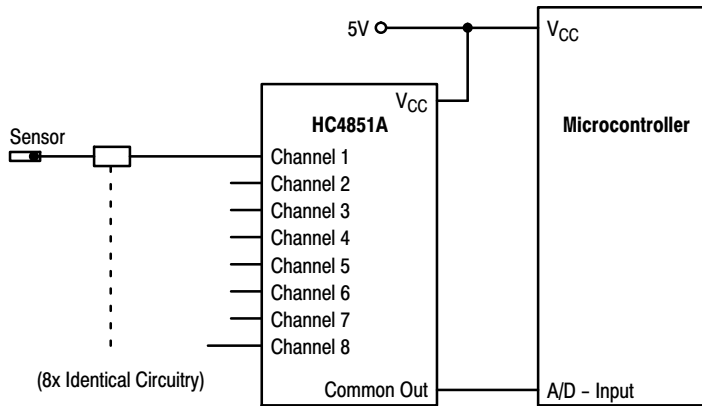


**Figure 12. MC74HC4851A Solution**
Solution by applying the HC4851A multiplexer
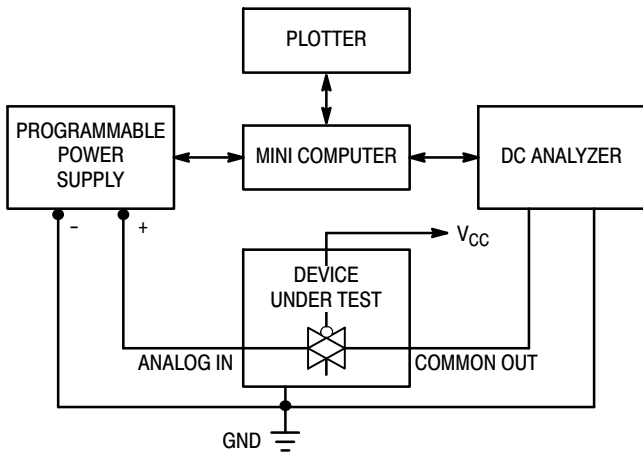
**Figure 13. On Resistance Test Set−Up**
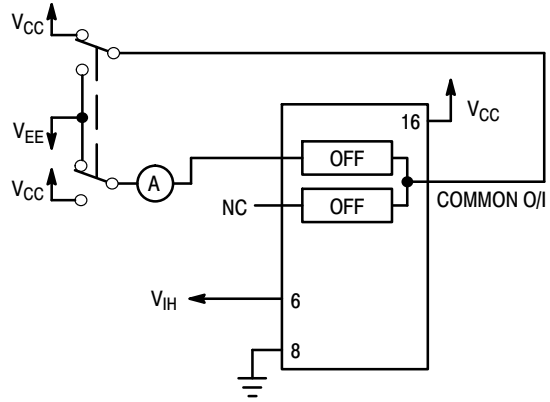


**Figure 14. Maximum Off Channel Leakage Current, Any One Channel, Test Set−Up**
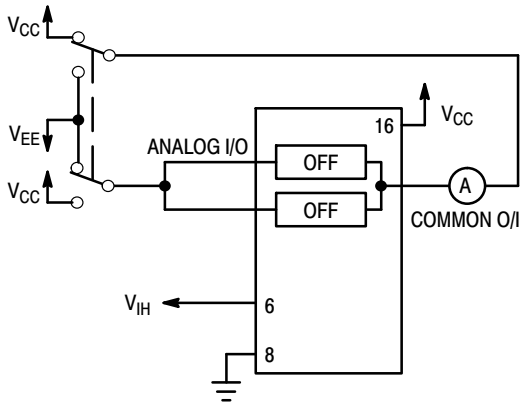


**Figure 15. Maximum Off Channel Leakage Current, Common Channel, Test Set−Up**
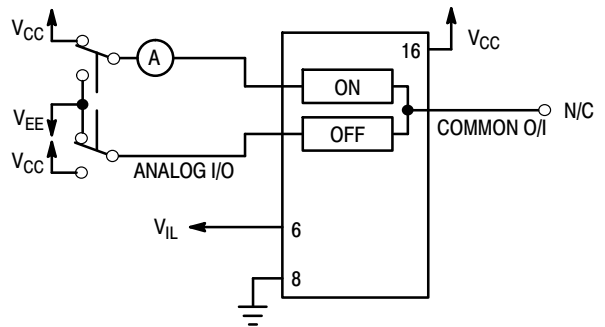


**Figure 16. Maximum On Channel Leakage Current, Channel to Channel, Test Set−Up**
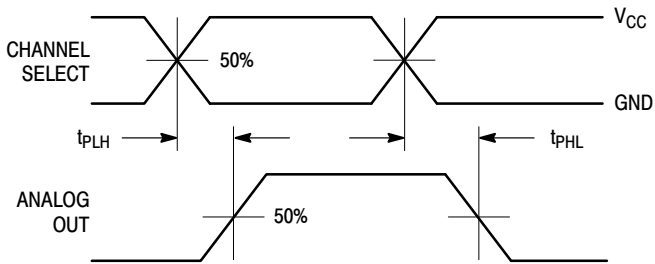


**Figure 17. Propagation Delays, Channel Select to Analog Out**
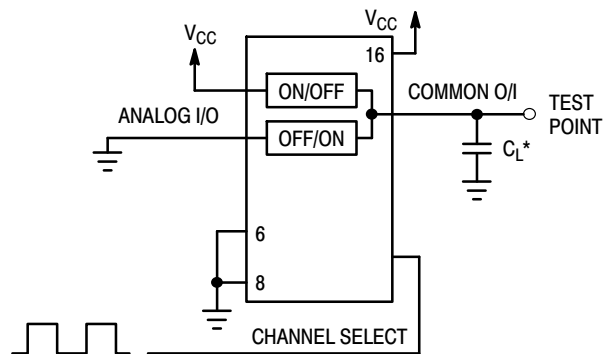


*Includes all probe and jig capacitance

**Figure 18. Propagation Delay, Test Set−Up Channel Select to Analog Out**
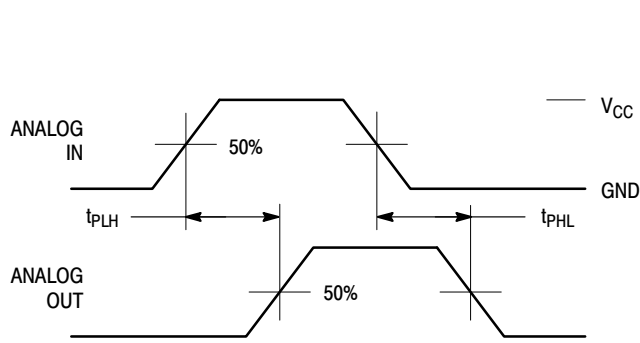
Figure 19. Propagation Delays, Analog In to Analog Out
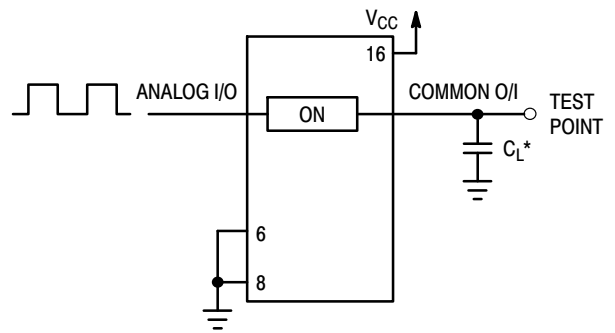


*Includes all probe and jig capacitance

Figure 20. Propagation Delay, Test Set−Up Analog In to Analog Out
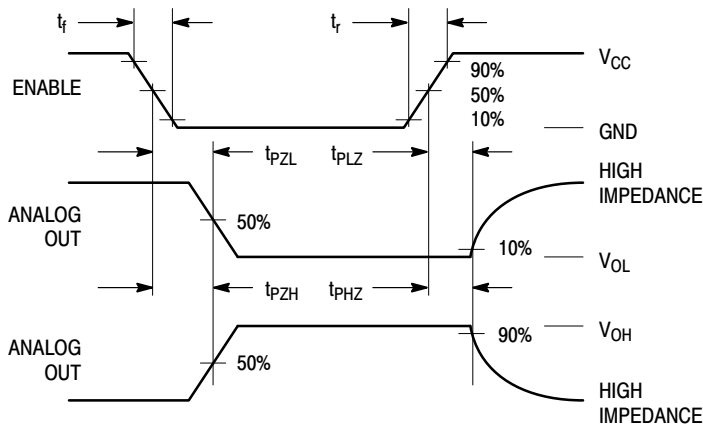


Figure 21. Propagation Delays, Enable to Analog Out
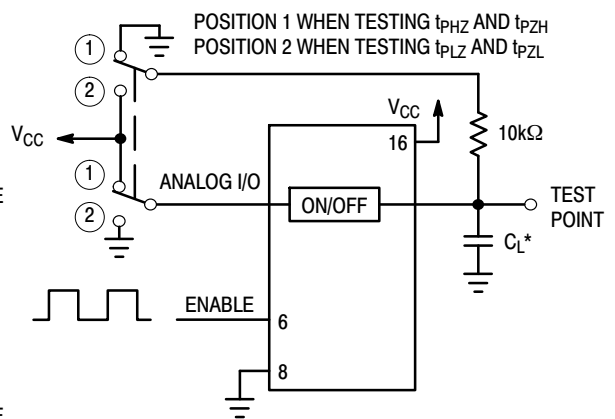


Figure 22. Propagation Delay, Test Set−Up Enable to Analog Out
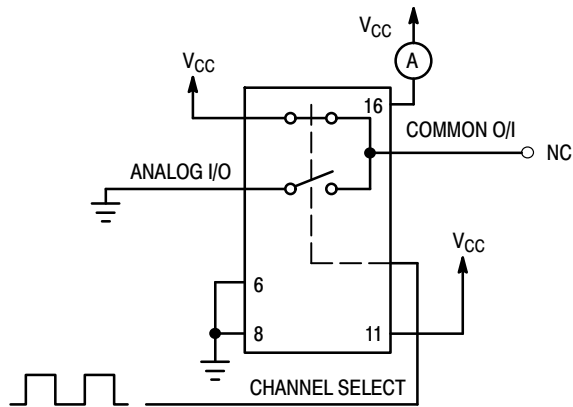


Figure 23. Power Dissipation Capacitance, Test Set−Up

# MC74HC4851A, MC74HC4852A
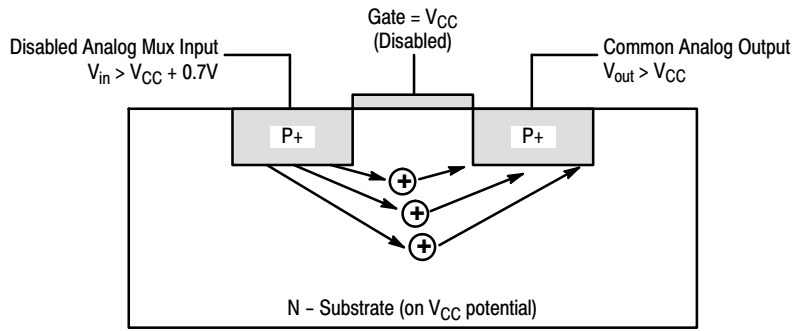


**Figure 24. Diagram of Bipolar Coupling Mechanism**
Appears if $V_{in}$ exceeds $V_{CC}$, driving injection current into the substrate
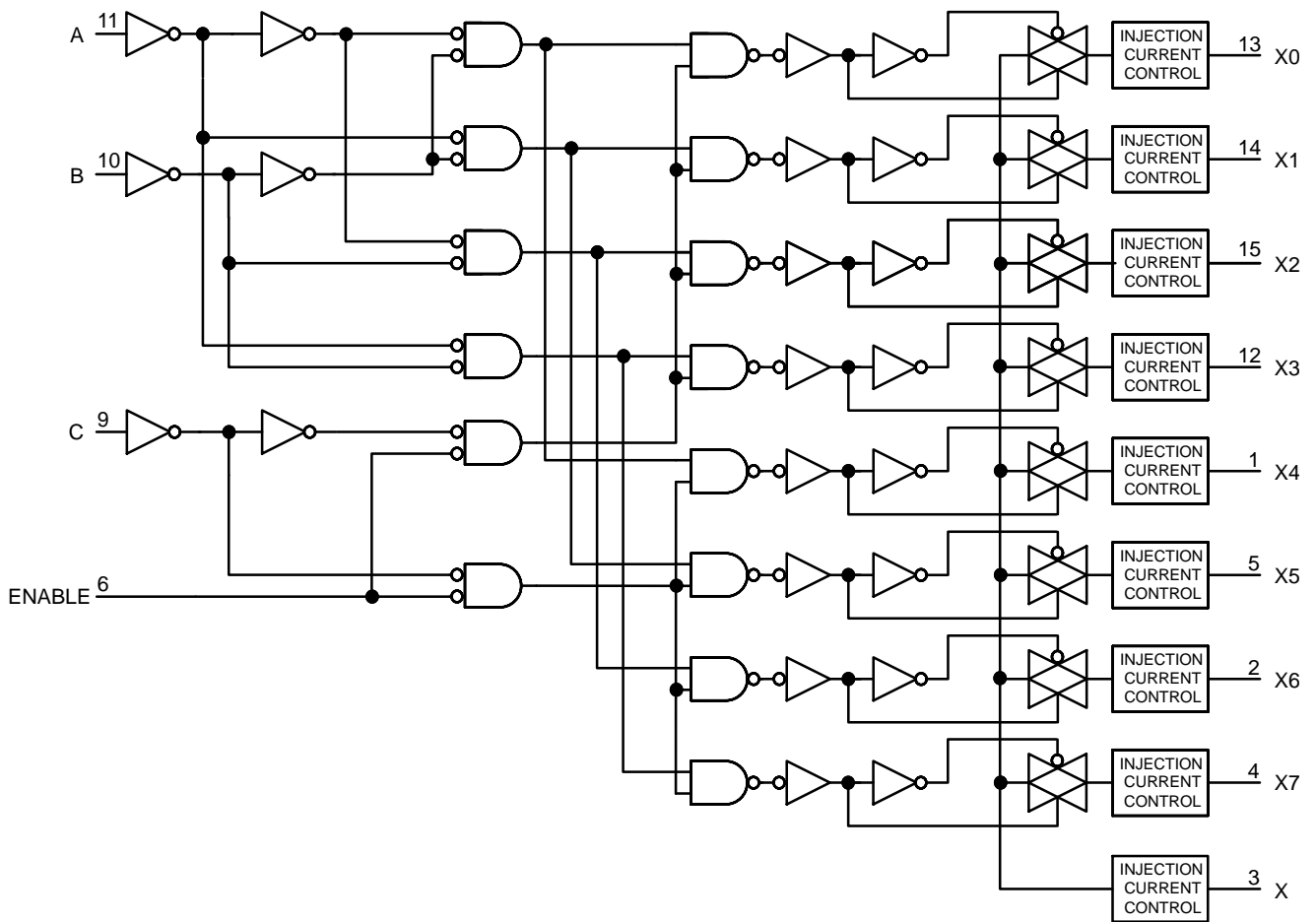


**Figure 25. Function Diagram, HC4851A**

# MC74HC4851A, MC74HC4852A
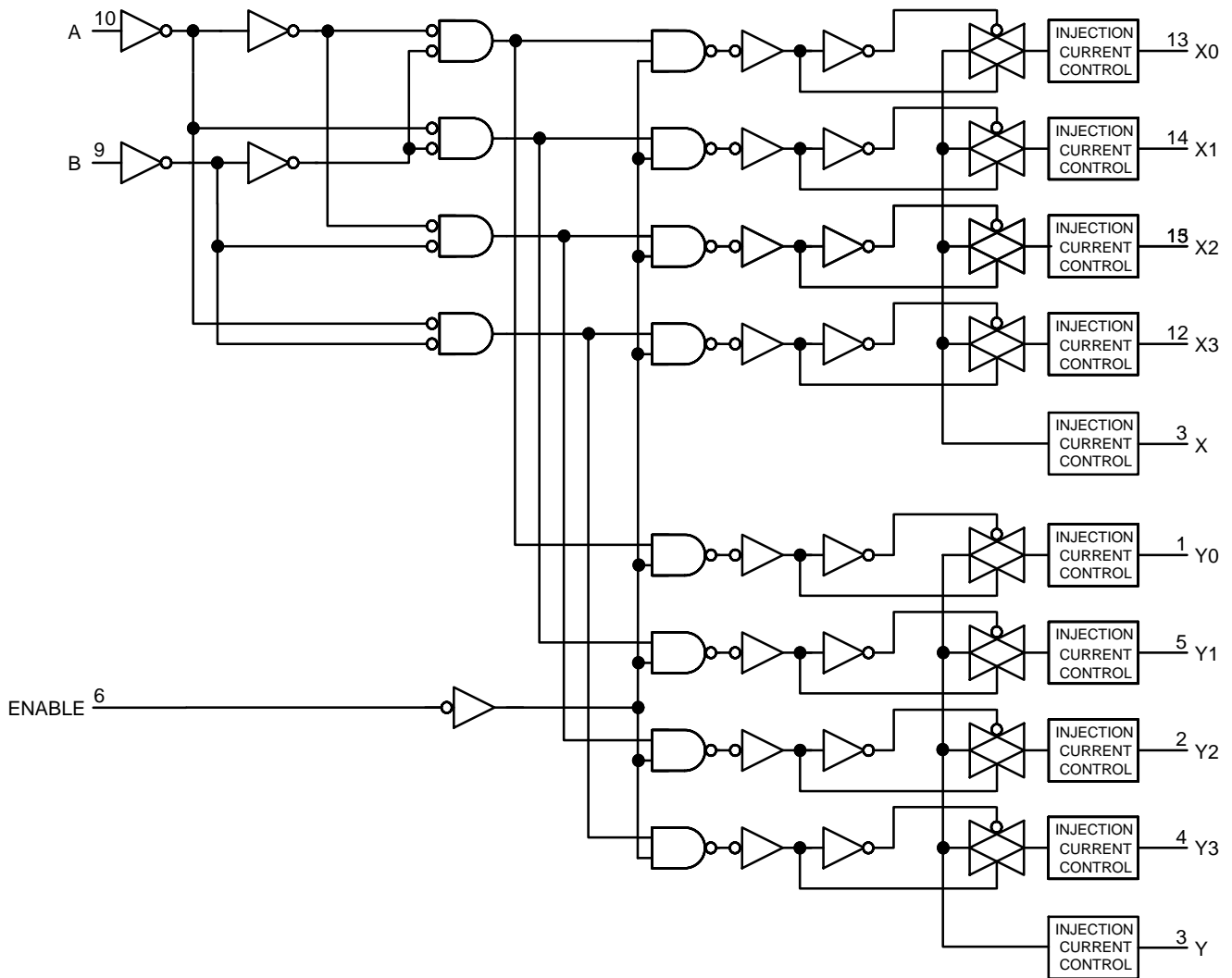


**Figure 26. Function Diagram, HC4852A**

**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| MC74HC4851ADG | SOIC−16 (Pb−Free) | 48 Units / Rail |
| MC74HC4851ADR2G | | 2500 Units / Tape & Reel |
| NLVHC4851ADR2G* | | 2500 Units / Tape & Reel |
| MC74HC4851ADTR2G | TSSOP−16 (Pb−Free) | 2500 Units / Tape & Reel |
| NLVHC4851ADTR2G* | | |
| MC74HC4851ADWR2G | SOIC−16 WIDE (Pb−Free) | 1000 Units / Tape & Reel |
| NLVHC4851ADWR2G* | | |
| NLV74HC4851AMNTWG*# | QFN16 (Pb−Free) | 3000 Units / Tape & Reel |
| NLV74HC4851AMN1TWG*# | | 3000 Units / Tape & Reel |

| Device | Package | Shipping† |
|---|---|---|
| MC74HC4852ADG | SOIC−16 (Pb−Free) | 48 Units / Rail |
| MC74HC4852ADR2G | | 2500 Units / Tape & Reel |
| NLV74HC4852ADR2G* | | 2500 Units / Tape & Reel |
| MC74HC4852ADTR2G | TSSOP−16 (Pb−Free) | 2500 Units / Tape & Reel |
| NLVHC4852ADTR2G* | | |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

#MN suffix is with pull−back lead, MN1 is without pull−back lead. Refer to 'Detail A' of case outline on page 16.

# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

**ON Semiconductor®**

**QFN16, 2.5x3.5, 0.5P**
CASE 485AW–01
ISSUE O
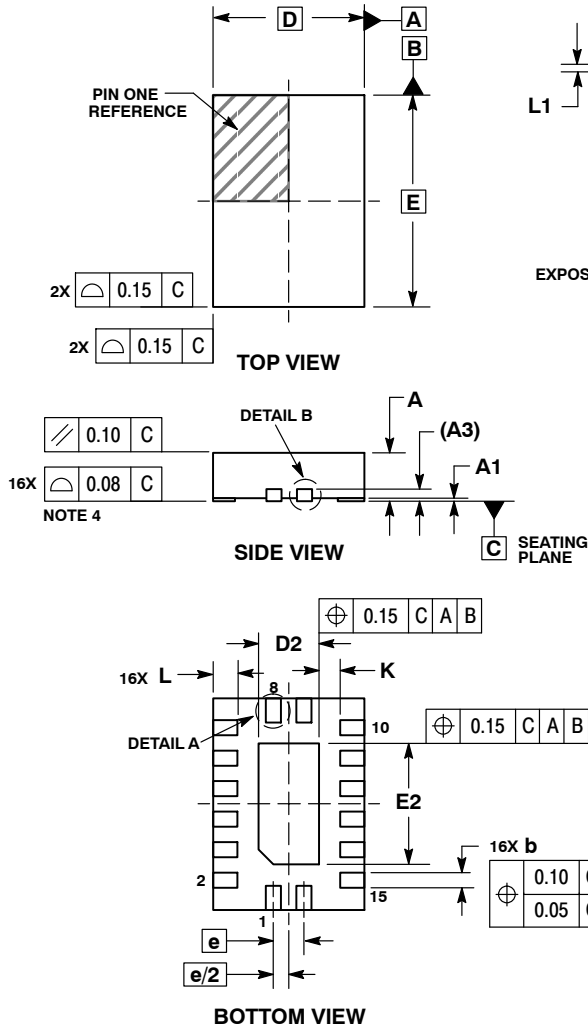
DATE 11 DEC 2008

**SCALE 2:1**

1

**TOP VIEW**

PIN ONE REFERENCE

2X ⌓ 0.15 C

2X ⌓ 0.15 C

D

A
B

E

**DETAIL A**
**ALTERNATE TERMINAL CONSTRUCTIONS**

L

L

L1

**DETAIL B**
**ALTERNATE CONSTRUCTIONS**

EXPOSED Cu    MOLD CMPD

**SIDE VIEW**

⫽ 0.10 C

16X ⌓ 0.08 C

NOTE 4

DETAIL B

A

(A3)

A1

C SEATING PLANE

**BOTTOM VIEW**

⊕ 0.15 C A B

D2

16X L

K

8

DETAIL A

10    ⊕ 0.15 C A B

E2

2

15

1

16X b

⊕ 0.10 C A B
  0.05 C    NOTE 3

e

e/2

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| DIM | MILLIMETERS | |
| --- | --- | --- |
| | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.20 | 0.30 |
| D | 2.50 BSC | |
| D2 | 0.85 | 1.15 |
| E | 3.50 BSC | |
| E2 | 1.85 | 2.15 |
| e | 0.50 BSC | |
| K | 0.20 | --- |
| L | 0.35 | 0.45 |
| L1 | --- | 0.15 |

## GENERIC MARKING DIAGRAM*
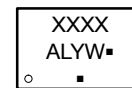
XXXX
ALYW■

XXXX = Specific Device Code
A    = Assembly Location
L    = Wafer Lot
Y    = Year
W    = Work Week
■    = Pb–Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, "G" or microdot " ■", may or may not be present.

## SOLDERING FOOTPRINT*

3.80

2.10

2.80    1.10

0.50 PITCH

1

16X
0.60

16X
0.30

PACKAGE OUTLINE

DIMENSIONS: MILLIMETERS
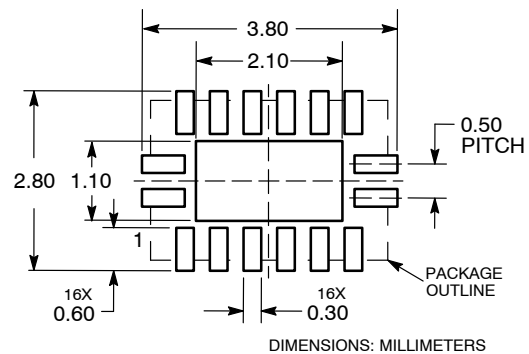
*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**SOIC−16**
CASE 751B−05
ISSUE K

**SCALE 1:1**

DATE 29 DEC 2006

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

⊕ | 0.25 (0.010) Ⓜ | B Ⓢ

⊕ | 0.25 (0.010) Ⓜ | T | B Ⓢ | A Ⓢ

| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NO CONNECTION
5. EMITTER
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NO CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR
15. EMITTER
16. COLLECTOR

STYLE 2:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION
4. CATHODE
5. CATHODE
6. NO CONNECTION
7. ANODE
8. CATHODE
9. CATHODE
10. ANODE
11. NO CONNECTION
12. CATHODE
13. CATHODE
14. NO CONNECTION
15. ANODE
16. CATHODE

STYLE 3:
PIN 1. COLLECTOR, DYE #1
2. BASE, #1
3. EMITTER, #1
4. COLLECTOR, #1
5. COLLECTOR, #2
6. BASE, #2
7. EMITTER, #2
8. COLLECTOR, #2
9. COLLECTOR, #3
10. BASE, #3
11. EMITTER, #3
12. COLLECTOR, #3
13. COLLECTOR, #4
14. BASE, #4
15. EMITTER, #4
16. COLLECTOR, #4

STYLE 4:
PIN 1. COLLECTOR, DYE #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. COLLECTOR, #3
6. COLLECTOR, #3
7. COLLECTOR, #4
8. COLLECTOR, #4
9. BASE, #4
10. EMITTER, #4
11. BASE, #3
12. EMITTER, #3
13. BASE, #2
14. EMITTER, #2
15. BASE, #1
16. EMITTER, #1

STYLE 5:
PIN 1. DRAIN, DYE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. DRAIN, #3
6. DRAIN, #3
7. DRAIN, #4
8. DRAIN, #4
9. GATE, #4
10. SOURCE, #4
11. GATE, #3
12. SOURCE, #3
13. GATE, #2
14. SOURCE, #2
15. GATE, #1
16. SOURCE, #1

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 7:
PIN 1. SOURCE N-CH
2. COMMON DRAIN (OUTPUT)
3. COMMON DRAIN (OUTPUT)
4. GATE P-CH
5. COMMON DRAIN (OUTPUT)
6. COMMON DRAIN (OUTPUT)
7. COMMON DRAIN (OUTPUT)
8. SOURCE P-CH
9. SOURCE P-CH
10. COMMON DRAIN (OUTPUT)
11. COMMON DRAIN (OUTPUT)
12. COMMON DRAIN (OUTPUT)
13. GATE N-CH
14. COMMON DRAIN (OUTPUT)
15. COMMON DRAIN (OUTPUT)
16. SOURCE N-CH

**SOLDERING FOOTPRINT**

8X
6.40

16X 1.12

16X
0.58

1.27
PITCH

DIMENSIONS: MILLIMETERS

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|---|---|---|
| **DESCRIPTION:** | SOIC−16 | **PAGE 1 OF 1** |

**SOIC−16 WB**
CASE 751G
ISSUE E

DATE 08 OCT 2021
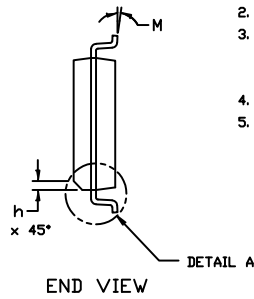
**1**

**SCALE 1:1**

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION OR FLASH TO BE 0.15 PER SIDE.

TOP VIEW

END VIEW

SIDE VIEW

DETAIL A
2X SCALE

| DIM | MILLIMETERS | |
|-----|------|------|
| | MIN. | MAX. |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| B | 0.35 | 0.49 |
| C | 0.23 | 0.32 |
| D | 10.15 | 10.45 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.53 REF | |
| L | 0.50 | 0.90 |
| M | 0° | 7° |

RECOMMENDED
MOUNTING FOOTPRINT

**GENERIC
MARKING DIAGRAM***

XXXXXXXXXXX
XXXXXXXXXXX
AWLYYWWG

XXXXX = Specific Device Code
A      = Assembly Location
WL     = Wafer Lot
YY     = Year
WW     = Work Week
G      = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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|---|---|---|
| DESCRIPTION: | SOIC−16 WB | PAGE 1 OF 1 |

**TSSOP−16**
CASE 948F−01
ISSUE B

DATE 19 OCT 2006

**SCALE 2:1**

16

1

**16X K REF**

⊕ | 0.10 (0.004) Ⓜ | T | U Ⓢ | V Ⓢ

△ | 0.15 (0.006) | T | U Ⓢ

**2X L/2**

L

16        9

B
−U−

PIN 1
IDENT.

1        8

△ | 0.15 (0.006) | T | U Ⓢ

A
−V−

**K**

**K1**

**J1**

**J**

**SECTION N−N**

**N**

0.25 (0.010)

**M**

**N**

**F**

**DETAIL E**

C

△ | 0.10 (0.004)

−T− SEATING
PLANE

D

G

H

−W−

**DETAIL E**

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | −−− | 1.20 | −−− | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.18 | 0.28 | 0.007 | 0.011 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0 ° | 8 ° | 0 ° | 8 ° |

**SOLDERING FOOTPRINT**

7.06

1

0.65
PITCH

16X
0.36

16X
1.26

DIMENSIONS: MILLIMETERS

**GENERIC
MARKING DIAGRAM\***

16

XXXX
XXXX
ALYW

1

XXXX    = Specific Device Code
A        = Assembly Location
L        = Wafer Lot
Y        = Year
W        = Work Week
G or ▪   = Pb−Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

| DOCUMENT NUMBER: | 98ASH70247A | |
|---|---|---|
| DESCRIPTION: | TSSOP−16 | PAGE 1 OF 1 |

**ADDITIONAL INFORMATION**

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