

74F299

Octal Universal Shift/Storage Register with Common Parallel I/O Pins

General Description

The 'F299 is an 8-bit universal shift/storage register with 3-STATE outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs, Q_0-Q_7 , are provided to allow easy serial cascading. A separate active LOW Master Reset is used to reset the register.

Features

- Common parallel I/O for reduced pin count
- Additional serial inputs and outputs for expansion
- Four operating modes: shift left, shift right, load and store
- 3-STATE outputs for bus-oriented applications
- Guaranteed 4000V minimum ESD protection

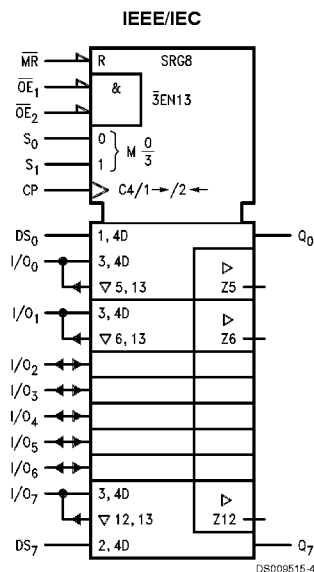
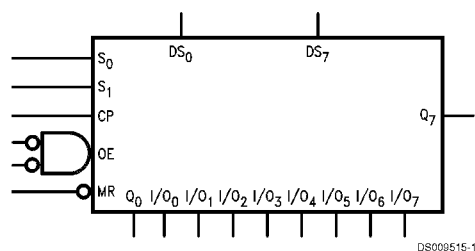
Ordering Code:

Commercial	Military	Package Number	Package Description
74F299PC		N20A	20-Lead (0.300" Wide) Molded Dual-In-Line
	54F299DM (Note 2)	J20A	20-Lead Ceramic Dual-In-Line
74F299SC (Note 1)		M20B	20-Lead (0.300" Wide) Molded Small Outline, JEDEC
74F299SJ (Note 1)		M20D	20-Lead (0.300" Wide) Molded Small Outline, EIAJ
	54F299FM (Note 2)	W20A	20-Lead Cerpack
	54F299LM (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Note 1: Devices also available in 13" reel. Use suffix = SCX and SJX.

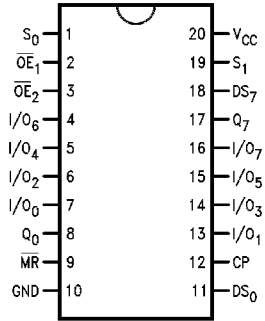
Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.

Logic Symbols

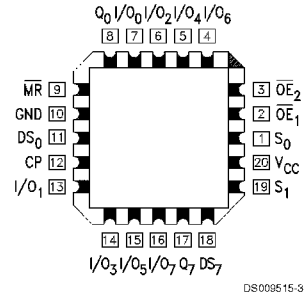


Connection Diagrams

Pin Assignment
for DIP, SOIC and Flatpak



Pin Assignment
for LCC



Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μA /-0.6 mA
DS ₀	Serial Data Input for Right Shift	1.0/1.0	20 μA /-0.6 mA
DS ₇	Serial Data Input for Left Shift	1.0/1.0	20 μA /-0.6 mA
S ₀ , S ₁	Mode Select Inputs	1.0/2.0	20 μA /-1.2 mA
\overline{MR}	Asynchronous Master Reset Input (Active LOW)	1.0/1.0	20 μA /-0.6 mA
\overline{OE}_1 , \overline{OE}_2	3-STATE Output Enable Inputs (Active LOW)	1.0/1.0	20 μA /-0.6 mA
I/O ₀ -I/O ₇	Parallel Data Inputs or 3-STATE Parallel Outputs	3.5/1.083	70 μA /-0.65 mA
Q ₀ , Q ₇	Serial Outputs	150/40(33.3)	-3 mA/24 mA (20 mA)
		50/33.3	-1 mA/20 mA

Functional Description

The 'F299 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous shift left, shift right, parallel load and hold operations. The type of operation is determined by S₀ and S₁, as shown in the Mode Select Table. All flip-flop outputs are brought out through 3-STATE buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q₀ and Q₇ are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on \overline{MR} overrides the Select and CP inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

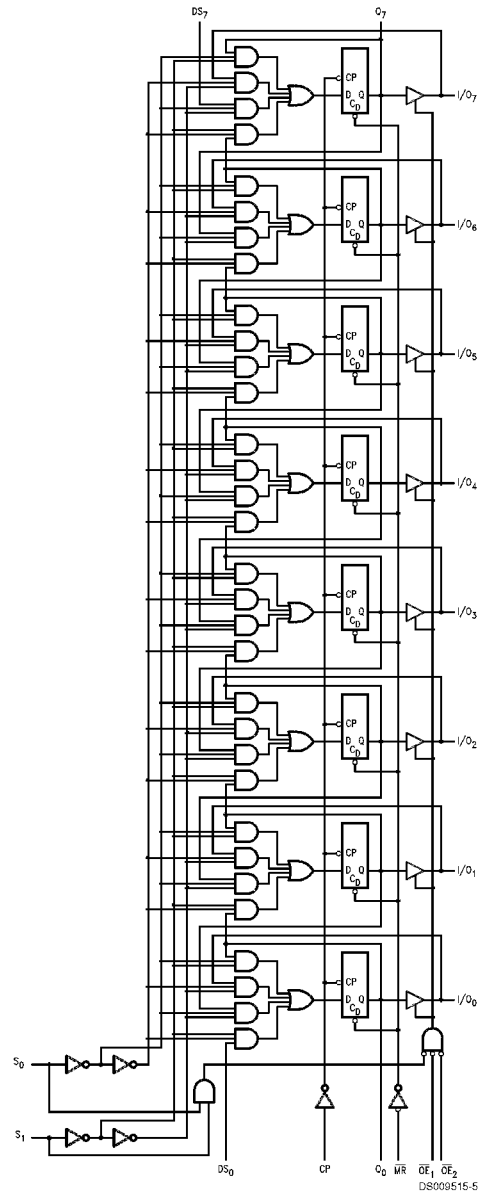
A HIGH signal on either \overline{OE}_1 or \overline{OE}_2 disables the 3-STATE buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The 3-STATE outputs are also disabled by HIGH signals on both S₀ and S₁ in preparation for a parallel load operation.

Mode Select Table

Inputs				Response
\overline{MR}	S ₁	S ₀	CP	
L	X	X	X	Asynchronous Reset; Q ₀ -Q ₇ = LOW
H	H	H	↗	Parallel Load; I/O _n → Q _n
H	L	H	↗	Shift Right; DS ₀ → Q ₀ , Q ₀ → Q ₁ , etc.
H	H	L	↗	Shift Left; DS ₇ → Q ₇ , Q ₇ → Q ₆ , etc.
H	L	L	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↗ = LOW-to-HIGH Clock Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 3)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
Plastic	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 4)	-0.5V to +7.0V
Input Current (Note 4)	-30 mA to +5.0 mA
ESD Last Passing Voltage (Min)	4000V
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	-0.5V to V _{CC}
Standard Output 3-STATE Output	
Current Applied to Output	-0.5V to +5.5V

in LOW State (Max)

twice the rated I_{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

Note 3: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 4: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		54F/74F			Units	V _{CC}	Conditions
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage		0.8			V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage		-1.2			V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54F 10% V _{CC}	2.5			V	Min	I _{OH} = -1 mA (Q ₀ , Q ₇ , I/O _n) I _{OH} = -3 mA (I/O _n)
		54F 10% V _{CC}	2.4					
		74F 10% V _{CC}	2.5					
		74F 10% V _{CC}	2.4					
		74F 5% V _{CC}	2.7					
74F 5% V _{CC}	2.7			I _{OH} = -1 mA (Q ₀ , Q ₇ , I/O _n) I _{OH} = -3 mA (I/O _n)				
V _{OL}	Output LOW Voltage	54 10% V _{CC}	0.5			V	Min	I _{OL} = 20 mA I _{OL} = 20 mA (Q ₀ , Q ₇) I _{OL} = 24 mA (I/O _n)
		74 10% V _{CC}	0.5					
		74 10% V _{CC}	0.5					
I _{IH}	Input HIGH Current	54F	20.0			μA	Max	V _{IN} = 2.7V (CP, DS ₀ , DS ₇ , S ₀ , S ₁ , MR, OE ₁ , OE ₂)
		74F	5.0					
I _{BVI}	Input HIGH Current Breakdown Test	54F	100			μA	Max	V _{IN} = 7.0V (CP, DS ₀ , DS ₇ , S ₀ , S ₁ , MR, OE ₁ , OE ₂)
		74F	7.0					
I _{BVIT}	Input HIGH Current Breakdown Test (I/O)	54F	1.0			mA	Max	V _{IN} = 5.5V (I/O _n)
		74F	0.5					
I _{OEX}	Output HIGH Leakage Current	54F	250			μA	Max	V _{OUT} = V _{CC}
		74F	50					
V _{ID}	Input Leakage Test	74F	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current	74F	3.75			μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current			-0.6	mA	Max	V _{IN} = 0.5V (CP, DS ₀ , DS ₇ , MR, OE ₁ , OE ₂) V _{IN} = 0.5V (S ₀ , S ₁)	
				-1.2				
I _{IH+}	Output Leakage Current			70	μA	Max	V _{I/O} = 2.7V (I/O _n)	
I _{OZH}								
I _{IL+}	Output Leakage Current			-650	μA	Max	V _{I/O} = 0.5V (I/O _n)	
I _{OZL}								

DC Electrical Characteristics (Continued)

Symbol	Parameter	54F/74F			Units	V _{CC}	Conditions
		Min	Typ	Max			
I _{OS}	Output Short-Circuit Current	-60		-150	mA	Max	V _{OUT} = 0V
I _{ZZ}	Bus Drainage Test			500	μA	0.0V	V _{OUT} = 5.25V
I _{CCH}	Power Supply Current	68	95		mA	Max	V _O = HIGH
I _{CCL}	Power Supply Current	68	95		mA	Max	V _O = LOW
I _{CCZ}	Power Supply Current	68	95		mA	Max	V _O = HIGH Z

AC Electrical Characteristics

Symbol	Parameter	74F			54F		74F		Units
		T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A , V _{CC} = Mil C _L = 50 pF		T _A , V _{CC} = Com C _L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
f _{max}	Maximum Input Frequency	70	100		85		70		MHz
t _{PLH}	Propagation Delay	4.0	7.0	8.0	4.0	9.0	4.0	8.5	ns
t _{PHL}	CP to Q ₀ or Q ₇	4.5	6.5	8.0	4.5	9.5	4.5	8.5	
t _{PLH}	Propagation Delay	3.5	7.0	9.0	3.5	10.0	3.5	10.0	ns
t _{PHL}	CP to I/O _n	4.0	8.5	9.0	4.0	11.0	4.0	10.0	
t _{PHL}	Propagation Delay	5.5	7.5	9.5	5.5	12.5	5.5	10.5	ns
t _{PHL}	MR to Q ₀ or Q ₇								
t _{PHL}	Propagation Delay	5.5	11.0	10.0	5.5	12.0	5.5	10.5	ns
t _{PHL}	MR to I/O _n								
t _{PZH}	Output Enable Time	3.5	6.0	8.0	3.0	9.5	3.5	9.0	ns
t _{PZL}	\overline{OE} to I/O _n	4.0	7.0	10.0	4.0	13.0	4.0	11.0	
t _{PHZ}	Output Disable Time	2.0	4.5	6.0	1.5	7.0	2.0	7.0	ns
t _{PLZ}	\overline{OE} to I/O _n	1.0	4.0	5.5	1.0	6.5	1.0	6.5	
t _{PZH}	Output Enable Time	3.5		9.0	3.0	10.5	3.5	10.0	ns
t _{PZL}	S _n to I/O _n	4.0		10.0	4.0	13.0	4.0	11.0	
t _{PHZ}	Output Disable Time	2.5		6.0	1.5	7.0	2.5	7.0	ns
t _{PLZ}	S _n to I/O _n	1.5		5.5	1.0	6.5	1.5	6.5	

AC Operating Requirements

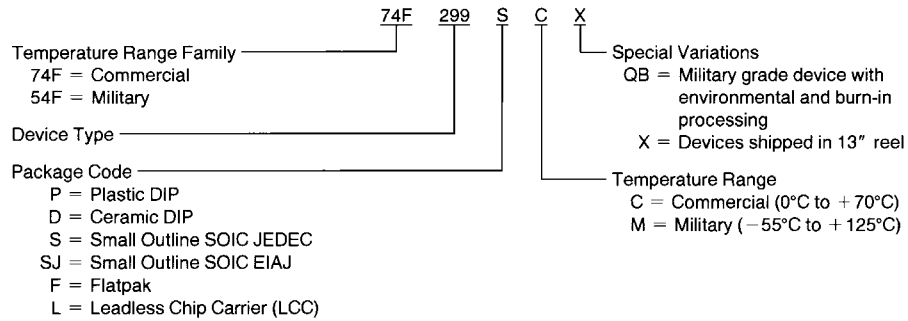
Symbol	Parameter	74F		54F		74F		Units
		T _A = +25°C V _{CC} = +5.0V		T _A , V _{CC} = Mil		T _A , V _{CC} = Com		
		Min	Max	Min	Max	Min	Max	
t _s (H)	Setup Time, HIGH or LOW	8.5		10.0		8.5		ns
t _s (L)	S ₀ or S ₁ to CP	8.5		7.5		8.5		
t _h (H)	Hold Time, HIGH or LOW	0		0		0		ns
t _h (L)	S ₀ or S ₁ to CP	0		0		0		
t _s (H)	Setup Time, HIGH or LOW	5.0		5.0		5.0		ns
t _s (L)	I/O _n , DS ₀ or DS ₇ to CP	5.0		5.0		5.0		
t _h (H)	Hold Time, HIGH or LOW	2.0		2.0		2.0		ns
t _h (L)	I/O _n , DS ₀ or DS ₇ to CP	2.0		2.0		2.0		

AC Operating Requirements (Continued)

Symbol	Parameter	74F		54F		74F		Units
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$		
		Min	Max	Min	Max	Min	Max	
$t_w(\text{H})$	CP Pulse Width	5.0		5.0		5.0		ns
$t_w(\text{L})$	HIGH or LOW	5.0		5.0		5.0		ns
$t_w(\text{L})$	$\overline{\text{MR}}$ Pulse Width, LOW	5.0		6.0		5.0		ns
t_{rec}	Recovery Time, $\overline{\text{MR}}$ to CP	7.0		12.0		7.0		ns

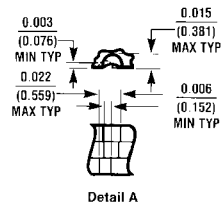
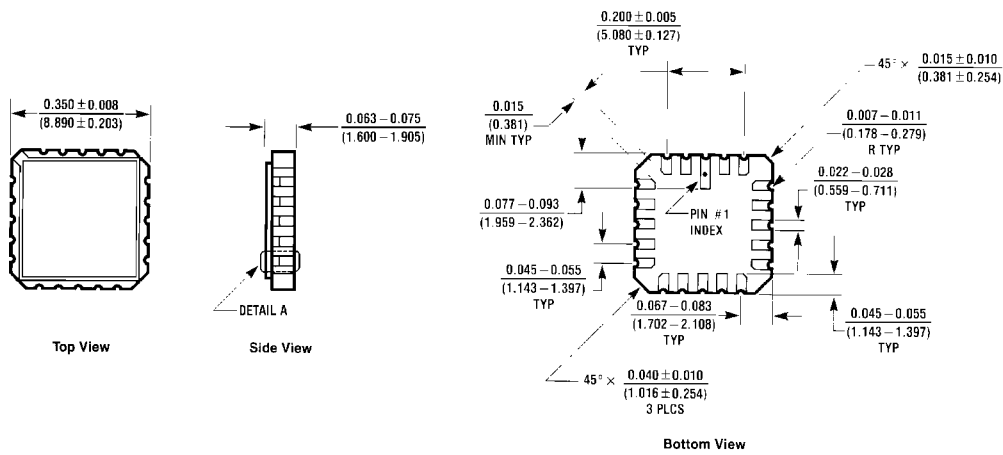
Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

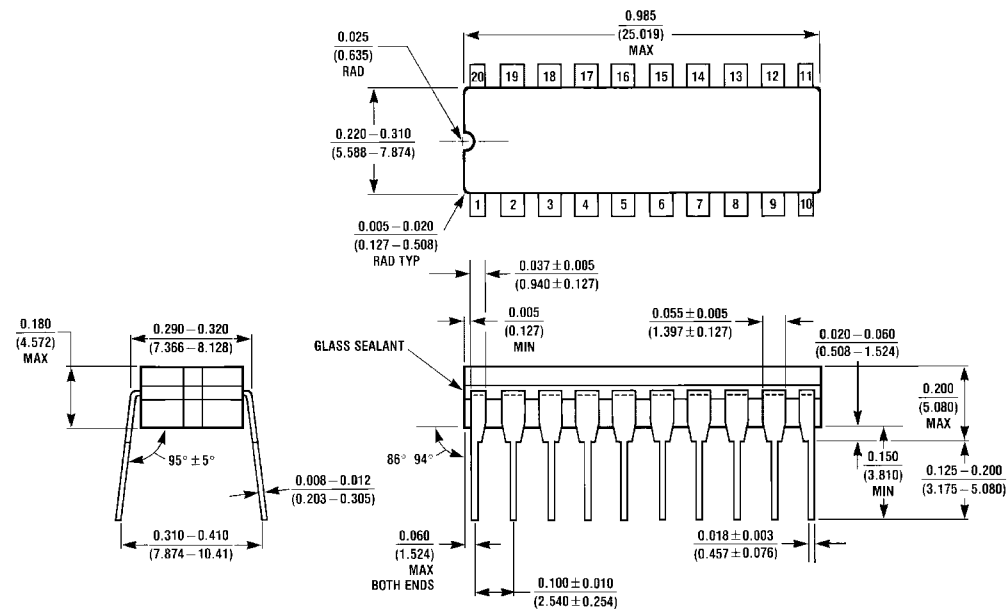


DS009515-6

Physical Dimensions inches (millimeters) unless otherwise noted

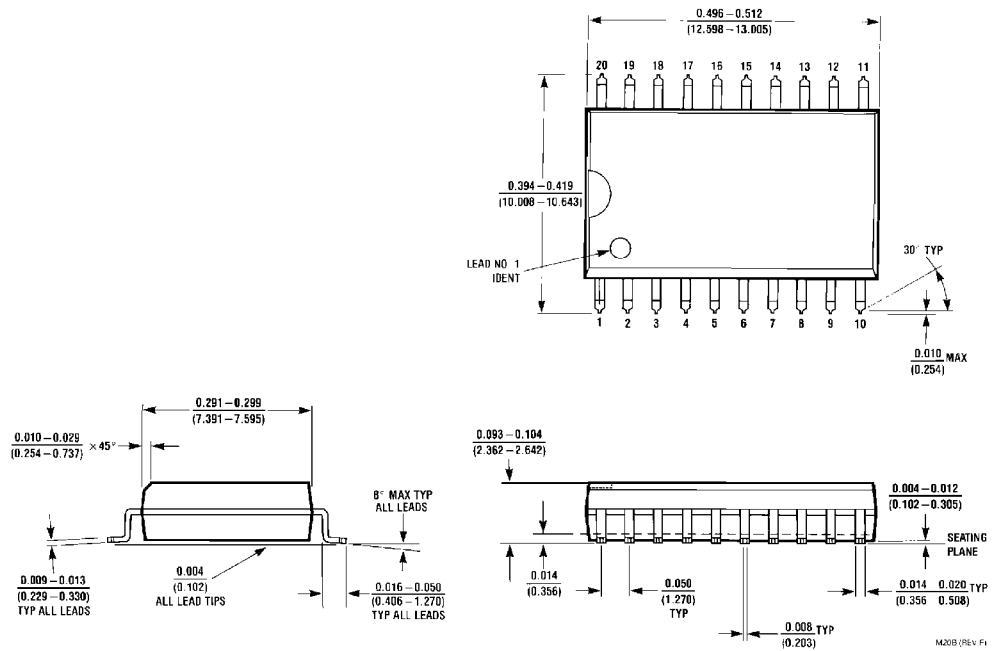


**20-Lead Ceramic Leadless Chip Carrier (L)
Package Number E20A**



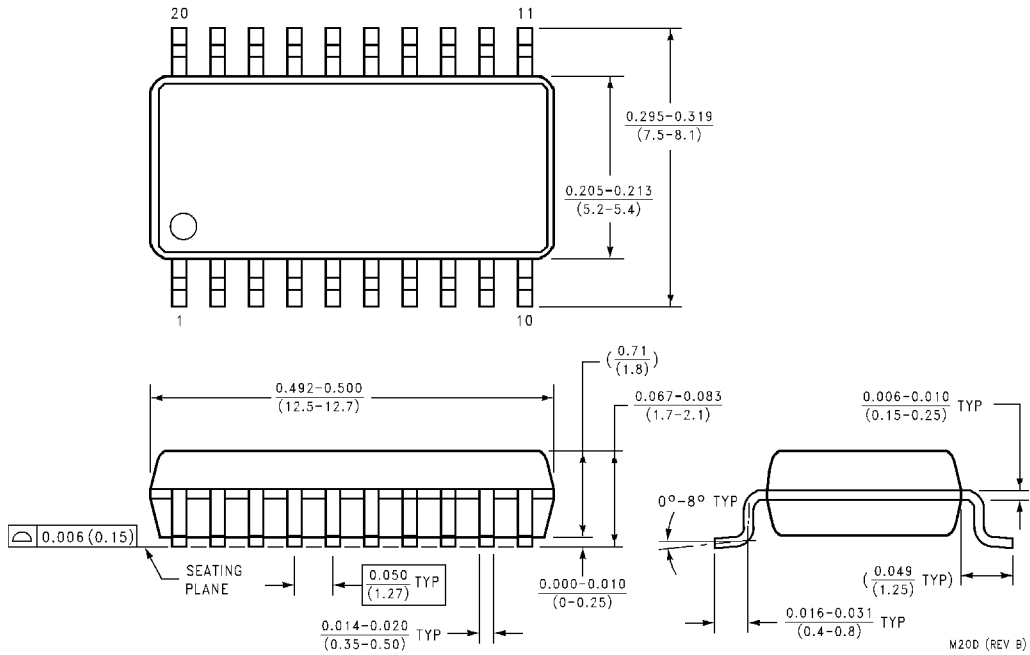
**20-Lead Ceramic Dual-In-Line Package (D)
Package Number J20A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

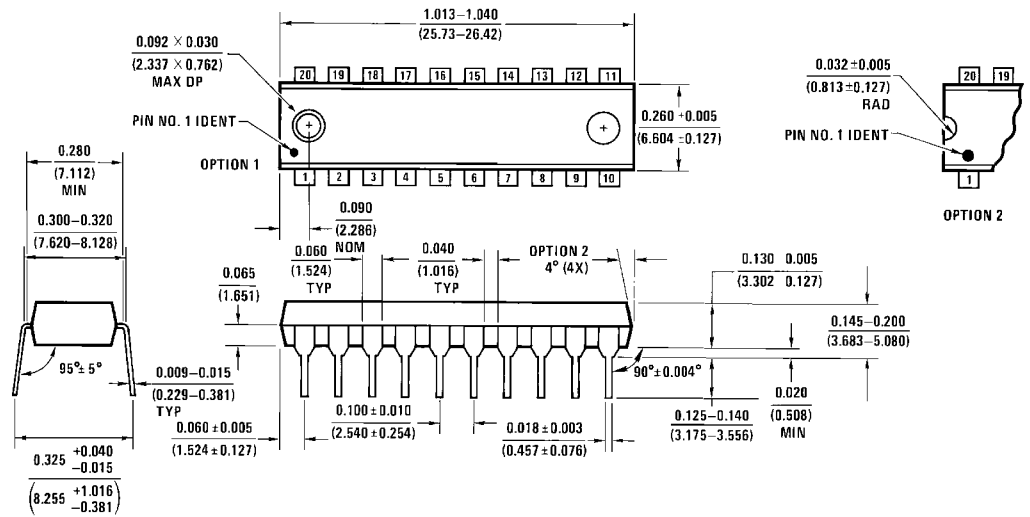


**20-Lead (0.300" Wide) Molded Small Outline Package, JEDEC (S)
Package Number M20B**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

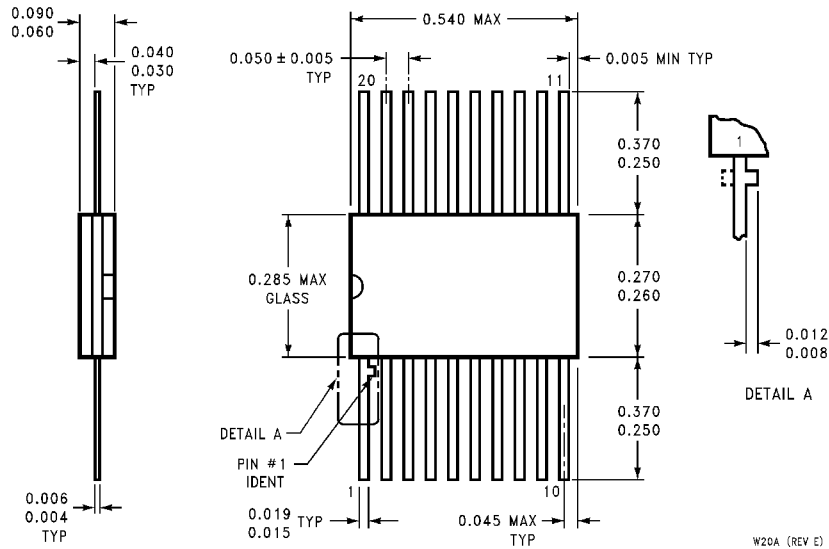


**20-Lead (0.300" Wide) Molded Small Outline Package, EIAJ (SJ)
Package Number MD20D**



**20-Lead (0.300" Wide) Molded Dual-In-Line Package (P)
Package Number N20A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**20-Lead Cerpack
Package Number W20A**

W20A (REV E)

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