FAIRCHILD SEMICONDUCTOR®

October 2009

FMS6400-1
Dual-Channel Video Driver with Integrated Filters and Composite Video Summer

Features

- 5.0 MHz 5th-Order Y, C filters with Composite Summer
- Selectable 0dB or 6dB Gain
- 50dB Stop-Band Attenuation at 27MHz on Y, C, and CV Outputs
- No External Frequency Selection Components or Clocks
- AC-Coupled Inputs
- AC-or DC-Coupled Outputs
- Continuous Time Low-Pass Filters
- 0.4% / 0.4° Differential Gain/Phase on Y, C, and CV Channels
- Integrated DC-Restore Circuitry with Low Tilt
- Lead (Pb) Free SOIC-8 Package

Description

The FMS6400-1 is a dual Y/C 5th-order Butterworth low-pass video filter optimized for minimum overshoot and flat group delay. The device contains a summing circuit to generate filtered composite video. In a typical application, the Y and C input signals from DACs are AC coupled into the filters. Both channels have DC-restore circuitry to clamp the DC input levels during video sync. The Y and C channels use separate feedback clamps. The clamp pulse is derived from the Y channel.

All outputs are capable of driving $2V_{PP}$, AC or DC coupled, into either a single or dual video load. A single video load consists of a series-75Ω impedance-matching resistor connected to a terminated 75Ω line. This presents a total of 150Ω of loading to the part. A dual load is two of these in parallel, which presents a total of 75Ω to the part. The gain of the Y, C, and CV signals can be selected for 0dB or 6dB with $1V_{PP}$ input levels. All video channels are clamped during sync to establish the appropriate output voltage reference levels.

Applications

- Cable Set-Top Boxes
- Satellite Set-Top Boxes
- DVD Players
- Personal Video Recorders (PVR)
- Video On Demand (VOD)

Related Applications Notes

- *AN-6041 PCB Layout Considerations for Video Filter / Drivers*

Ordering Information

Part Number	Operating Temperature Range	Eco Status	Package	Packing Method
FMS64001CS1X	0°C to +70°C	RoHS	8-Lead, Small-Outline Integrated Circuit (SOIC)	2500 Reel

For Fairchild's definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Block Diagram

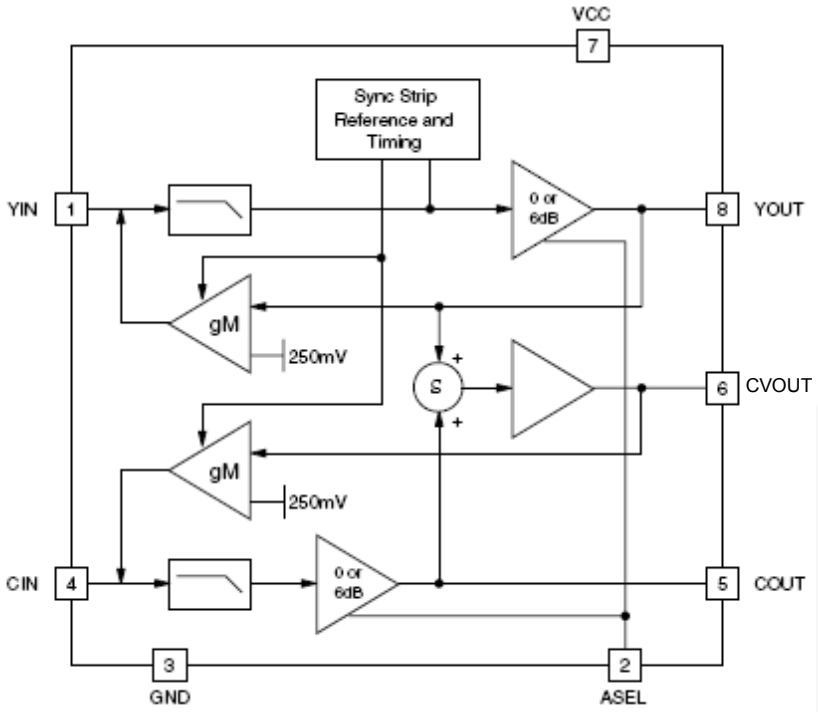

Figure 1. Block Diagram

Typical Application Diagram

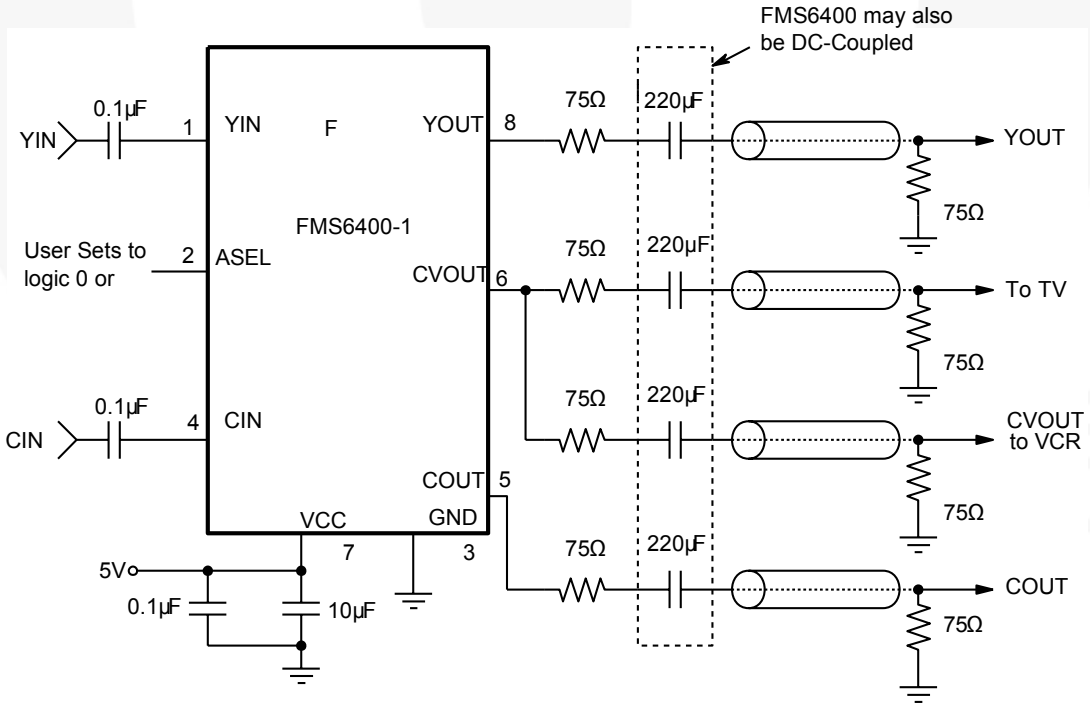

Figure 2. AC-or DC-Coupled Application Diagram

Pin Configurations

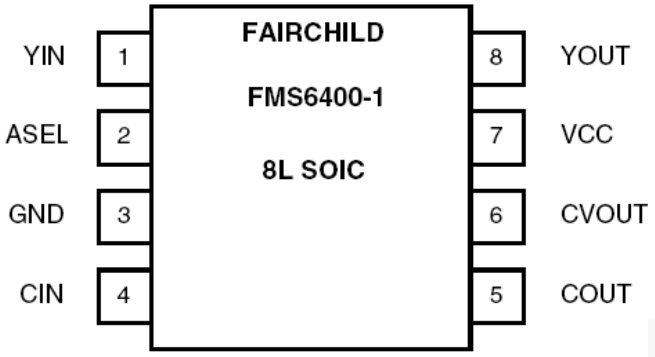

Figure 3. FMS6400 SOIC-8

Pin Definitions

Pin #	Name	Type	Description
1	YIN	Input	Liminance (Luma) input. In a typical system, this pin is connected to the Luma or composite video output pin from the external video encoder.
2	ASEL	Input	Channel gain select. “0” = -0dB, “1” = 6dB.
3	GND	Input	Must be tied to ground.
4	CIN	Input	Chrominance (Chroma) input. In a typical system, this pin is connected to the Chroma output pin from the external video encoder.
5	COUT	Output	Filtered chrominance video output from the C_{IN} channel.
6	CVOUT	Output	Composite video output. This pin is the sum of Y_{OUT} and C_{OUT}.
7	VCC	Inputs	+5V Supply
8	YOUT	Output	Filtered luminance output from the Y_{IN} channel.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	DC Supply Voltage	-0.3	6.0	V
V_{IO}	Analog and Digital I/O	-0.3	V_{CC} +0.3	V
I_{OUT}	Output Current Any One Channel, Do Not Exceed		40	mA

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_A	Operating Temperature Range	0		+70	°C
V_{CC}	Supply Voltage Range	4.75	5.00	5.25	V

ESD Information

Symbol	Parameter	Value	Unit
ESD	Human Body Model, JESD22-A114	8	kV
	Charged Device Model, JESD22-C101	2	

Reliability Information

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_J	Junction Temperature			+150	°C
T_{STG}	Storage Temperature Range	-65		+150	°C
T_L	Lead Temperature (Soldering, 10 seconds)			300	°C
Θ_{JA}	Thermal Resistance (JEDEC Standard Multi-Layer Test Boards, Still Air)		115		°C/W

DC Specifications

T_A = 25°C, V_{CC} = 5.0V, V_{IN} = 1V_{PP}, ASEL = 1 (6dB gain); all input is AC coupled with 0.1µF; all output is AC coupled with 220µF into a 150Ω load; referenced to 400kHz, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current(1)	No Load		50	65	mA
V_{IN}	Input Voltage Maximum			1.4		V_{PP}
PSRR	Power Supply Rejection Ratio	All Channels DC		50		dB

Note:
1. 100% tested at 25°C.

AC Electrical Specifications

T_A = 25°C, V_{CC} = 5.0V, V_{IN} = 1V_{PP}, ASEL = 1 (6dB gain); all input is AC coupled with 0.1µF; all output is AC coupled with 220µF into a 150Ω load; referenced to 400kHz, unless otherwise noted.

Symbol	Parameter		Conditions	Min.	Typ.	Max.	Unit
AV_{0dB}	Channel Gain(2)		All Channel, ASEL = 0	-0.25	0	0.25	dB
AV_{6dB}	Channel Gain(2)		All Channel, ASEL = 1	5.75	6.00	6.25	dB
C_{SYNC}	C_{OUT} Output Level (During Sync)(2)		Sync Present on Y_{IN} (after 6dB Gain)	0.80	1.00	1.30	V
Y_{SYNC}	Y_{OUT} Output Level (During Sync)(2)			0.20	0.35	0.50	
CV_{SYNC}	CV_{OUT} Output Level (During Sync)(2)			0.20	0.35	0.50	
t_{CLAMP}	Clamp Response Time (Y Channel)		Settled to within 10mV		10		ms
f_{Flat}	Gain Flatness to 2.4MHz		All Channels		-0.05		dB
f_C	-3dB Bandwidth(2)		All Channels	4.1	5.1		MHz
f_{SB}	Stopband Attenuation(2)		All Channels at 27MHz	37	52		dB
dG	Differential Gain		All Channels		0.4		%
dP	Differential Phase		All Channels		0.4		°
THD	Output Distortion		V_{OUT} = 1.4V_{PP}, 3.58MHz		0.3		%
X_{TALK}	Crosstalk		At 3.58MHz		-45		dB
SNR	Signal-to-Noise Ratio	Y, C Channel	NTC-7 weighting; 4.2MHz LP, 100kHz HP		75		dB
		CV Channel			70		
t_{pd}	Propagation Delay		All Channels		136		ns
GD	Group Delay Deviation		All Channels at 3.58MHz		10		ns
t_{SKEW}	Skew Between Y_{OUT} and C_{OUT}		At 1MHz		0		ns
t_{CLGCV}	Chroma-Luma Gain CV_{OUT}(2)		f = 3.58MHz (referenced to Y_{IN} at 400KHz)	94	100	104	%
t_{CLDCV}	Chroma-Luma Delay CV_{OUT}				10		ns

Note:
2. 100% tested at 25°C,

Application Information

Functional Description

This product is a two-channel monolithic, continuous-time, video filter designed for reconstructing the luminance and chrominance signals from an S-Video D/A source. Composite video output is generated by summing the Y and C outputs. The chip is designed to have AC-coupled inputs and works equally well with AC- or DC-coupled outputs.

The reconstruction filters provide a 5th-order Butterworth response with group delay equalization. This provides a maximally flat response in terms of delay and amplitude. Each of the three outputs is capable of driving $2V_{PP}$ into a 75Ω load.

All channels are clamped during the sync interval to set the appropriate minimum output DC level. With this operation, the effective input time constant is greatly reduced, which allows for the use of small low-cost coupling capacitors. The net effect is that the input settles to 10mV in 10ms for any DC shifts present in the input video signal.

In most applications, the input coupling capacitors are 0.1µF. The Y and C inputs typically sink 1µA of current during active video, which normally tilts a horizontal line by 2mV at the Y output. During sync, the clamp restores this leakage current by sourcing an average of 20µA over the clamp interval. Any change in the coupling capacitor values affects the amount of tilt per line. Any reduction in tilt comes with an increase in settling time.

Luminance (Y) I/O

The typical Luma input is driven by either a low-impedance source of $1V_{PP}$ or the output of a 75Ω-terminated line driven by the output of a current DAC. In either case, the input must be capacitively coupled to allow the sync detect and DC restore circuitry to operate properly.

All outputs are capable of driving $2V_{PP}$, AC or DC coupled, into either a single or dual video load. A single video load consists of a series-75Ω, impedance-matching resistor connected to a terminated 75Ω line. This presents a total of 150Ω of loading to the part. A dual load is two of these in parallel, which presents a total of 75Ω to the part.

Channel gain of 0dB on all channels is selected by tying pin 2 to ground. Channel gain of 6dB on all channels is selected by tying pin 2 to V_{CC}. Both gain settings assume standard input video levels of $1V_{PP}$.

Chrominance (C) I/O

The chrominance input can be driven in the same manner as the luminance input, but is typically only a $0.7V_{pp}$ signal. Since the chrominance signal doesn't contain any DC content, the output signal can be AC coupled using as small as a 0.1µF capacitor if DC coupling is not desired.

Composite Video (CV) Output

The composite video output driver is same as the other outputs.

Layout Considerations

General layout and supply bypassing play major roles in high-frequency performance and thermal characteristics. Fairchild offers a demonstration board, FMS6400DEMO, to use as a guide for layout and to aid in device testing and characterization. The FMS6400DEMO is a four-layer board with a full power and ground plane. For optimum results, follow the steps below as a basis for high frequency layout:

- Include 10µF and 0.1µF ceramic bypass capacitors.
- Place the 10µF capacitor within 0.75 inches of the power pin.
- Place the 0.1µF capacitor within 0.1 inches of the power pin.
- If using DC-coupled outputs, use a large ground plane to help dissipate heat.
- Minimize all trace lengths to reduce series inductances.

Output Considerations

The FMS6400-1 outputs are DC offset from the input by 150mV. Therefore, $V_{OUT} = 2*V_{IN}$ DC+150mV. This offset is required to obtain optimal performance from the output driver and is held at the minimum value to decrease the standing DC current into the load. Since the FMS6400-1 has a 2x (6dB) gain, the output is typically connected via a 75Ω-series back-matching resistor, followed by the 75Ω video cable. Due to the inherent divide by two of this configuration, the blanking level at the load of the video signal is always less then 1V. When AC-coupling the output, ensure that the coupling capacitor of choice passes the lowest frequency content in the video signal and that line time distortion (video tilt) is kept as low as possible.

The selection of the coupling capacitor is a function of the subsequent circuit input impedance and the leakage current of the input being driven. To obtain the highest quality output video signal, the series termination resistor must be placed as close to the output pin as possible. This greatly reduces the parasitic capacitance and inductance effect on the output driver. The distance from the device pin to the series termination resistor should be no greater than 0.1 inches.

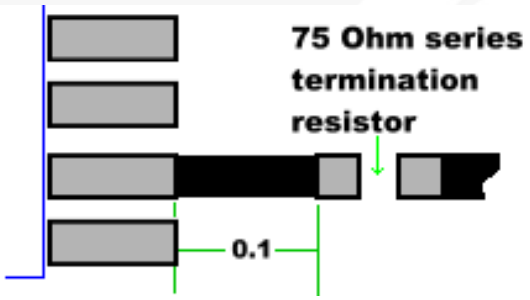

Figure 4. Distance from Device Pin to Series Termination Resistor

Physical Dimensions

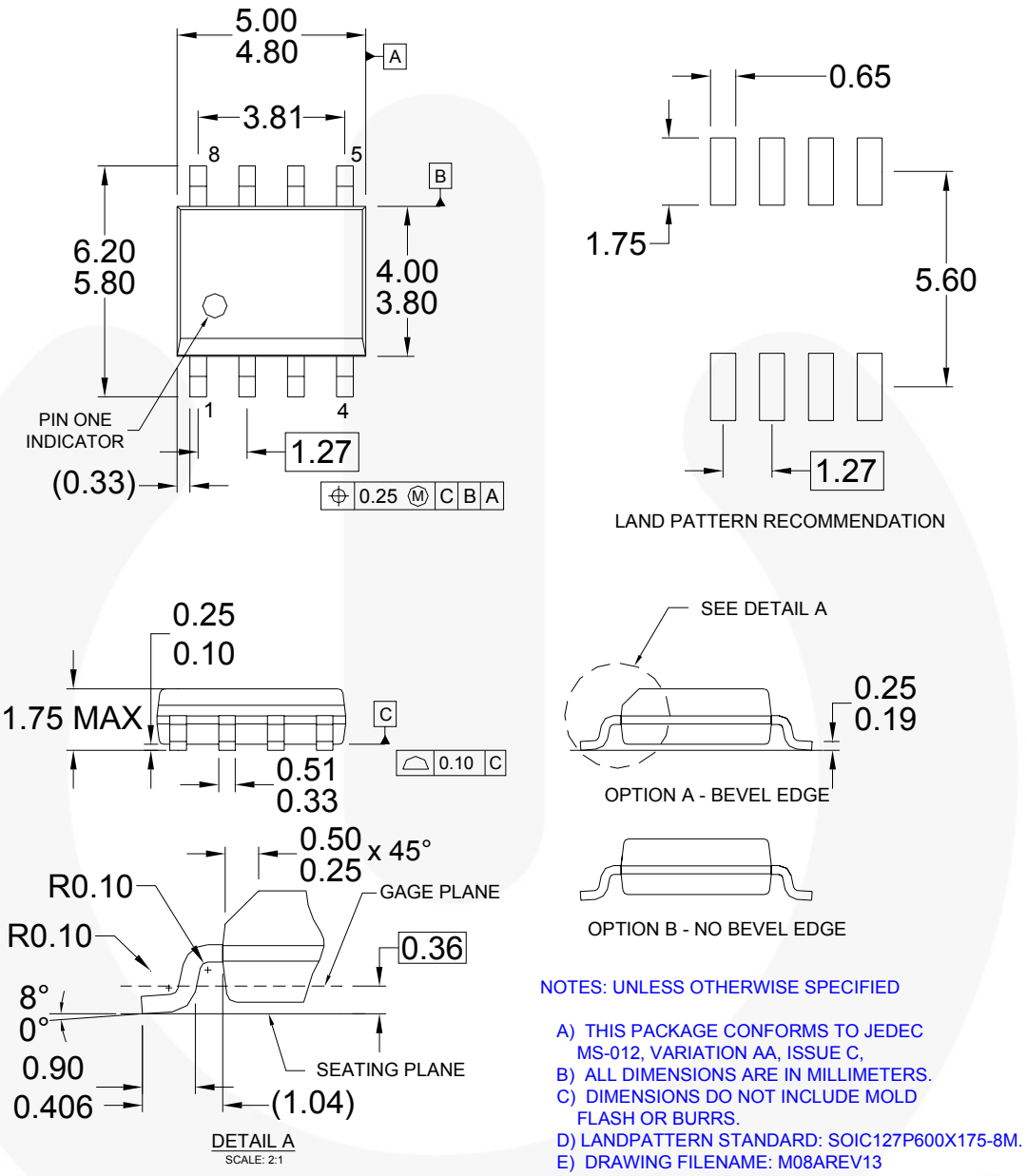

Figure 5. 8- Lead Small Outline Integrated Circuit (SOIC) Package

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