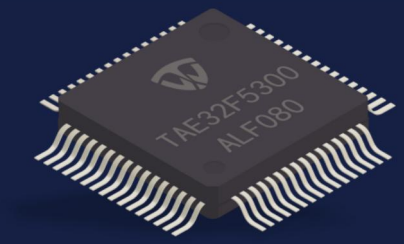
珠海泰为电子有限公司
Zhuhai Tai-Action Electronics CO., LTD.

TAE32F5300 Series



Datasheet

Revision:Rev 1.3
Date:April 18, 2022

Contents

List of tables

List of figures

Features

- Core: ARM Cortex™-M3 32-bit CPU
  - System operating frequency 90MHz
  - Core Built-in 32-bit HW multiplication / division
- ERPU
  - 5 IIRs,support 1/2/3/4 order.
  - ECU calculation unit,RMS Current (Irms) / RMS Voltage (Urms) / Active Power (P) / Reactive Power (Q) / Apparent Power (S) / Power Factor (PF) / Signal Frequency (F) .
- Memories
  - Up to 75Kbytes of Flash memory, support ECC error correction, read/write protection, encryption and zero-delay execution.
  - Up to 16Kbytes Data-FLASH memory
  - Up to 16Kbytes system SRAM and 8Kbytes algorithm SRAM
- Clock management
  - Support single power, voltage range: 3.1V to 3.6V
  - Support power-on/off reset and under-voltage reset
  - Built-in independent watchdog (IWDG) and window watchdog (WWDG)
  - High-frequency RC oscillator: 8MHz (full temperature range ±1% accuracy)
  - Supports 6M-26MHz crystal oscillators, supports solutions without crystals
  - 3 PLLs, support SSC spread spectrum function
  - Clock security system, crystal oscillator abnormal detection circuit and automatic switching
  - Temperature sensor
- DMA
  - 2-channel DMA controller
  - Support arbitrary transfer between memory and peripherals.
- GPIO
  - Support I/O function multiplexing mapping, support bit operation
  - Pull-up/pull-down resistors for all I/Os
  - Supports external interrupt input,supports upper and lower edge triggers, can be used to generate interrupts, event wake-ups, and supports one NMI interrupt
  - 2-speed adjustable drive capacity, maximum 24mA drive capacity
- TIMER
  - 4 channels of 16-bit timers and 4 channels of 32-bit timers
  - Support timing, PWM output and Capture functions
  - Support automatic reload function
- HRPWM
  - The minimum resolution of each PWM output is 195ps
  - Support complementary / independent output mode , support symmetric / asymmetric waveform output
  - Push-pull, dead zone and chopper insertion mechanism,64PIN package supports 6-channel fault and event input,48PIN package supports 6- channel fault and event input, 40PIN package supports 3-channel fault and 6-channel event input,32PIN package supports 3-channel fault and 2-channel event input.Built-in fault and abnormal protection function
  - Support synchronization mechanism between multiple PWM channels
- ADC
  - 2 completely independent high-speed analog -to-digital converters (ADC)
  - Support 2.2MSPS sampling rate, ADC resolution up to 13 bits, effective digits 11 bits
  - Supports 24 analog sampling channels (12 channels for each ADC, each 18 sampling pins)

- Support regular sequence conversion and injection sequence conversion, support gain compensation and offset compensation mechanism
- Support single / discontinuous / continuous sampling mode, support event triggered sampling, support HRPWM synchronous trigger sampling
- ADC reference source, support internal reference voltage

■ DAC/CMP
- 4 DACs and 4 CMPs
- DAC resolution is 12 bits, INL/DNL is less than 5 LSB
- Support sawtooth wave and triangle wave output, support direction and amplitude programmable
- CMP conversion delay is 15ns/18ns/21ns at minimum/typical/maximum

■ Communication Interface
- 2 UARTs interface, support RS485 communication
- 2 I2Cs interface, support SMBus
- One CAN controller, support CAN2.0B
- One USB interface, support USB2.0 protocol, support full speed mode
- One DALI interface, support Master and Slave mode, support 1.2/2.4/4.8K multiple baud rate

■ Programmable voltage detector (PVD)

■ 128-bit unique ID

■ Two low-power modes: sleep mode and Stop mode

■ Support 2-wire SWD debug interface

■ Junction temperature: -40℃~125℃

■ Package:LQFP64(10*10),LQFP48(7*7),QFN40(6*6), QFN32(5*5)

1 Introduction

This document must be read in conjunction with the TAE32F5300, reference manual available from the website www.tai-action.com.

- The Cortex™-M3 Technical Reference Manual can be downloaded from the following link
- http://infocenter.arm.com/help/topic/com.arm.doc.100165_0201_00_en/arm_cortexm3_processor_trm_100165_0201_00_en.pdf

- The Cortex™-M3 Device General User Guide can be downloaded according to the following link:
- http://infocenter.arm.com/help/topic/com.arm.doc.dui0552a/DUI0552A_cortex_m3_dgug.pdf

2 Description

The TAE32F5300 incorporates the high-performance ARM Cortex™-M3 32-bit RISC core operating at up to 90 MHz frequency, high-speed embedded memories (up to 75Kbytes of Flash memory, up to 24Kbytes of SRAM), and an extensive range of enhanced I/Os and peripherals connected to one AHB bus and two APB buses.

The TAE32F5300 offer two fast 11-bit ADCs (2.2Msps),up to four comparators,four DAC channels, four general-purpose 32-bit timer,and four general-purpose 16-bit timers.It also feature standard and advanced communication interfaces: two UART,two I2C, one CAN,one USB and one DALI.

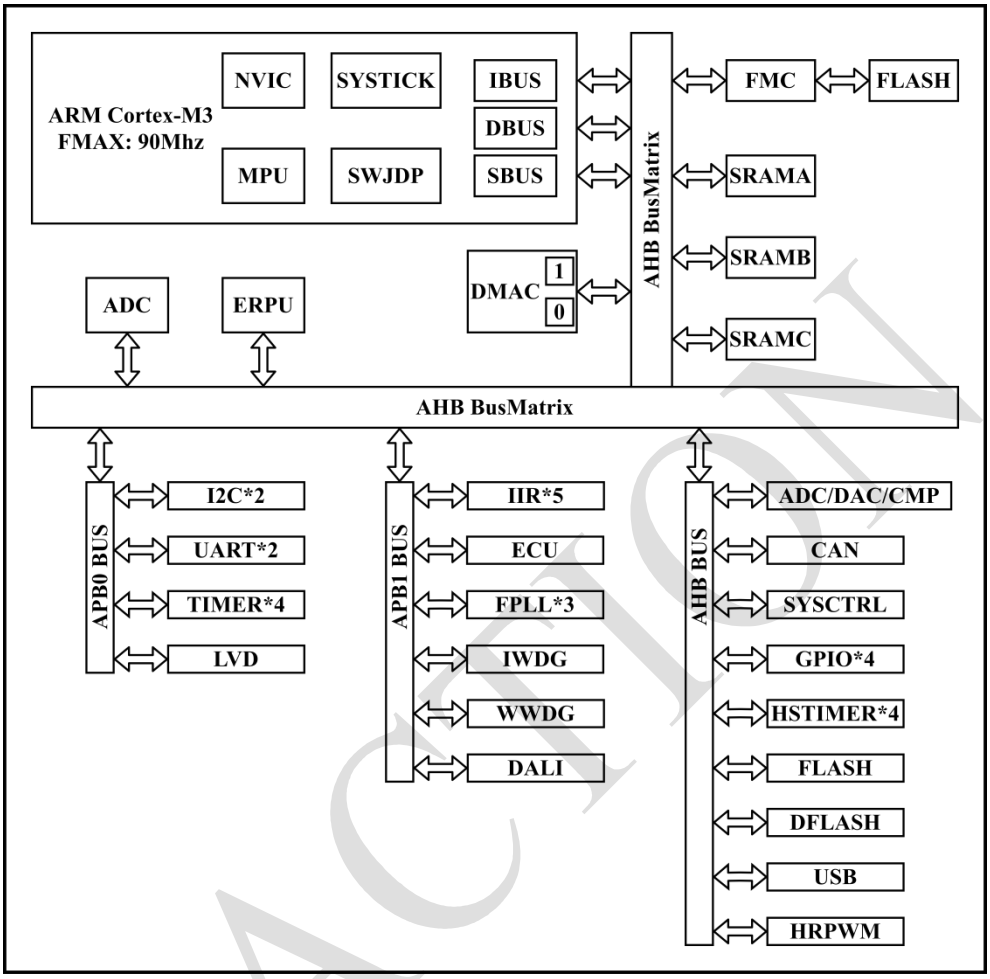
The TAE32F5300 operates in the –40 to +125 °C temperature ranges from 3.1 to 3.6 V power supply.

The TAE32F5300 offers devices in 32-pin,40-pin,48pin and 64-pin packages.

Table 1. TAE32F5300 device features and peripheral counts

Peripheral		TAE32F5300 AQC128	TAE32F5300 AWD128	TAE32F5300 ALD128	TAE32F5300 AEF128
Flash memory (Kbytes)		75	75	75	75
System SRAM (Kbytes)		16	16	16	16
Algorithm SRAM		8	8	8	8
Timer	Timer	8	8	8	8
	SysTick timer	1	1	1	1
	Watchdog(independent, window)	2	2	2	2
Comm. interfaces	HRPWM	4	5	4	6
	UART	2	2	2	2
	I2C	2	2	2	2
	CAN	1	1	1	1
	USB	0	1	1	1
	DALI	1	1	1	1
GPIO	Normal I/Os	22	30	33	49
DMA channels		2	2	2	2
ADC channels		9	11	11	22
DAC channels		3	4	3	4
Ultra-fast analog comparator		3	3	3	4
CPU frequency		90Mhz			
Operating voltage		3.1 to 3.6 V			
Operating temperature		Ambient operating temperature: - 40 to 105 °C Junction temperature: - 40 to 125 °C			
Package		QFN 32L	WQFN 40L	LQFP 48L	eLQFP 64L

Figure 1. TAE32F5300 block diagram



3 Functional overview

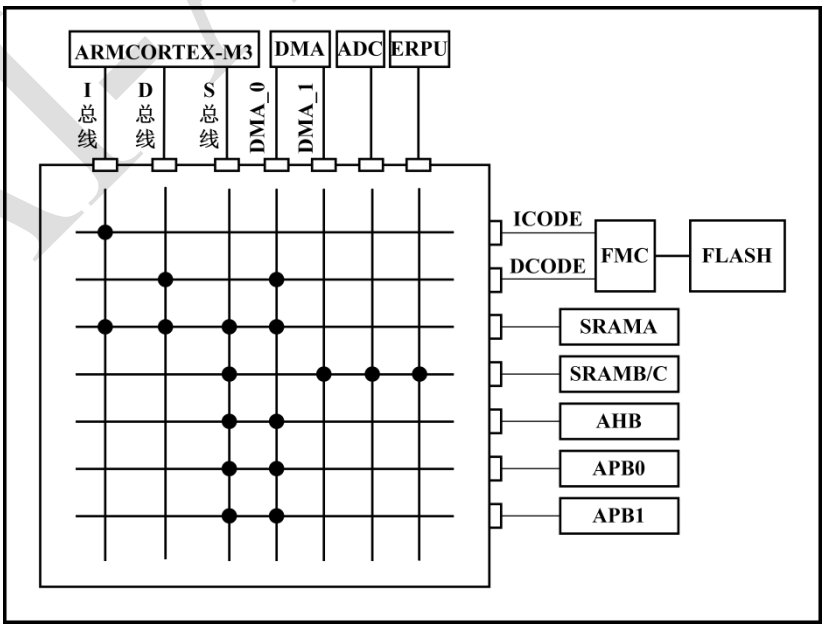
3.1 Interconnect matrix

Main system is composed of a 32-bit multi-layer AHB bus matrix.It can realize the interconnection of the following parts:

- Five Master Bus:
  - Cortex™-M3 core I Bus、D Bus 和 S Bus
  - DMA 0
  - DMA 1
- Eight Controlled Bus:
  - FLASH ICode
  - FLASH DCode
  - SRAMA(16KB)
  - SRAMB(4KB) (used for ADC and ERPU data)
  - SRAMC(4KB) (used for ADC and ERPU data)
  - AHB
  - APB0
  - APB1

Through the bus matrix,the access from the master bus to the controlled bus can be realized.Even when multiple high-speed peripherals are running at the same time,the system can achieve concurrent access and efficient operation.This architecture is shown in Figure 2.

Figure 2. System Bus interconnection matrix



I Bus: This bus is used to connect the instruction bus of the Cortex™-M3 core to the bus matrix, and the core obtains instructions through this bus. The object accessed by this bus is the memory

containing the code (internal FLASH/SRAM).

D bus: This bus is used to connect the Cortex™-M3 data bus to the bus matrix, and the core performs immediate data loading and debugging access through this bus. The object accessed by this bus is the memory (internal FLASH/SRAM) containing code or data.

S bus: This bus is used to connect the system bus of the Cortex™-M3 core to the bus matrix. This bus is used to access data located in peripherals or SRAM. You can also get instructions through this bus (lower efficiency than ICode). The object that this bus visits is 16KB, 4KB, 4KB internal SRAM and AHB0 peripheral hardware, APB0 peripheral hardware, APB1 peripheral hardware.

DMA memory bus: This bus is used to connect the DMA memory bus master interface to the bus matrix. DMA uses this bus to carry in and out of memory data. The object of this bus access is the data memory: internal FLASH/SRAM (16KB, 4KB, 4KB).

Bus matrix: The bus matrix is used for access arbitration management between master buses.

AHB/APB bus bridge: Through one AHB and two APB bus bridges (APB0/APB1) , a fully synchronized connection between the AHB bus and two APB buses can be realized, so that the peripheral frequency can be flexibly selected.

3.2 Memories

3.2.1 FLASH

The Embedded FLASH Controller interface is used to manage the CPU's access to Embedded FLASH through I-Code Bus and D-Code Bus. The Embedded FLASH Controller can perform erasing and programming operations on the FLASH memory bank, implement a read/write protection mechanism for the FLASH memory bank, and realize the data encryption/decryption function of the FLASH memory bank.

The FLASH structure is as follows:

- The main memory block is divided into multiple sectors.
- System memory, the device starts from this memory in system memory boot mode.
- The option byte is used to configure functions such as read protection, write protection, and encryption.

3.2.2 SRAM

The system SRAM can be accessed in bytes, half words (16 bits) or full words (32 bits). Read and write operations are executed at CPU speed, and the waiting period is 0. The system SRAM is divided into three blocks:

- The SRAMA (16KB) block mapped at address 0x2000 0000, which can be accessed by all AHB master buses.

- The SRAMB (4KB) block mapped at address 0x2000 4000 can be accessed by all AHB master bus, DMA master bus, ADC and ERPU. The AHB main bus supports concurrent SRAM access. For example, when the CPU reads/writes 4KB SRAM, ADC and ERPU can read/write 4KB SRAM at the same time.
- The SRAMC (4KB) block mapped at address 0x2000 5000 can be accessed by all AHB master bus, DMA master bus, ADC and ERPU. The AHB main bus supports concurrent SRAM access. For example, when the CPU reads/writes 4KB SRAM, ADC and ERPU can read/write 4KB SRAM at the same time.
- When BOOT=SRAM, the 16KB SRAMA block is mapped to the starting address of 0x1000 0000
- When BOOT=FLASH, the 16KB SRAMA block is mapped to the starting address of 0x1800 0000

If you choose to boot from SRAM, the CPU can access the system SRAM through the system bus or I-Code/D-Code bus. To obtain the best performance during SRAM execution, physical remapping (through boot pins) should be selected.

3.3 Boot configuration

The memory uses a fixed memory map. The starting address of the code area is 0x0000 0000 (accessed through the ICode/DCode bus), and the starting address of the data area is 0x2000 0000 (accessed through the system bus). The Cortex™-M3 CPU always obtains the reset vector through the I Code bus, which means that only the code area (usually FLASH) can provide boot space. The device implements a special mechanism that can be booted from other memories (such as internal SRAM).

In the device, two different boot modes can be selected through the BOOT pin, as shown in Table 2.

Table 2. Boot modes

Boot pin	Boot mode	Boot memory
0	FLASH	Boot from user Flash memory
1	SRAM	Boot from embedded SRAM

After reset, the value of the BOOT pin is latched on the fourth rising edge of SYSCLK. After reset, the user can select the desired boot mode by setting the BOOT pin.

The BOOT pin will only resample the BOOT pin when the device is powered on again. Therefore, after such a start, the CPU will obtain the top value of the stack from the address 0x0000 0000, and then execute the code from the bootp memory starting at 0x0000 0004.

Note: If the device boots from SRAM, in the application initialization code, it is necessary to use the NVIC program and interrupt vector table and offset register to reallocate the vector table in SRAM.

3.4 Power management

3.4.1 Power supply schemes

The embedded linear voltage regulator supplies power for all digital circuits, and the output voltage of the voltage regulator is approximately 1.5V.

This voltage regulator needs to connect two external capacitors between dedicated pins VDD and VSS. All packages are equipped with VDD pins. The specific pins are related to the package.

The voltage regulator is always in the enabled state after reset. According to the different application modes, the following three different working modes can be selected.

- In operating mode, the voltage regulator provides full power for the 1.5 V domain (core, memory and digital peripherals). In this mode, the output voltage of the voltage regulator can be adjusted to a voltage value of 1.5V through software configuration (PMUCR register) 的位[15:13]).
- In standby mode, the voltage regulator provides low power for the 1.5 V domain (core, memory and digital peripherals), and can retain the contents of registers and internal SRAM. In this mode, the output voltage of the voltage regulator is adjusted to 1.1V through software configuration (bits [15:13] of the PMUCR register).

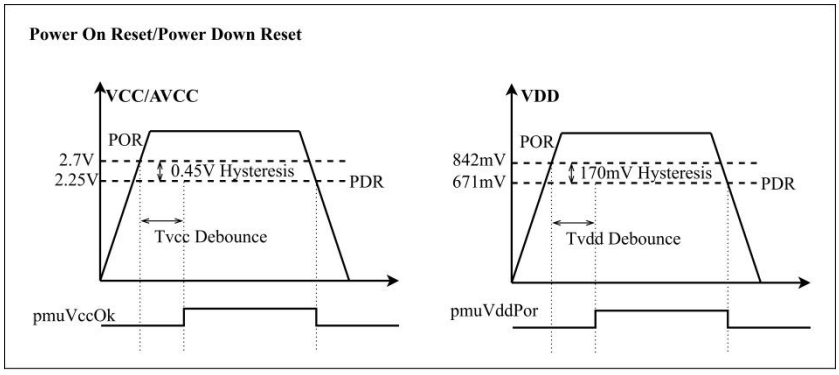
Note: When configuring the VDD bit to 1.1V, pay attention to the configuration related to VDD LVD to prevent mistakenly entering the reset state.

3.4.2 Power-on reset(POR)/Power-down reset(PDR)

The device integrates POR/PDR circuit, which can work normally from 2.8V.

When VCC/AVCC is lower than the specified threshold VPOR/PDR, the device will remain reset without the need for an external reset circuit. For detailed information about the power-on/power-down reset threshold, please refer to the electrical characteristics section.

Figure 3. Power-on reset/power-down reset waveform



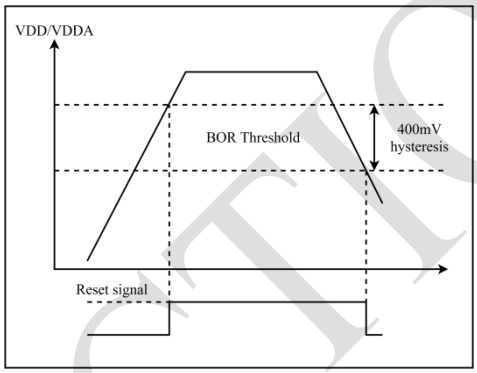
3.4.3 Brown-out reset(BOR)

During power-up,a brown-out reset(BOR) will keep the device in reset until the power supply voltage reaches the specified V_{BOR} threshold.

The default state of BOR is off , and 4 V_{BOR} thresholds can be selected.

- BOR level 0(V_{BOR0}):the reset threshold level of the voltage range from 1.80V to 2.40V.
- BOR level 1(V_{BOR1}):the reset threshold level of the voltage range from 2.40V to 2.55V.
- BOR level 2(V_{BOR2}):the reset threshold level of the voltage range from 2.55V to 2.70V.
- BOR level 3(V_{BOR3}):the reset threshold level of the voltage range from 2.70V to 3.00V.

Figure 4. BOR Threshold



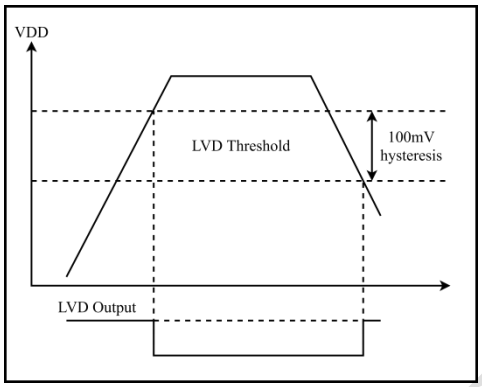
3.4.4 Programmable voltage detector (PVD)

Use the PVD unit to monitor the VCC/VDD power supply voltage, monitor the VCC/VDD low voltage and overcurrent, and compare it with the threshold selected by the voltage threshold control register (LACR) in the PVD low voltage detection module of the device .

VCC/VDD low-voltage and over-current monitoring functions are respectively enabled by setting the Enable of the voltage threshold control register (LACR) in the PVD module to enable the corresponding functions of the PVD.

The power control/status register (LCR) in the PVD unit provides a VCC/VDD undervoltage or overcurrent flag to indicate whether the power supply voltage is less than the PVD threshold or whether the power supply current is greater than the PVD threshold. The event is internally connected to the NMI interrupt. If the interrupt is enabled, a non-maskable interrupt can be generated; the event is internally connected to the system reset, and if the reset is enabled, a system reset can be generated; the event is internally connected to the event system, and the function Usefulness is to perform emergency shutdown tasks under abnormal conditions.

Figure 5. LVD Threshold



3.4.5 Low-power modes

The devic supports two low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- Sleep mode

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- Stop mode

Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.

Reduce the power consumption of the mode by one of the following methods:

- Reduce the system clock speed
- When the APB and AHB peripherals are not used, turn off the corresponding peripheral clock

Table 3. Low-power modes

Mode name	Input	wake up	Impact on VDD	Regulator
Sleep mode	WFI	Interrupt occurs	CPU CLK off has no effect on other clocks or analog clock sources	Open
	WFE	event occurs		
Stop mode	DEEPSLEEP and WFI or WFE	Interrupt occurs	Except the LSI clock, all clocks are stopped	Open

3.5 Clocks and startup

System clock selection is performed on startup, however the internal RC32K oscillator is selected on reset as default CPU clock. An external 6-26MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers allow to configure the AHB frequency, The maximum frequency of the AHB and the two APB domains is 90MHz.

ADC and HRPWM maximum frequency is 160MHz.

3.6 Embedded Flash memory(FLASH)

- Up to 75KB
- Up to 160 sectors, 480 bytes per sector
- Support device/sector erase (Device/Sector Erase)
- LASH can be used as boot code space (selected by BOOT pin) to store and execute user code
- FLASH supports 128-bit wide programming function, supports reading FLASH by byte/halfword/word
- Enhanced security functions
  - FLASH read protection function (RDP)
  - FLASH write protection function (WRP)
  - FLASH storage body is encrypted and stored to realize the protection of user code and realize zero-wait encryption and decryption operations
- FLASH I/D bus 128Bit wide prefetch and cache function
  - 512 Byte cache on FLASH I-Code Bus
  - 256 Byte cache on FLASH D-Code Bus
- Error code correction (ECC), support for error detection
- FLASH low-power mode

3.7 Data FLASH memory(DFLASH)

DFLASH mainly has the following characteristics:

- Up to 18KByte storage space
- DFLASH memory includes 1 main memory area (Main Memory) + 1 secondary memory area (Secondary Memory)
  - The main storage area contains 32 sectors, each sector is 512Byte, totaling 16 KByte
  - The secondary storage area contains 4 sectors, each sector is 512Byte, totaling 2KByte
  - The main storage area supports Sector Erase and Chip Erase
  - The secondary storage area only supports Sector Erase, which is not affected by Chip erase
- Support register mode read/program/erase operation
- 32Bit bus width, supports two operation modes: Byte or Word
- Support lock/unlock protection to avoid data misoperation
- Support Standby/Wakeup to enter/exit low power consumption mode

3.8 Interrupts and events

3.8.1 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller (NVIC) able to handle up to 51 interrupt channels that can be masked and 8 priority levels.
The NVIC benefits are the following:

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved on interrupt entry and restored on interrupt exit with no instruction overhead

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.9 General-purpose inputs/outputs(GPIO)

GPIO mainly has the following characteristics:

- Controlled I/O up to 49
- Output status: push-pull or open-drain + pull-up/pull-down
- Input status: floating, pull-up/pull-down, analog
- Output data from output data registers or peripherals (multiplexed function output)
- Data input to the input data register or peripherals (multiplexed function input)
- Analog function
- Set and reset registers, and have bit-wise write permissions on output data registers
- Optional synchronization function and anti-shake function
- Configurable current drive capability
- Each I/O can independently configure the output Slew Rate and input Hysteresis
- Multiple function input/output selection register
- Multiple function is highly flexible, allowing the I/O pins to be configured as GPIO or various peripheral functions
- All I/Os can be independently configured with external input trigger interrupt enable, rising edge/falling edge/double edge triggering, independent interrupt pending flag

3.10 Timers and Watchdogs

3.10.1 General-purpose timers(TIMER)

The TIMERx (x = 0 ... 7) has the following characteristics:

- 16-bit (TIMER0/1/2/3) or 32-bit (TIMER4/5/6/7) automatic reload increment counter.
- 16-bit (TIMER0/1/2/3) or 32-bit (TIMER4/5/6/7) prescaler, used to prescale the counter clock source. Among them, TIMER0/1/2/3 uses APB0CLK as the clock source, and TIMER4/5/6/7 uses AHB0CLK as the clock source.
- 16-bit (TIMER0/1/2/3) or 32-bit (TIMER4/5/6/7) counting start value and end value registers, which are used to flexibly set the start and end count values of the counter.
- Two working modes:
  - Cyclic mode, automatically reload after counting and continue counting
  - Single-shot mode, automatically turn off the enable of the timer after the count is completed
- Independent channel, which can be used for:
  - Input capture
  - Output comparison
  - PWM generation
  - ETR external trigger input
- Two sets of timer synchronization function
- Interrupts are generated when the following events occur:

- Counter overflow (Overflow Event)
- Update Event (Enable): The counter overflow generates an update event, which can also be generated by software (UG)
- Input capture (Capture Event), repeat capture (Over Capture Event)
- Compare Event

3.10.2 Independent watchdog(IWDG)

IWDG mainly has the following characteristics:

- Free running down counter
- 16-bit reload count value register, count clock supports frequency division from 4 to 512
- The clock is provided by an independent RC oscillator (LSI) (can run independently in standby mode)
- reset is generated when the down counter value reaches 0x0 (if the watchdog is activated)

3.10.3 Window watchdog(WWDG)

WWDG mainly has the following characteristics:

- Free running down counter
- Reset conditions (the WWDG_TIMEOUTRST_EN bit of the SYSCTRL_SYSCFGCR register is 1, allowing the WWDG system to be reset, see DBG module introduction for details)
  - Reset when the down counter value is less than 0x40 (if the watchdog is activated)
  - Reset when the down counter is reloaded outside the window (if the watchdog is activated)
- Early Wake-up Interrupt (EWI): Triggered when the down counter is reduced to 0x4 (if enabled and the watchdog is activated), it can be used to reload the counter in the interrupt to avoid WWDG reset

3.11 Direct memory access(DMA)

- The flexible general-purpose DMA is able to manage memory-to-memory, peripheral-to memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.
- Each of the 2 DMA channels is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.
- The DMA can be used with the main peripherals: I2C, UART.

3.12 Infinite Impulse Response(IIR)

IIR mainly has the following characteristics:

- The order (1-4) is dynamically adjustable
- DISCAL amplification supports 2^16, FBSCAL and DOSCAL support 2^32
- Support shadow register and reload function
- Support internal soft recovery

3.13 Energy Calculation Unit(ECU)

ECU module functions include:

- Provide one-way current and one-way voltage RMS measurement
- Provide active power measurement, and the measurement accuracy meets the following accuracy requirements
  - >50% full load; reach 0.5% accuracy; full load refers to ADC full scale amplitude *90%
  - 30%~50%, reaching 1% accuracy
  - 10%~30%, reach 2.5% accuracy
- Reactive power measurement is provided, and the measurement accuracy meets the following accuracy requirements
  - >50% full load; reach 0.5% accuracy; full load refers to ADC full scale amplitude *90%
  - 30%~50%, reaching 1% accuracy
  - 10%~30%, reach 2.5% accuracy
- Provide measurement of electrical energy parameters such as apparent power, power factor, and fundamental frequency
- Provide gain correction, offset correction, phase correction functions
- Provide independent square root operation function

3.14 Fast analog-to-digital converter(ADC)

- High-performance features
  - 2 ADCs, can run in synchronous mode
  - Each ADC is connected to 11 external channels + 1 internal channel
  - Each ADC supports independent configuration of single-ended/differential input of each channel
  - Each ADC supports independent configuration of the sampling time of each channel
  - Each ADC supports up to 16 regular channels
  - Each ADC supports up to 4 injection channels (analog input is allocated as regular channels or injection channels are fully configurable)
  - Each channel of ADC supports 12 channels of DMA to carry data for regular channels
  - Each ADC supports 4 dedicated data registers for injection channel use
- Oversampler

- Each ADC supports 16-bit data registers, and the number of data bits is up to 16 bits
- Each ADC supports 2~256 times oversampling
- Programmable right shift of each ADC data

- Data preprocessing
  - Each ADC supports gain compensation, up to 4 groups of compensation coefficients
  - Each ADC supports offset compensation, up to 4 groups of compensation coefficients
- Conversion start
  - Each ADC supports regular conversion and injection conversion via software
  - Each ADC supports the start of regular conversion and injection conversion through hardware trigger events (internal timer events or GPIO input events) with configurable polarity
- Conversion mode
  - Each ADC can convert a single channel, or scan a channel sequence
  - Each ADC in single mode converts the selected input once every time it is triggered
  - Each ADC continuously converts the selected input at each trigger in continuous mode
  - Each ADC in discontinuous mode converts the selected input in groups each time it is triggered
  - Each ADC supports interrupt generation when it is ready, conventional/injection conversion end, conventional/injection sequence conversion end, analog watchdog 0/1/2 or data overrun event
- Each ADC supports 3 analog watchdogs, the analog watchdog can filter and ignore data out of range
- ADC input range: GND≤VIN≤3V

3.15 Digital-to-analog converter(DAC)

The main functions of DAC are as follows:

- Four DAC interfaces, each interface corresponds to an output channel
- Support triangle wave generation mode
- Support sawtooth wave generation mode
- Support software trigger conversion
- Support external event trigger conversion

3.16 Comparators(CMP)

- Optional negative analog input
  - I/O pin input (each comparison channel has two pins to choose from)
  - DAC channel output (internal signal)
  - Internally connected to GND
- Programmable hysteresis
- Mapping output to I/O, and output after debounce
- Redirect the output to the timer input used to trigger the following events

  - Capture events
  - Circuit break event (used for fast PWM shutdown)
- Blanking comparator output
- Rising edge and falling edge interrupt

3.17 High precision pulse width modulator(HRPWM)

- Multiple timing units
  - 195 ps resolution, which has been compensated for voltage and temperature changes
  - All outputs support high resolution, and the duty cycle, frequency and pulse width can be adjusted in the trigger single pulse mode
  - 6 16-bit timing units (each timing unit contains an independent counter and 4 comparison units)
  - 12 outputs can be controlled by the timing unit, each channel has up to 18 set/reset sources
  - Modular structure can meet the needs of a variety of independent converters equipped with 1 or 2 switches, and can also meet the needs of a few large-scale multi-switch topologies
- Up to 6 external events, which can be used in any timing unit
  - Programmable polarity and effective edge
  - Fast asynchronous mode
  - Programmable digital filter
  - Use blanking and windowing modes to achieve false event filtering
- Multiple channels can be connected to the built-in analog peripherals
  - 8 trigger events connected to the ADC converter
  - 8 trigger events connected to the DAC converter (triangular wave compensation)
  - 12 trigger events (reset and step) connected to the DAC converter (sawtooth compensation)
- Comprehensive protection mechanism
  - 6 fault inputs can be used in combination and linked to any timing unit
  - Programmable polarity and effective edge
  - Programmable digital filter
- Multiple HRPWM units can be synchronized with external synchronization input/output
- Multi-function output stage
  - High-resolution dead zone insertion
  - Programmable output polarity
  - Chopping mode
- 8 interrupt vectors, each vector has up to 12 sources

3.18 Communication interfaces

3.18.1 Inter-integrated circuit interface (I2C)

- Two-wire I2C serial interface-composed of serial data line (SDA) and serial clock (SCL)
- Two speeds
  - Standard mode (0 to 100 Kb/s)
  - Fast mode (≤400 Kb/s)
- Master or slave I2C operation
- 7-bit or 10-bit addressing
- 7-bit or 10-bit combined format transmission
- transmitting and receiving buffer
- Interrupt or polling mode operation
- Programmable SDA hold time
- Support SMBus/PMBus

3.18.2 Universal Asynchronous Receivers / Transmitters (UART)

- Support 9-bit serial data transmission
- Wrong start bit detection
- Support programmable decimal baud rate
- Support multi-point RS485 interface
- Optional parity bit, stop bit
- 16-bit FIFO depth
- Support interrupt mode
- The programmable serial data baud rate can be calculated by the following formula: baud rate = (serial clock frequency)/(16×divisor)

3.18.3 Controller area network (CAN)

- Support CAN specification
  - CAN 2.0B (up to 8 bytes payload)
- Freely programmable data rate
  - CAN 2.0B defines a data rate up to 1Mbit/s
- Programmable baud rate prescaler (1/2 to 1/256)
- Separate clock domain for CPU interface and CAN module
- Two sending buffers
  - One main transmit buffer (PTB)
  - Optional configurable secondary transmit buffer (STB)
  - The received "not accepted" or "incorrect" message will not overwrite the stored message

- A dual-port storage module for PTB and STB
- Independent programmable internal 29-bit acceptance filter
  - The number of acceptance filters that can be selected for general parameters, ranging from 1 to 16
- Extended functions
  - Single-shot transmission mode (for PTB and/or STB)
  - Listen only mode
  - Loopback mode (internal and external)
  - Transceiver standby mode
- Extended status and error reporting
  - Capture the error that occurred last time
  - Capture the location where the arbitration is lost
  - Programmable error warning limit
- Different host controller interfaces
  - 32-bit synchronous host controller interface; 8-bit host wrapper
  - According to the requirements, the optional application program is specific to the interface of the host controller
- Configurable interrupt source

3.18.4 Universal serial bus(USB)

- USB2.0 protocol, supports full-speed mode (does not support high-speed and low-speed modes)
- There are 3 endpoints including endpoint 0, all of which support RX and TX
- 256 bytes dedicated data packet buffer memory
- Cyclic Redundancy Check (CRC) generation/check, non-return-to-zero inversion (NRZI) encoding/decoding and bit stuffing
- Support control, ISO, interrupt and bulk transmission
- USB insertion/removal detection
- USB suspend/wake up function
- Support DMA, endpoint 1 and endpoint 2 are each equipped with a DMA

3.18.5 Digital addressable lighting interface (DALI)

DALI mainly has the following characteristics:

- Support master mode and slave mode
- Support Manchester encoding and decoding
- Support data bit 16/17/18/24Bit
- Support 1.2K/2.4K/4.8K baud rate
- Support forward frame and backward frame delay parameters can be configured
- Support filtering, filter length can be configured
- Support baud rate fault tolerance, the fault tolerance mechanism is updated at each transition edge
- Support RX, TX polarity can be matched

4 Pinout and pin descriptions

Figure 6. eLQFP64L pinout

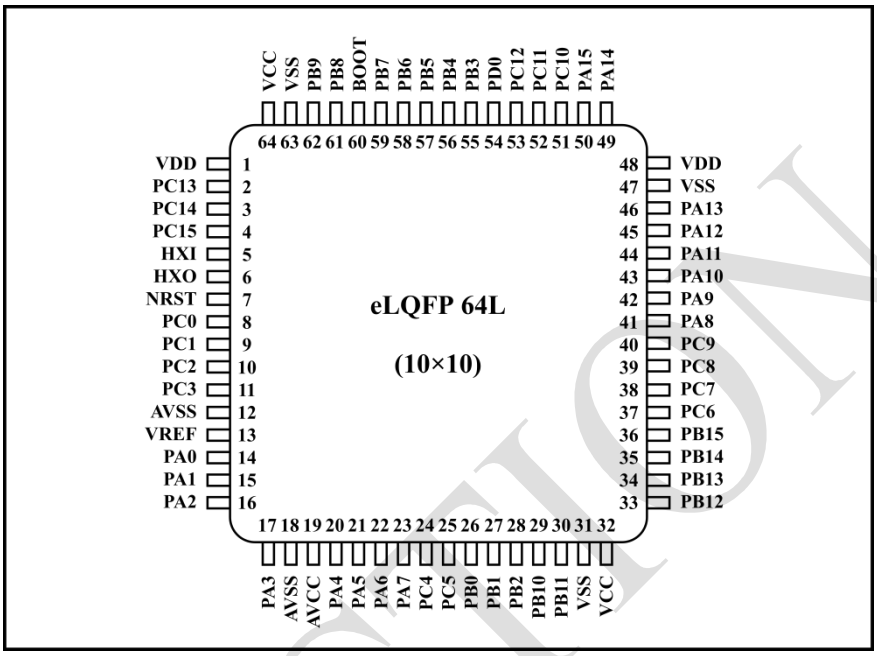


Figure 7. LQFP48L pinout

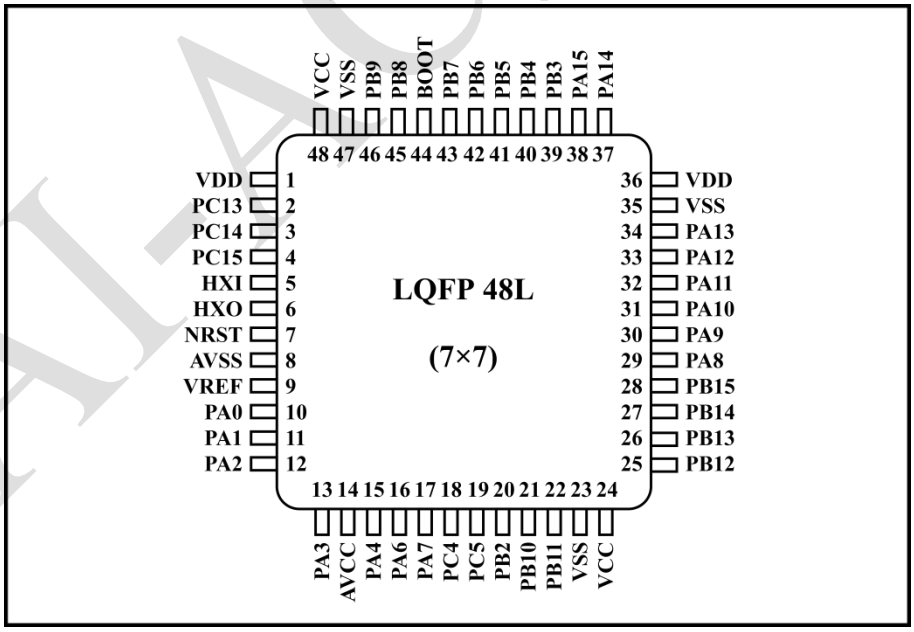


Figure 8. QFN40 pinout

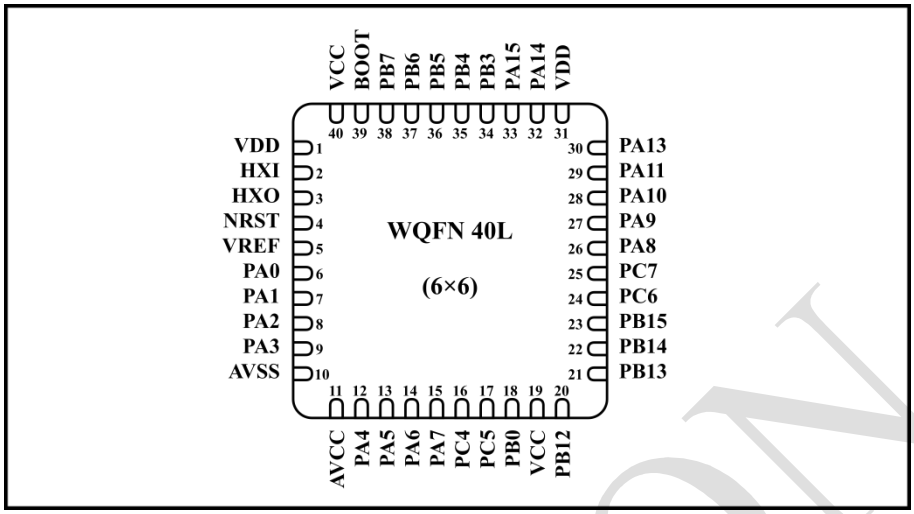


Figure 9. QFN32 pinout

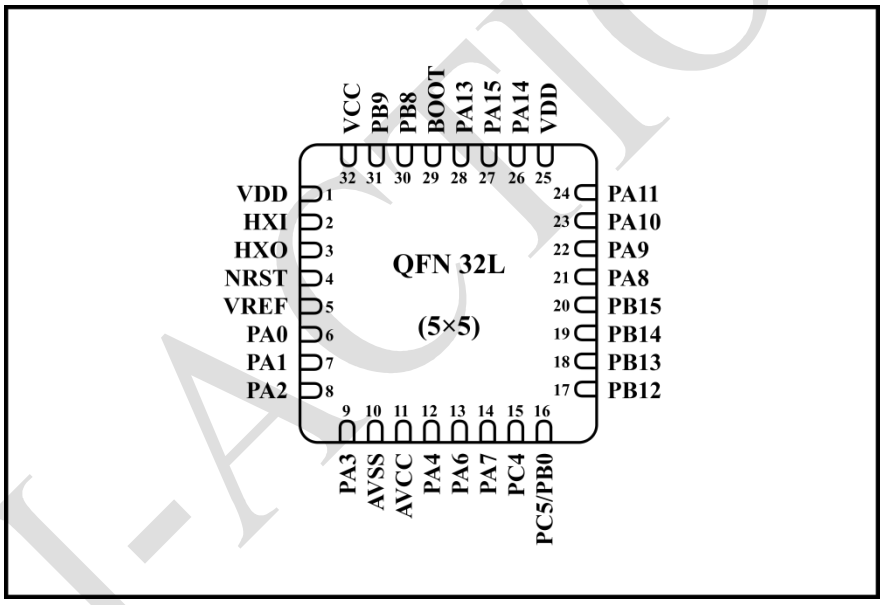


Table 4. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	SO	Supply output pin
	I	Input only pin
	I/O	Input / output pin
I/O structure	TT	3.3 V tolerant I/O
	B	Dedicated BOOT pin
	RST	Bi-directional reset pin with embedded weak pull-up resistor
Notes	Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Pin functions	Functions selected through GPIOx_MUX registers	

Table 5. TAE32F5300 pin definitions

Package					Pin type	I/O structure	Digital Functions	Analog Functions
QFN32	WQFN40	LQFP48	eLQFP64	Pin name				
1	1	1	1	VDD	SO	-	-	-
-	-	2	2	PC13	I/O	TT	TIMER5, TIMER6	-
-	-	3	3	PC14	I/O	TT	TIMER0	-
-	-	4	4	PC15	I/O	TT	TIMER1, TIMER4	-
2	2	5	5	HXI	-		-	-
3	3	6	6	HXO	-		-	-
4	4	7	7	NRST	I	RST	-	-
-	-	-	8	PC0	I/O	TT	TIMER4	ADC0/1_IN6
-	-	-	9	PC1	I/O	TT	-	ADC0/1_IN7
-	-	-	10	PC2	I/O	TT	TIMER6	ADC0/1_IN8
-	-	-	11	PC3	I/O	TT	TIMER7	ADC0/1_IN9
-	-	8	12	AVSS	S	-	-	-
5	5	9	13	VREF	SO	-	-	-
6	6	10	14	PA0	I/O	TT	TIMER4, DALI_TX, CMP3_OUT	ADC0_IN0
7	7	11	15	PA1	I/O	TT	TIMER0, TIMER5, DALI_RX, I2C1_SMBA, UART1_DE	ADC0_IN1
8	8	12	16	PA2	I/O	TT	TIMER0, TIMER6, I2C1_SCL, UART1_TX, CMP0_OUT	ADC0_IN2, CMP0_INM_0
9	9	13	17	PA3	I/O	TT	TIMER1, TIMER7, I2C1_SDA, UART1_RX	ADC0_IN3
10	10	-	18	AVSS	S	-	-	-
11	11	14	19	AVCC	S	-	-	-
12	12	15	20	PA4	I/O	TT	TIMER1,I2C1_SMBA, UART0_TX	ADC1_IN0, DAC0_OUT, CMP0_INM_1, CMP1_INM_1, CMP2_INM_1, CMP3_INM_1
-	13	-	21	PA5	I/O	TT	TIMER4, CAN_TX, I2C1_SCL, UART0_RX, CMP3_OUT	ADC1_IN1, DAC1_OUT
13	14	16	22	PA6	I/O	TT	TIMER0, TIMER2, CAN_RX, I2C1_SDA, UART0_DE	ADC1_IN2, DAC2_OUT

14	15	17	23	PA7	I/O	TT	TIMER1, TIMER3, TIMER4, I2C1_SMBS	ADC1_IN3, CMP0_INP
15	16	18	24	PC4	I/O	TT	TIMER4, UART0_TX, CMP3_OUT	ADC1_IN4, CMP3_INP
16	17	19	25	PC5	I/O	TT	UART0_RX	ADC1_IN5, DAC3_OUT
16	18		26	PB0	I/O	TT	TIMER2, TIMER5	ADC0_IN4, CMP1_INP
-	-	-	27	PB1	I/O	TT	TIMER3, TIMER6, UART1_DE, HRPWM_EVT0, HRPWM_SCIN, HRPWM_SCOUT, CMP1_OUT	ADC0_IN5
-	-	20	28	PB2	I/O	TT	CAN_TX, I2C0_SCL, UART1_TX, HRPWM_SCIN	ADC1_IN10, CMP1_INM_0
-	-	21	29	PB10	I/O	TT	TIMER6, CAN_RX, I2C0_SDA, UART1_RX, UART1_TX, HRPWM_FLT2	ADC0_IN10
-	-	22	30	PB11	I/O	TT	TIMER7, UART1_RX, HRPWM_FLT3	CMP2_INP
-	-	23	31	VSS	S	-	-	-
-	19	24	32	VCC	S	-	-	-
17	20	25	33	PB12	I/O	TT	HRPWM_OUT2A	-
18	21	26	34	PB13	I/O	TT	TIMER4, HRPWM_OUT2B	-
19	22	27	35	PB14	I/O	TT	TIMER0, TIMER5, UART1_DE, HRPWM_OUT3A	CMP3_INM_0
20	23	28	36	PB15	I/O	TT	TIMER2, TIMER1, TIMER6, HRPWM_OUT3B	CMP2_INM_0
-	24	-	37	PC6	I/O	TT	TIMER0, HRPWM_EVT4, HRPWM_OUT5A	-
-	25	-	38	PC7	I/O	TT	TIMER1, UART0_DE, HRPWM_FLT4, HRPWM_OUT5B	-
-	-	-	39	PC8	I/O	TT	TIMER2, HRPWM_OUT4A	-

-	-	-	40	PC9	I/O	TT	TIMER3, HRPWM_OUT4B	-
21	26	29	41	PA8	I/O	TT	MCO, TIMER4, CAN_TX, UART0_RX, HRPWM_OUT0A	-
22	27	30	42	PA9	I/O	TT	TIMER6, TIMER5, CAN_RX, UART0_TX, HRPWM_OUT0B	-
23	28	31	43	PA10	I/O	TT	TIMER7, TIMER6, CAN_TX, I2C0_SMBA, UART0_RX, HRPWM_OUT1A, CMP2_OUT	-
24	29	32	44	PA11	I/O	TT	TIMER5, TIMER7, CAN_RX, I2C0_SMBS, UART0_TX, HRPWM_OUT1B	-
-	-	33	45	PA12	I/O	TT	TIMER2, TIMER4, TIMER5, CAN_TX, UART0_DE, HRPWM_FLT0, CMP0_OUT	-
28	30	34	46	PA13	I/O	TT	SWDAT, TIMER2, I2C1_SCL, HRPWM_FLT4, CMP2_OUT	-
-	-	35	47	VSS	S	-	-	-
25	31	36	48	VDD	S	-	-	-
26	32	37	49	PA14	I/O	TT	SWCLK, TIMER5, I2C0_SDA, I2C1_SDA, UART1_TX, HRPWM_FLT5, HRPWM_SCIN	-
27	33	38	50	PA15	I/O	TT	TIMER4, I2C0_SMBA, I2C0_SCL, UART1_TX, UART1_RX, HRPWM_FLT1	-
-	-	-	51	PC10	I/O	TT	I2C0_SMBS,UART1_RX, UART0_TX, HRPWM_FLT4, HRPWM_FLT0	-
-	-	-	52	PC11	I/O	TT	UART0_RX, HRPWM_EVT1	-

-	-	-	53	PC12	I/O	TT	UART1_DE, UART0_DE, HRPWM_EVT0, HRPWM_FLT2	-
-	-	-	54	PD0	I/O	TT	TIMER0, HRPWM_FLT5, HRPWM_FLT3, CMP2_OUT	-
-	34	39	55	PB3	I/O	TT	SWO, TIMER1, TIMER5, I2C1_SCL, UART1_TX, HRPWM_SCOUT, HRPWM_EVT2	USB-DM
-	35	40	56	PB4	I/O	TT	TIMER0, I2C1_SDA, UART1_RX, HRPWM_EVT1	USB-DP
-	36	41	57	PB5	I/O	TT	TIMER2, I2C0_SMBA, I2C1_SMBA, HRPWM_EVT5, CMP3_OUT	-
-	37	42	58	PB6	I/O	TT	TIMER2, I2C0_SCL, I2C1_SMBS, UART0_TX, HRPWM_EVT0, HRPWM_SCIN, HRPWM_EVT3	-
-	38	43	59	PB7	I/O	TT	TIMER3, TIMER0, I2C0_SDA, UART0_RX, HRPWM_EVT4, CMP1_OUT	-
29	39	44	60	BOOT	I	B	-	
30	-	45	61	PB8	I/O	TT	TIMER2, CAN_RX, I2C0_SCL, UART1_RX, HRPWM_EVT2	-
31	-	46	62	PB9	I/O	TT	TIMER3, CAN_TX, I2C0_SDA, UART1_TX, HRPWM_EVT3, CMP0_OUT	-
-	-	47	63	VSS	S	-	-	-
32	40	48	64	VCC	S	-	-	-

Table 6. Alternate functions

Pin name	Functions															
	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
	IN	OUT	SYS	TIMER0-3	TIMER 0-3	TIMER 4-7	TIMER 4-7	CAN/I2C0	I2C0/DALI	I2C1/UART1	UART0/UART1	HRPWM/USB	HRPWM	HRPWM	CMP0-3	Analog function
PA0	-	-	-	-	-	TIMER4	-	-	DALI_TX	-	-	-	-	-	CMP3_OUT	ADC0_IN0
PA1	-	-	-	-	TIMER0	TIMER5	-	-	DALI_RX	I2C1_SMBA	UART1_DE	-	-	-	-	ADC0_IN1
PA2	-	-	-	-	TIMER0	TIMER6	-	-	-	I2C1_SCL	UART1_TX	-	-	-	CMP0_OUT	ADC0_IN2,CMP0_INM_0
PA3	-	-	-	-	TIMER1	TIMER7	-	-	-	I2C1_SDA	UART1_RX	-	-	-	-	ADC0_IN3
PA4	-	-	-	TIMER1	-	-	-	-	-	I2C1_SMBA	UART0_TX	-	-	-	-	ADC1_IN0,DAC0_OUT, CMP0_INM_1,CMP1_INM_1, CMP2_INM_1,CMP3_INM_1
PA5	-	-	-	-	-	TIMER4	-	CAN_TX	-	I2C1_SCL	UART0_RX	-	-	-	CMP3_OUT	ADC1_IN1,DAC1_OUT
PA6	-	-	-	TIMER0	TIMER2	-	-	CAN_RX	-	I2C1_SDA	UART0_DE	-	-	-	-	ADC1_IN2,DAC2_OUT
PA7	-	-	-	TIMER1	TIMER3	-	TIMER4	-	-	I2C1_SMBS	-	-	-	-	-	ADC1_IN3,CMP0_INP
PA8	-	-	MCO	-	-	-	TIMER4	CAN_TX	-	-	UART0_RX	-	-	HRPWM_OUT0A	-	-
PA9	-	-	-	-	-	TIMER6	TIMER5	CAN_RX	-	-	UART0_TX	-	-	HRPWM_OUT0B	-	-
PA10	-	-	-	-	-	TIMER7	TIMER6	CAN_TX	I2C0_SMBA	-	UART0_RX	-	-	HRPWM_OUT1A	CMP2_OUT	-
PA11	-	-	-	-	-	TIMER5	TIMER7	CAN_RX	I2C0_SMBS	-	UART0_TX	-	-	HRPWM_OUT1B	-	-
PA12	-	-	-	-	TIMER2	TIMER4	TIMER5	CAN_TX	-	-	UART0_DE	-	-	HRPWM_FLT0	CMP0_OUT	-
PA13[1]	-	-	SWDAT	-	TIMER2	-	-	-	-	I2C1_SCL	-	HRPWM_FLT4	-	-	CMP2_OUT	-
PA14[1]	-	-	SWCLK	-	-	-	TIMER5	-	I2C0_SDA	I2C1_SDA	UART1_TX	HRPWM_FLT5	HRPWM_SCIN	-	-	-
PA15	-	-	-	-	-	TIMER4	-	I2C0_SMBA	I2C0_SCL	UART1_TX	UART1_RX	-	-	HRPWM_FLT1	-	-
PB0	-	-	-	TIMER2	-	-	TIMER5	-	-	-	-	-	-	-	-	ADC0_IN4,CMP1_INP
PB1	-	-	-	TIMER3	-	-	TIMER6	-	-	UART1_DE	-	HRPWM_EVT0	HRPWM_SCIN	HRPWM_SCOUT	CMP1_OUT	ADC0_IN5
PB2	-	-	-	-	-	-	-	CAN_TX	I2C0_SCL	UART1_TX	-	-	-	HRPWM_SCIN	-	ADC1_IN10,CMP1_INM_0
PB3	-	-	SWO	TIMER1	-	TIMER5	-	-	-	I2C1_SCL	UART1_TX	-	HRPWM_SCOUT	HRPWM_EVT2	-	USB-DM
PB4	-	-	-	TIMER0	-	-	-	-	-	I2C1_SDA	UART1_RX	-	-	HRPWM_EVT1	-	USB-DP
PB5	-	-	-	-	TIMER2	-	-	-	I2C0_SMBA	I2C1_SMBA	-	-	-	HRPWM_EVT5	CMP3_OUT	-

PB6	-	-	-	-	TIMER2	-	-	-	I2C0_SCL	I2C1_SMBS	UART0_TX	HRPWM_EVT0	HRPWM_SCIN	HRPWM_EVT3	-	-
PB7	-	-	-	TIMER3	TIMER0	-	-	-	I2C0_SDA	-	UART0_RX	-	-	HRPWM_EVT4	CMP1_OUT	-
PB8	-	-	-	-	TIMER2	-	-	CAN_RX	I2C0_SCL	-	UART1_RX	-	-	HRPWM_EVT2	-	-
PB9	-	-	-	-	TIMER3	-	-	CAN_TX	I2C0_SDA	-	UART1_TX	-	-	HRPWM_EVT3	CMP0_OUT	-
PB10	-	-	-	-	-	TIMER6	-	CAN_RX	I2C0_SDA	UART1_RX	UART1_TX	-	-	HRPWM_FLT2	-	ADC0_IN10
PB11	-	-	-	-	-	TIMER7	-	-	-	-	UART1_RX	-	-	HRPWM_FLT3	-	CMP2_INP
PB12	-	-	-	-	-	-	-	-	-	-	-	-	-	HRPWM_OUT2A	-	-
PB13	-	-	-	-	-	-	TIMER4	-	-	-	-	-	-	HRPWM_OUT2B	-	-
PB14	-	-	-	-	TIMER0	-	TIMER5	-	-	-	UART1_DE	-	-	HRPWM_OUT3A	-	CMP3_INM_0
PB15	-	-	-	TIMER2	TIMER1	-	TIMER6	-	-	-	-	-	-	HRPWM_OUT3B	-	CMP2_INM_0
PC0	-	-	-	-	-	-	TIMER4	-	-	-	-	-	-	-	-	ADC0/1_IN6
PC1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	ADC0/1_IN7
PC2	-	-	-	-	-	-	TIMER6	-	-	-	-	-	-	-	-	ADC0/1_IN8
PC3	-	-	-	-	-	-	TIMER7	-	-	-	-	-	-	-	-	ADC0/1_IN9
PC4	-	-	-	-	-	-	TIMER4	-	-	-	UART0_TX	-	-	-	CMP3_OUT	ADC1_IN4,CMP3_INP
PC5	-	-	-	-		-	-	-	-	-	UART0_RX	-	-	-	-	ADC1_IN5,DAC3_OUT
PC6	-	-	-	TIMER0	-	-	-	-	-	-	-	HRPWM_EVT4	-	HRPWM_OUT5A	-	-
PC7	-	-	-	TIMER1	-	-	-	-	-	-	UART0_DE	HRPWM_FLT4	-	HRPWM_OUT5B	-	-
PC8	-	-	-	TIMER2	-	-	-	-	-	-	-	HRPWM_OUT4A	-	-	-	-
PC9	-	-	-	TIMER3	-	-	-	-	-	-	-	HRPWM_OUT4B	-	-	-	-
PC10	-	-	-	-	-	-	-	I2C0_SMBS	-	UART1_RX	UART0_TX	-	HRPWM_FLT4	HRPWM_FLT0	-	-
PC11	-	-	-	-	-	-	-	-	-	-	UART0_RX	HRPWM_EVT1	-	-	-	-
PC12	-	-	-	-	-	-	-	-	-	UART1_DE	UART0_DE	HRPWM_EVT0	-	HRPWM_FLT2	-	-
PC13	-	-	-	-	-	TIMER6	TIMER5	-	-	-	-	-	-	-	-	-
PC14	-	-	-	TIMER0	-	-	-	-	-	-	-	-	-	-	-	-
PC15	-	-	-	-	TIMER1	TIMER4	-	-	-	-	-	-	-	-	-	-
PD0	-	-	-	TIMER0	-	-	-	-	-	-	-	HRPWM_FLT5	-	HRPWM_FLT3	CMP2_OUT	-

Note:(1) PA13/PA14 are debugging pins, the PA13 data interface has a built-in pull-up, and the PA14 clock interface has a built-in pull-down.

5 Memory mapping

Figure 10. TAE32F5300 memory map

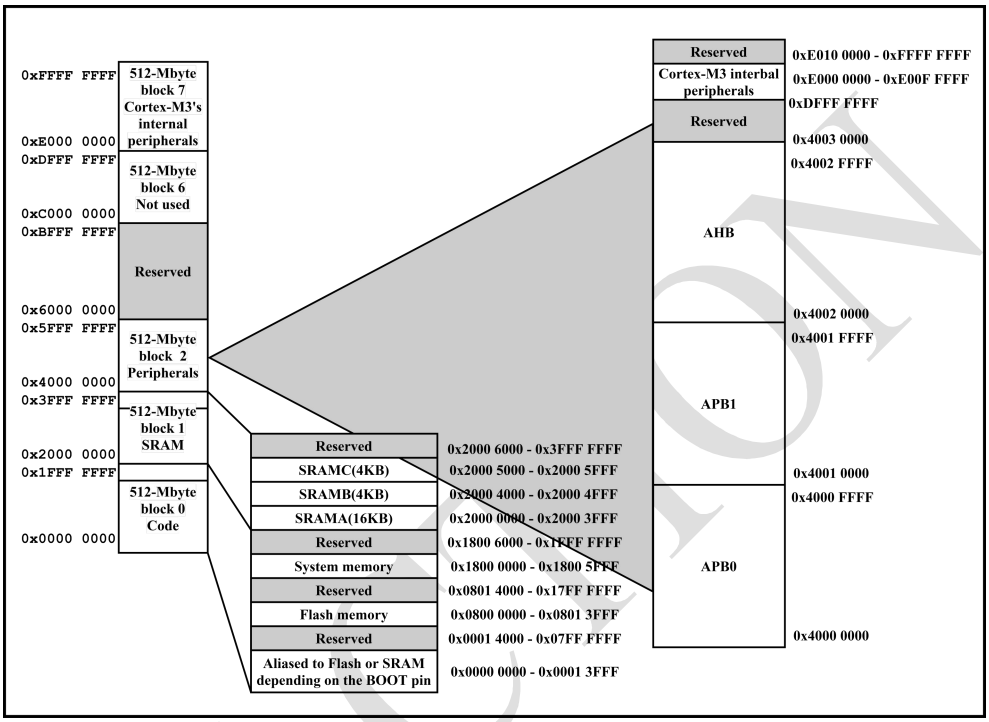


Table 7. TAE32F5300 peripheral register boundary addresses

Bus	Boundary address	Peripheral
Reserved	0xE010 0000 - 0xFFFF FFFF	Reserved
Cortex™-M3	0xE000 0000 - 0xE00F FFFF	Cortex™-M3 internal peripherals
Reserved	0x4003 0000 - 0xDFFF FFFF	Reserved
AHB	0x4002 EC00 - 0x4002 EFFF	CMP
	0x4002 E800 - 0x4002 EBFF	DAC
	0x4002 E400 - 0x4002 E7FF	ADC1
	0x4002 E000 - 0x4002 E3FF	ADC0
	0x4002 D000 - 0x4002 DFFF	HRPWM
	0x4002 C000 - 0x4002 CFFF	USB
	0x4002 A000 - 0x4002 AFFF	DFLASH CTRL
	0x4002 9000 - 0x4002 9FFF	FLASH CTRL
	0x4002 8400 - 0x4002 84FF	TIMERGRP1
	0x4002 8300 - 0x4002 83FF	TIMER7
	0x4002 8200 - 0x4002 82FF	TIMER6
	0x4002 8100 - 0x4002 81FF	TIMER5
	0x4002 8000 - 0x4002 80FF	TIMER4
	0x4002 7000 - 0x4002 7FFF	GPIOD

	0x4002 6000 - 0x4002 6FFF	GPIOC
	0x4002 5000 - 0x4002 5FFF	GPIOB
	0x4002 4000 - 0x4002 4FFF	GPIOA
	0x4002 3000 - 0x4002 3FFF	SYSCTRL
	0x4002 2000 - 0x4002 2FFF	CAN
	0x4002 0000 - 0x4002 0FFF	DMA
APB1	0x4001 FF00 - 0x4001 FFFF	ECU
	0x4001 F900 - 0x4001 F9FF	IIR4
	0x4001 F800 - 0x4001 F8FF	IIR3
	0x4001 F700 - 0x4001 F7FF	IIR2
	0x4001 F600 - 0x4001 F6FF	IIR1
	0x4001 F500 - 0x4001 F5FF	IIR0
	0x4001 B000 - 0x4001 BFFF	FPLL2
	0x4001 A000 - 0x4001 AFFF	FPLL1
	0x4001 9000 - 0x4001 9FFF	FPLL0
	0x4001 8000 - 0x4001 8FFF	WWDG
	0x4001 7000 - 0x4001 7FFF	IWDG
	0x4001 6000 - 0x4001 6FFF	DALI
APB0	0x4000 D000 - 0x4000 DFFF	LVDCTRL
	0x4000 C400 - 0x4000 C4FF	TIMERGRP0
	0x4000 C300 - 0x4000 C3FF	TIMER3
	0x4000 C200 - 0x4000 C2FF	TIMER2
	0x4000 C100 - 0x4000 C1FF	TIMER1
	0x4000 C000 - 0x4000 C0FF	TIMER0
	0x4000 5000 - 0x4000 5FFF	UART1
	0x4000 4000 - 0x4000 4FFF	UART0
	0x4000 1000 - 0x4000 1FFF	I2C1
	0x4000 0000 - 0x4000 0FFF	I2C0

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to VSS.

6.1.1 Minimum and maximum values

Unless otherwise specified, the maximum and minimum values are the test results under the worst environmental temperature, supply voltage and frequency.

6.2 Absolute maximum rating

Voltage, current, or temperature exceeding the absolute maximum ratings shown in the table below may cause permanent damage to the device.

6.2.1 Voltage characteristics

Table 8. Voltage characteristics

Symbol	Parameter	Min	Max	Unit
VCC -VSS	External main supply voltage (including VCC、AVCC)	-0.3	4.0	V
VCC - AVCC	Allowed voltage difference for VDD and VDDA	-0.4	0.4	V
VIN	Input voltage on GPIO	VSS-0.3	4.0	V
	Input voltage on crystal	VSS-0.3	1.8	V
ΔVCCx	Variations between different VCC power pins	-	50	mV
ΔVSSx	Variations between different VSS power pins (including AVSS)	-	50	mV
ESD(HBM)	Electrostatic discharge voltage (human body model)	TBD	-	V

6.2.2 Current characteristics

Table 9. Current characteristics

Symbol	Parameter	Max.	Unit
ΣI_{VCC}	Total current into sum of all VCC power lines	200	mA
ΣI_{AVCC}	Total current into sum of all AVCC power lines	100	mA
I_{VCC}	Maximum current into each VCC power line	100	mA
I_{AVCC}	Maximum current into each AVCC power line	100	mA
I_{IO}	Output current source by any GPIO and control pin	24	mA
ΣI_{IO}	Total output current sunk by sum of all GPIO and control pins	80	mA

6.2.3 Thermal characteristics

Table 10. Thermal characteristics

Symbol	Parameter	Max.	Unit
T_{STRG}	Storage temperature range	TBD	℃
T_j	Junction temperature	125	℃

6.3 Operating conditions

Table 11. Operating conditions

General Operating Conditions						
Symbol	**Parameters**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
F_{hclk}	Internal AHB clock frequency		0		90	MHz
F_{pclk0}	Internal APB0 clock frequency		0			MHz
F_{pclk1}	Internal APB1 clock frequency		0			MHz
VCC	Standard operating voltage		3.1	3.3	3.63	V
AVCC	Analog operating voltage	Have a potential equal to VCC	3.1	3.3	3.63	V
VDD	Digital Core operating voltage		1.35	1.5	1.65	V
V_{REF}	Reference voltage	After calibration		1.5		
V_{IN}	I/O input voltage	GPIO	-0.3		VCC+0.3	V
		HXI、HXO	-0.3		VDD+0.3	V
PD	Overall power consumption	TA=85℃,frequency=90MHz,non-loaded			400	mW
T_J	Temperature range		-40		125	℃

6.4 Operating conditions at power-up / power-down

(VCC=AVCC=3.3V,VDD=1.5V,TA=25℃.Unless otherwise specified)

Table 12. Operating conditions at power up / power down

Operating conditions at power up / power down						
Symbol	**Parameters**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
VCC_{POR}*	AVCC/VCC Power on/power down reset threshold	Falling edge	1.54	1.75	1.91	V
		Rising edge	1.97	2.12	2.3	V
$VCC_{PORhyst}$*	AVCC/VCC POR hysteresis			400		mV
VCC_{OK}*	AVCC/VCC Power on OK threshold	Falling edge		2.25		V
		Rising edge		2.7		V
VDD_{POR}*	VDD Power on/power down reset threshold	Falling edge	0.54	0.66	0.7	V
		Rising edge	0.82	0.87	0.92	V
$VDD_{PORhyst}$*	VDD POR hysteresis			100		mV

VCC_{LVD}*	VCC、AVCC Low-voltage detection threshold	2bit Configurable	2.4		3	V
T_{rst}*	Power on reset threshold		1.3	2	2.9	ms

Note:*Guaranteed by design.

6.5 Internal Reference Voltage

(AVCC=3.3V,TA=25℃)

Table 13. Internal Reference Voltage

Internal Reference Voltage						
Symbol	**Parameters**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
V_{REF}	Internal reference voltage	-40℃ < TA < 105℃		1.5		V
T_{coeff}*	Temperature coefficient	-40℃ < TA < 105℃		50	100	ppm/℃
V_{REF+}	Internal positive reference voltage	-40℃ < TA < 105℃,After TRIM		3		V
$V_{REF+(no)}$*	Internal positive reference noise	CL=2.2uF		110		uVrms

Note:*Guaranteed by design.

6.6 Clock characteristics

6.6.1 External Crystal Oscillator Characteristics

(VCC=AVCC=3.3V,AVDD=1.5V,TA=25℃)

Table 14. External Crystal Oscillator Characteristics

External Crystal Oscillator Characteristics						
Symbol	**Parameter**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
F_{xosc}	External clock source frequency or XOSC frequenc		4	8	26	MHz
VXI_H*	XI input high-level voltage		1.05	-	1.65	V
VXI_L*	XI input low-level voltage		0	-	0.45	V
Duty	External input clock duty cycle		45	50	55	%
R_{FB}	Feedback resistor		40	50	60	kΩ
I_{AVCC}	Power consumption of starting circuit	During Start-Up			2	mA
		Rs=30,CL=10pF @ 8MHz		0.4		
		Rs=45,CL=10pF @ 8MHz		0.5		
		Rs=30,CL=5pF @ 32MHz		0.8		

		Rs=30,CL=10pF @ 32MHz		1		
		Rs=30,CL=20pF @ 32MHz		1.5		
gm*	Oscillator transconductance	During startup, DR is adjustable	2		20	mA/V
T_{su}*	Startup time	Software enable to output stable clock		0.5	2	ms

Note:*Guaranteed by design.

6.6.2 High-Speed Internal RC oscillator Characteristics

(VCC=AVCC=3.3V,VDD=1.5V,TA=25℃)

Table 15. High-Speed Internal RC oscillator Characteristics

High-Speed Internal RC oscillator Characteristics						
symbol	**Parameter**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
F_{HSI}**	Frequency		5	8	13	MHz
DuCy	Duty Cycle		45	50	55	%
ACC*	Oscillator frequency accuracy	TA=-40 ~ 105℃		±1		%
		TA=-10 ~ 85℃		±0.6		
		TA=0 ~ 85℃				
T_{su}*	Startup time	Software enable to output stable clock			1	us
I_{VCC}	Oscillator power consumption	TA=25℃ @ 8MHz		1.2		mA

Note:*Oscillation frequency is measured during CP test and stored at flash. Accuracy is tested during Characterization.

Note:**The oscillation frequency is not calibrated during factory trim, user should adjust PLLDIV coefficients to get an accurate PLL output frequency.

6.6.3 Low-Speed Internal RC oscillator Characteristics

(VCC=AVCC=3.3V,TA=25℃)

Table 16. Low-Speed Internal RC oscillator Characteristics

Low-Speed Internal RC oscillator Characteristics						
symbol	**Parameter**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
F_{LSI}**	Frequency		24	32	40	kHz
DuCy	Duty Cycle		45	50	55	%
ACC*	Oscillator frequency accuracy	TA=-40 ~ 105℃		±0.35		%

Note:*Guaranteed by design.

Note:**The oscillation frequency is not calibrated during factory trim.

6.6.4 PLL Characteristics

(VCC=AVCC=3.3V,TA=25℃)

Table 17. PLL Characteristics

PLL Characteristics					
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**
F_{PLL_IN}	PLL Input Clock	4		26	MHz
F_{PLL_OUT}	PLL Output Clock	60	160	220	MHz
T_{LOCK}*	PLL Lock Clock		0.5	2	ms
T_{Jitter}*	Cycle to Cycle Jitter			300	ps

Note:*Guaranteed by design.

6.6.5 HRPWM Characteristics

(VCC=AVCC=3.3V,TA=25℃)

Table 18. HRPWM Characteristics

HRPWM Characteristics						
Symbol	**Parameter**	**Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
F_{HRPWM}	HRPWM Clock frequency		120		160	MHz
T_{RES}*	Clock resolution	F_{HRPWM}=160MHz, TA=-40~105℃	-	195	-	ps
ResTIMER	Timer resolution				16	bit
$F_{CHOPFREQ}$	Chopping clock frequency		1/256		1/16	F_{HRPWM}
T_{1STPW}	Chopping the first pulse width		16		256	T_{HRPWM}

Note:*Guaranteed by design.

6.7 FLASH Memory Characteristics

Table 19. FLASH Memory Characteristics

FLASH Memory Characteristics						
Symbol	**Parameter**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
T_{PROG}	Byte Program time			6		us
T_{SECTOR_ERAZE}	Sector Erase time			4		ms
T_{CHIP_ERAZE}	Chip Erase time			20		ms
T_{ACCESS}	Fast read access time			30		ns
N_{END}	FLASH Endurance		20			kCycles
	DFLASH Endurance		100			
T_{RET}	Data Retention	TA=25℃	100			Years
		TA=105℃	20			
		TA=125℃	10			

6.8 IO static Characteristics

Table 20. IO static Characteristics

IO static Characteristics						
Symbol	**Parameter**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
V_{IL}	Low level input voltage	GPIO Hysteresis On	0.43*VCC-0.15	0.45*VCC-0.12	0.48*VCC-0.12	V
		HXI Hysteresis On	0.665	0.714	0.771	
		GPIO Hysteresis Off	0.455*VCC	0.5*VCC	0.54*VCC	
V_{IH}	High level input voltage	GPIO Hysteresis On	0.54*VCC+0.08	0.545*VCC+0.165	0.56*VCC+0.2	
		HXI Hysteresis On	0.732	0.784	0.846	
		GPIO Hysteresis Off	0.455*VCC	0.5*VCC	0.54*VCC	
C_{IO}	IO pin capacitance	Total Capacitance should add Package Cap:1.5pF	1.39	1.65	1.75	pF
R_{PU}	weak pull-up equivalent resistor		8.3	10	12	kΩ
R_{PD}	weak pull-down equivalent resistor		8.3	10	12	kΩ
V_{OL}	Low level output voltage	IIO=+6mA, DS=0	-	-	0.57	V
		IIO=+20mA, DS=1	-	-	0.66	
V_{OH}	High level output voltage	IIO=+6mA, DS=0	VCC-0.59	-	-	V
		IIO=+20mA, DS=1	VCC-0.68	-	-	
R_{NRST}	NRST PIN Pull-up resistor		75	100	125	kΩ
R_{BOOT}	BOOT PIN Pull-up resistor		75	100	125	kΩ

6.9 Analog peripheral characteristics

6.9.1 ADC characteristics

(AVCC=3.3V,TA=25℃,F_ADC=160MHz,Unless otherwise specified)

Table 21. ADC Characteristics

ADC Characteristics						
Symbol	**Parameter**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
AVCC	Analog supply voltage for ADC		3.1	3.3	3.6	V
Resolution	ADC Resolution			13		bit

V_{ref+}	ADC Positive reference voltage			3		V
V_{ref-}	ADC Negative reference voltage, the device is internally connected to AVSS			0		V
V_{AIN}	ADC Input voltage range		AVSS		3	V
C_{IN}	ADC Input capacitance			1.6		pF
F_{ADC}	ADC Working Clock			160		MHz
F_s	ADC Sampling Rate	2 times oversampling			2.2	MSps
T_{sample}	ADC Sampling time ADC Clock cycle		6		1530	Tadc
T_{con}	Total conversion time	Tcon=Tsample(6~1530Tadc) +Tconv(30Tadc)	36		1560	Tadc
DNL*	Differential nonlinearity			TBD		LSB
INL*	Integral nonlinearity			TBD		LSB
I_{AVCC}	ADC Power consumption	Single ended / differential, 2.2MSPS		2		mA
DR*	ADC Dynamic Range	Differential mode, -40dBFS Input measurement, 10kHz Sinusoidal signal		70		dB
		Single ended mode, -40dBFS Input measurement, 10kHz Sinusoidal signal		65		dB
SNDR*	ADC Signal to noise distortion ratio	Differential mode, -6dBFS Input measurement, 10kHz Sinusoidal signal		68		dB
		Single ended mode, -6dBFS Input measurement, 10kHz Sinusoidal signal		65		dB

Note:*Guaranteed by design.

6.9.2 DAC Characteristics

(AVCC=3.3V,TA=25℃,Unless otherwise specified)

Table 22. DAC Characteristics

DAC Characteristics						
Symbol	**Parameter**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
AVCC	Analog supply voltage		3.1	3.3	3.6	V
Resolution	DAC Resolution			12		bit
V_{ref+}	DAC Positive reference voltage, The device is internally connected to AVCC			AVCC		V
V_{ref-}	DAC Negative reference voltage, The device is internally connected to AVSS			AVSS		V
V_{DACOUT}	DAC Output voltage range		AVSS		AVCC-1LSB	V
$t_{setting}$*	DAC Setting time	DAC Data 0->4095 DAC Data 4095->0 CL=50pF			3	us
DNL*	Differential nonlinearity				±1	LSB
INL*	Integral nonlinearity				±2	LSB
I_{AVCC}	DAC Power consumption			2		mA
Update Rate	DAC Data update rate				2	MS/s

Note:*Guaranteed by design.

6.9.3 Comparator Characteristics

(AVCC=3.3V,TA=25℃)

Table 23. Comparator Characteristics

Comparator Characteristics						
Symbol	**Parameter**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
AVCC	Analog supply voltage		3.1	3.3	3.6	V
V_{in}	CMP Input voltage range		GND		AVCC	V
V_{offset}*	CMP Offset voltage			±5		mV
V_{hyst}*	CMP Hysteresis voltage	0~30mV adjustable	0		30	mV
T_{DLY}*	CMP Delay	From CMP Input pin to Output pin,CL= 30pF		15	20	ns

Note:*Guaranteed by design.

6.9.4 Temperature Sensor Characteristics

(AVCC=3.3V,TA=25℃)

Table 24. Temperature Sensor Characteristics

Temperature Sensor Characteristics						
Symbol	**Parameter**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Slope*	Slope of temperature curve		4.6	4.81	5	mV/℃
V_0	Temperature sensor output Voltage at 0℃		1.26	1.34	1.42	V
T_{START}	Startup time		4		10	us

Note: In order to ensure the measurement accuracy of the temperature sensor, ADC oversampling can be turned on.

Note: *Guaranteed by design.

7 Package information

Figure 11. eLQFP64L package outline

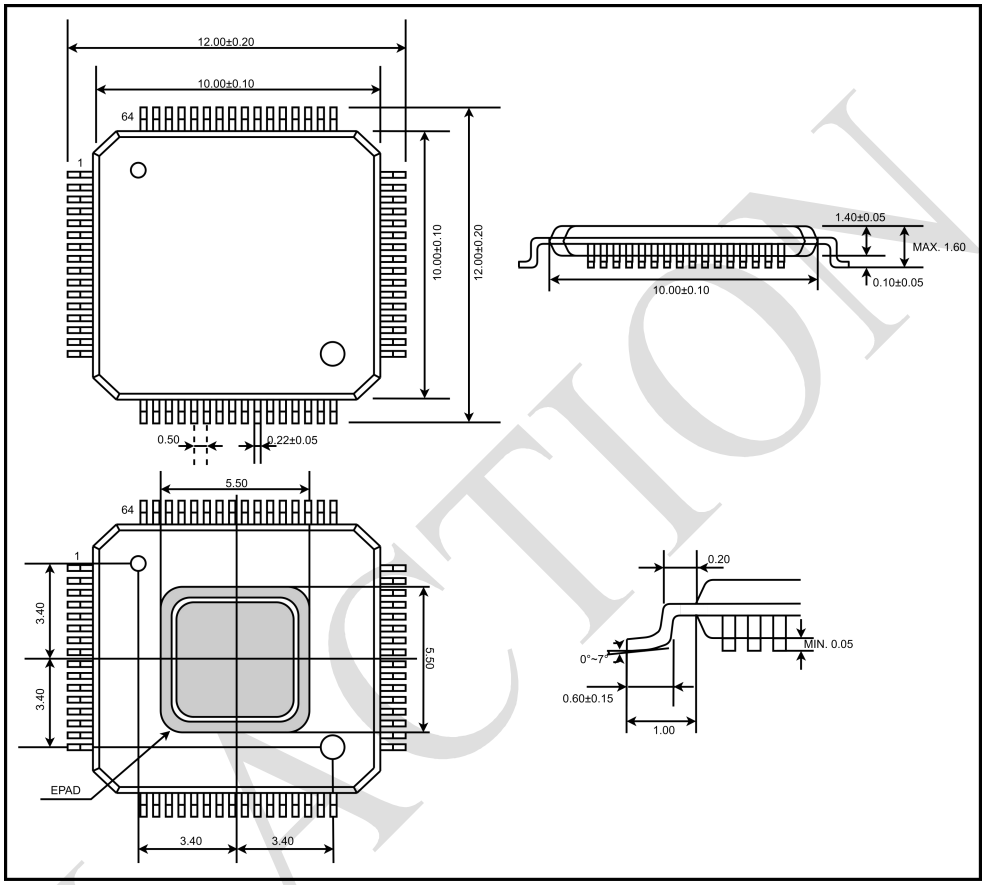


Figure 12. LQFP48L package outline

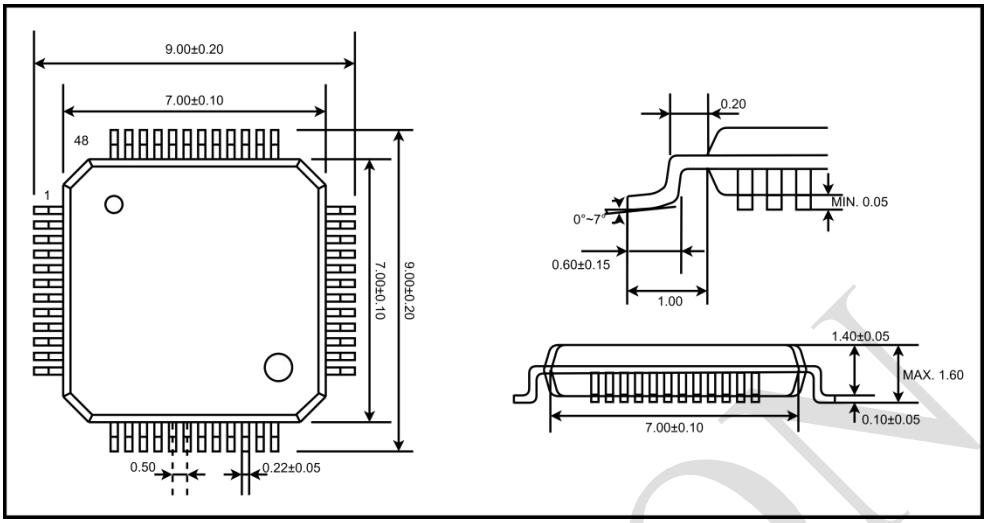


Figure 13. WQFN40 package outline

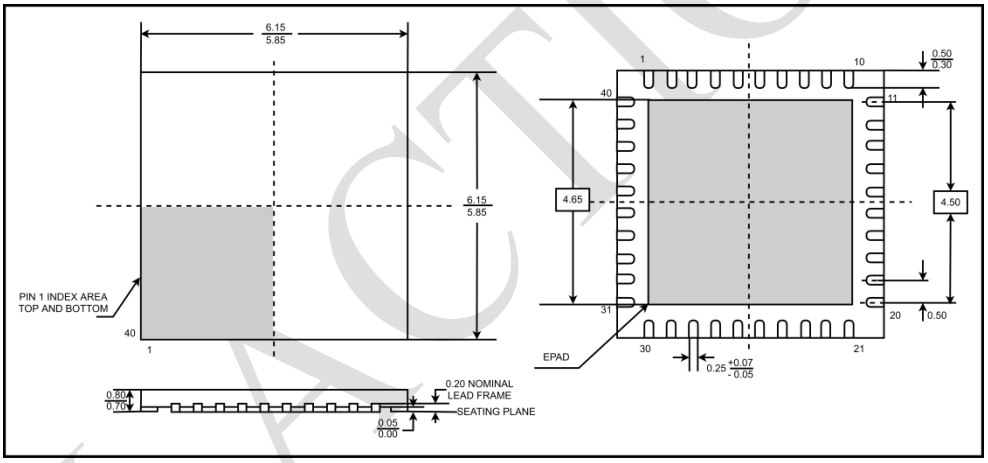
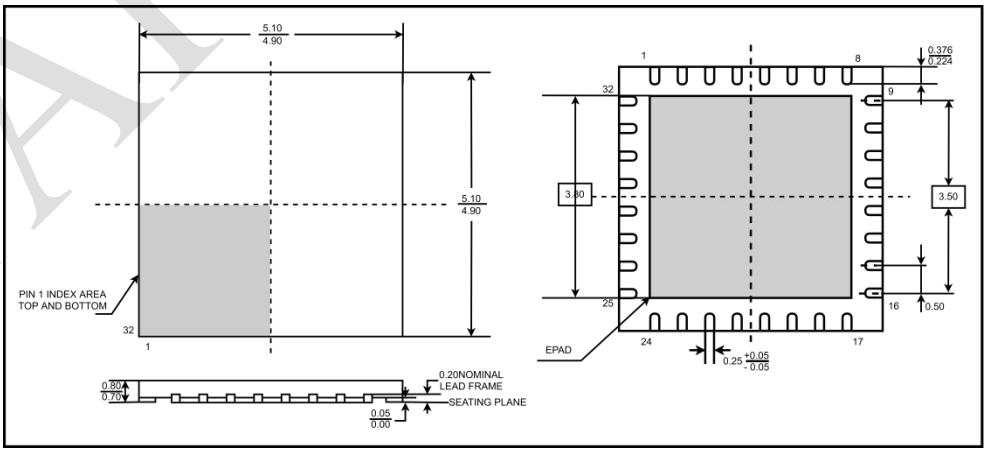


Figure 14. QFN32 package outline



NOTE：UNITS OF MEASURE = MILLIMETER

8 Ordering information

Table 25. Ordering information scheme

Example: TAE32 F 5300 A L F 128

Device family

TAE30 = ARM Cortex-M0 32bit
TAE32 = ARM Cortex-M3 32bit
TAE33 = ARM Cortex-M4 32bit
TAE34 = ARM Cortex-M7 32bit

Product type

F = Flash type
L = Low power consumption type

Device subfamily

5300 = Product number

Junction temperature range

G = Industrial temperature range, -40 to 105 °C
A = Industrial temperature range, -40 to 125 °C

Pin count

E = eLQFP
L = LQFP
W = WQFN
Q = QFN

Pin count

C = 32 pins
D = 40 or 48 pins
F = 64 pins

Flash memory size

128= 80KB(5KB ECC)

Revision history

Date	Revision	Changes
2021/11/24	v1.0	Initial release.
2021/12/8	v1.1	Add the Description of 48PIN package
2021/12/13	v1.2	Edit LQFP48 pinout
2022/3/11	v1.2.1	Modify the number of 12-bit DAC channels in the Table 1. TAE32F5300 device features and peripheral counts(32-pin)
2022/4/18	V1.3	Refinement of four types of packaging for TAE32F5300