August 2014

FSA880 / FSA881 – USB Port 2:1 Switch with Accessory and Charger Detection

Features

Switch Type	2:1 USB
Switch Mechanism	Automatic switching with Available Interrupt
Accessory Detection	USB Data Cable Chargers (CDP, DCP, Travel Adapter, Car Kit-CEA-936-A) Factory-Mode Cables
USB	FS and HS 2.0 Compliant
USB Charging	Battery Charging 1.1 Compliant Charger Detect, DCD, OVT (28 V)
UART	RxD and TxD
VBAT	3.0 to 4.4 V
Programmability	I^2C
ESD	15kV IEC 61000-4-2 Air Gap
Operating Temperature	-40°C to 85°C
Package	16-Lead UMLP 1.8x2.6x0.55 mm, 0.4 mm Pitch
JIG Option	FSA880 – Active LOW FSA881 – Active HIGH
Ordering Information	FSA880UMX FSA881UMX

Description

The FSA88x is a high-performance switch featuring automatic switching and accessory detection for a USB port. The FSA88x allows sharing of a common USB port to pass USB data, as well as factory programmability. In addition, the FSA88x integrates accessory detection of devices such as USB chargers and factory data cables. The FSA88x can be programmed for manual switching or automatic switching of data paths. VBUS_IN has 28 V over-voltage tolerance.

The difference between the FSA880 and the FSA881 is that FSA880 JIG output is an open-drain, active-LOW output, while FSA881 JIG is an active-HIGH, CMOS output.

Applications

- Cellular Phones, Smart Phones
- MP3 and PMP

Related Resources

- FSA880 / FSA881 Demonstration Board

Typical Application

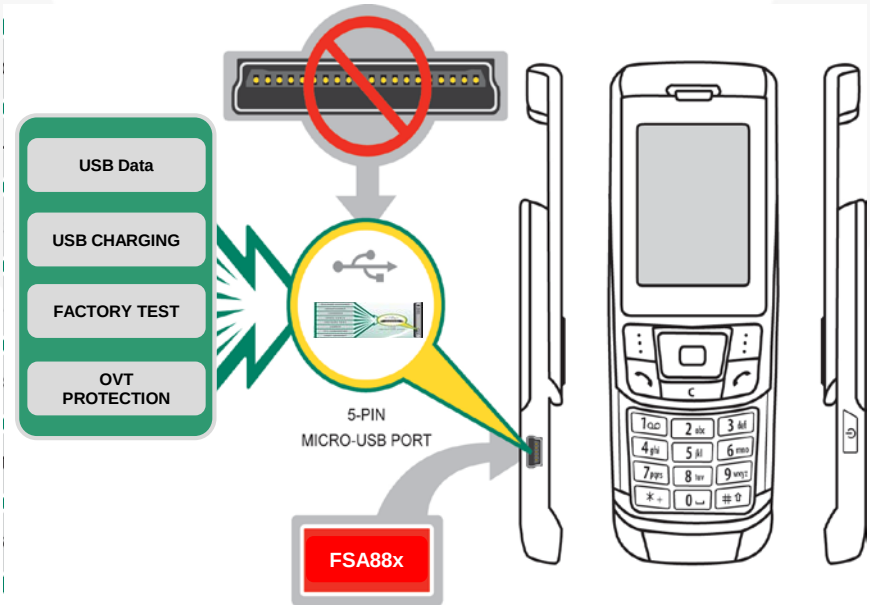


Figure 1. Mobile Phone Example

Ordering Information

Part Number	Operating Temperature Range	Top Mark	Package
FSA880UMX	-40 to +85°C	KU	16-Lead, Ultrathin Molded Leadless Package (UMLP), 1.8 mm x 2.6 mm x 0.55 mm, 0.4 mm Pitch
FSA881UMX	-40 to +85°C	KX	16-Lead, Ultrathin Molded Leadless Package (UMLP), 1.8 mm x 2.6 mm x 0.55 mm, 0.4 mm Pitch

Block Diagram

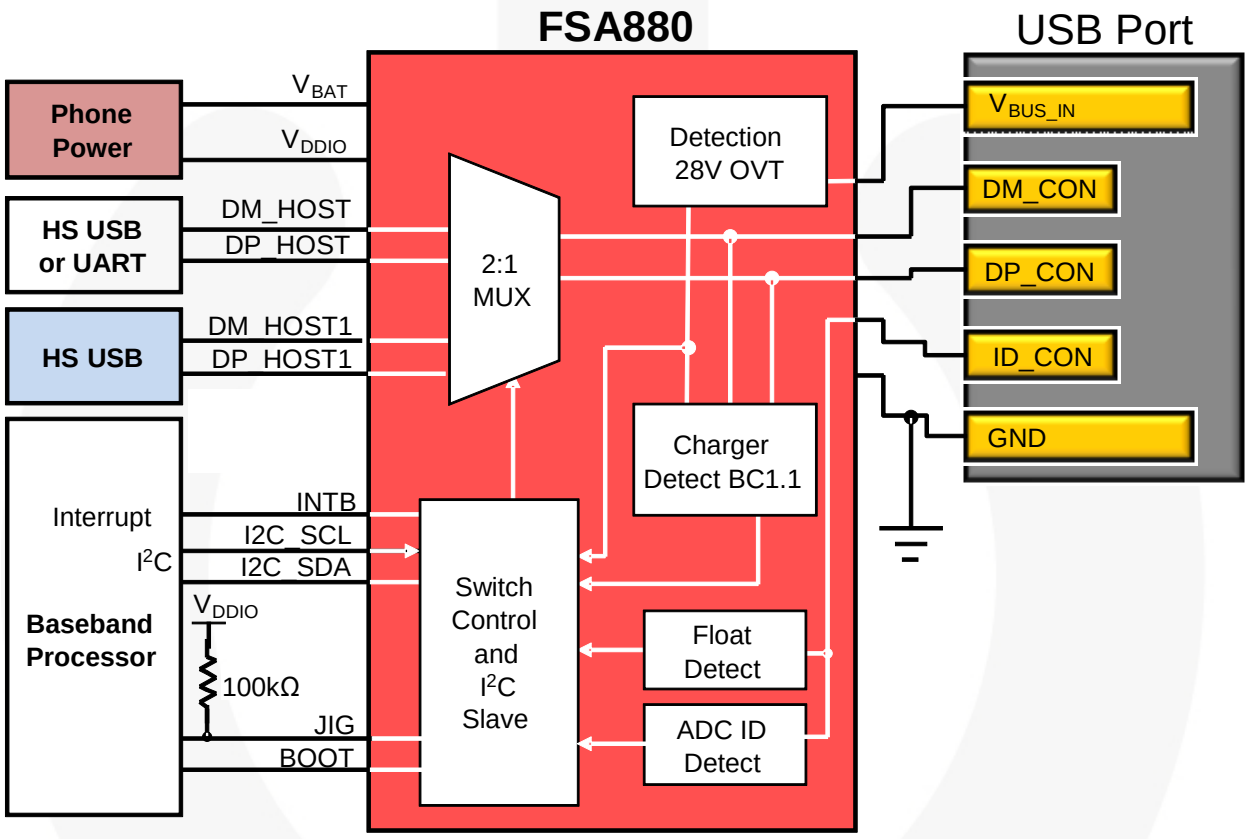


Figure 2. Block Diagram

Pin Configuration

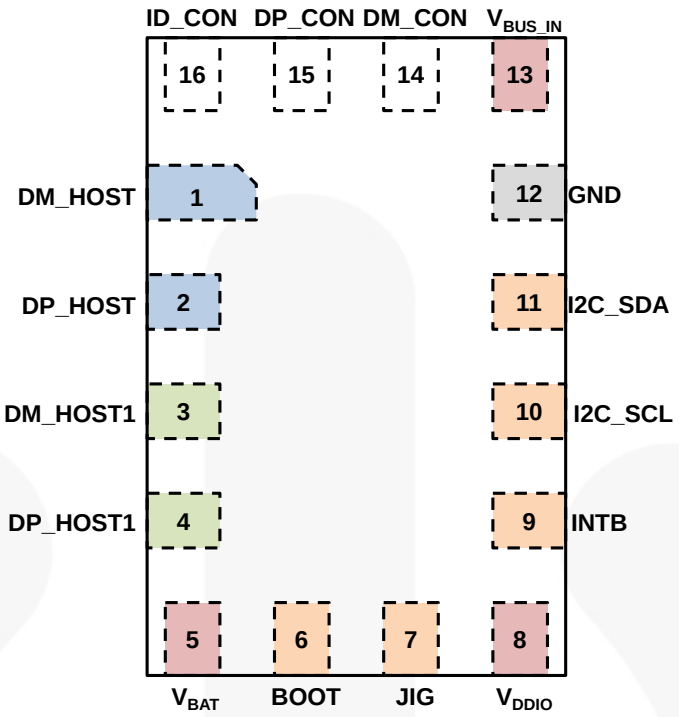


Figure 3. Pin Assignment (Through View)

Pin Descriptions

Name	Pin #	Type	Default State	Description
USB/UART Interface				
DP_HOST	2	Signal Path	Open	D+ signal switch path, dedicated USB port to be connected to the resident USB / UART on the phone. Default port for all USB accessories and USB factory modes.
DM_HOST	1	Signal Path	Open	D- signal switch path, dedicated USB port to be connected to the resident USB / UART on the phone. Default port for all USB accessories and USB factory modes.
V_{BUS_IN}	13	Input	N/A	Input voltage supply pin to be connected to the VBUS pin of the USB connector
USB/UART Interface 1				
DM_HOST1	3	Signal Path	Open	D- signal switch path, dedicated USB port to be connected to the secondary resident USB / UART on the phone. Default port for UART factory modes.
DP_HOST1	4	Signal Path	Open	D+ signal switch path, dedicated USB port to be connected to the secondary resident USB / UART on the phone. Default port for UART factory modes.
Connector Interface				
GND	12	Ground	N/A	Ground
ID_CON	16	Signal Path	Open	Connected to the USB connector ID pin and used for detecting accessories
DP_CON	15	Signal Path	Open	Connected to the USB connector D+ pin; depending on the signaling mode, this pin can be switched to DP_HOST or RxD_HOST pins.
DM_CON	14	Signal Path	Open	Connected to the USB connector D- pin; depending on the signaling mode, this pin can switched to DM_HOST or TxD_HOST pins.
Power Interface				
V_{DDIO}	**8**	Power	N/A	Input baseband interface I/O supply pin
V_{BAT}	**5**	Power	N/A	Input voltage supply pin to be connected to the mobile phone battery output or to an internal regulator on the phone
Factory Interface				
JIG	7	FSA880: Open-Drain Output FSA881: CMOS Output	FSA880:Hi-Z FSA881: LOW	Output control signal and used by the processor for factory test modes FSA880: Active LOW open-drain output FSA881: Active HIGH CMOS output
BOOT	6	CMOS Output	LOW	Output control signal and used by the processor for factory test modes
I^2C Interface				
I2C_SCL	10	Input	Hi-Z	I^2C serial clock signal to be connected to the phone-based I^2C master
I2C_SDA	11	Open-Drain I/O	Hi-Z	I^2C serial data signal to be connected to the phone-based I^2C master
INTB	9	CMOS Output	LOW	Interrupt active LOW output used to prompt the phone baseband processor to read the I^2C register bits, indicate a change in ID_CON pin status or accessories' attach status

Note:

1. LOW = V_{OL} or V_{IL}; HIGH = V_{OH} or V_{IH}.

1. Functionality

The FSA88x is USB port accessory detector and switch with integrated 28 V over-voltage tolerance. Fully controlled using I^2C, FSA88x enables high-speed USB 2.0 Standard Downstream Port (SDP), USB Charging Downstream Port (CDP) battery charger, USB Dedicated Charging Port (DCP) charger data cables to use a common connector micro or mini USB 2.0 port. Factory-mode cables can be detected and switched to use either the UART or USB data path. The FSA88x can be programmed for manual switching or automatic switching of data paths.

The architecture uses ID pin detection for convenient factory testing. Figure 9 - Figure 13 show the FSA88x passing the USB eye compliance test with ample margin.

1.1. Functional Overview

The FSA88x is designed for minimal software requirements for proper operation. The flow diagram in Figure 4 walks through the fundamental steps of operation and contains references to more detailed information.

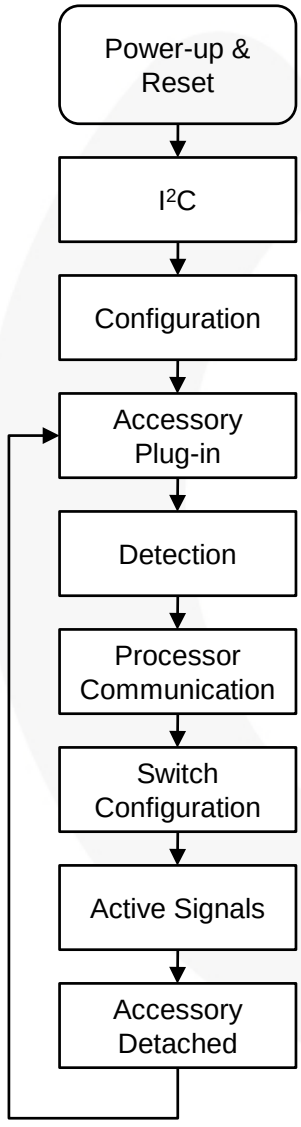


Figure 4. Basic Operation Flow

Flow Diagram	State	Datasheet Section	Description
	Power-Up & Reset	*Section 2*	Applies power to the device and resets state of the device
	I^2C	*Section* 3	Communication with device through I^2C
	Configuration	*Section* 4	Configures the device using I^2C and the internal registers (which can be bypassed during power-up)
	Detection	*Section 5*	Manages accessory detection, including attachment and detachment
	Processor Communication	*Section 6*	How the detection of the accessory is indicated to the processor
	Switch Configuration	*Section 7*	Configuration of switches based on detection
	Active Signal	*Section 8*	Signal performance of selected configuration

2. Power-Up & Reset

The FSA88x does not need special power sequencing for correct operation. The main power is provided by V_{BAT} only. V_{DDIO} is only used for I^2C interface and interrupt processing.

Table 1 summarizes the enabled features of each power state. The valid voltages levels for each power supply can be found in Section 9.

Table 1. Power States Summary

Valid V_{BUS_IN}	Valid V_{BAT}	Valid V_{DDIO} (1)	Power State	Enabled Functionality	
				Processor Communication (I^2C & Interrupts)	Detection
X	N	N	Power Down	NO	
X	N	Y (2)	Not Typical	Illegal State	
X	Y	N	Powered from V_{BAT}	NO	YES
X	Y	Y	Powered from V_{BAT}	YES	YES

Notes:
1. V_{DDIO} is expected to be the same supply used by the baseband I/Os.
2. Typically V_{DDIO} is only present when V_{BAT} is valid.
3. X = Don't care.

2.1. Reset

When the device is reset, all the registers are initialized to the default values shown in Section 9.9 and all switch paths are open. After reset or power up, FSA88x enters Standby Mode and is ready to detect accessories sensed on its V_{BUS_IN} and / or ID_CON pins.

2.1.1. Hardware Reset

Power-on reset is caused by the initial rising edge of V_{BAT}

2.1.2. Software Reset

The device can be reset through software by writing to the Reset bit in the Register (1BH).

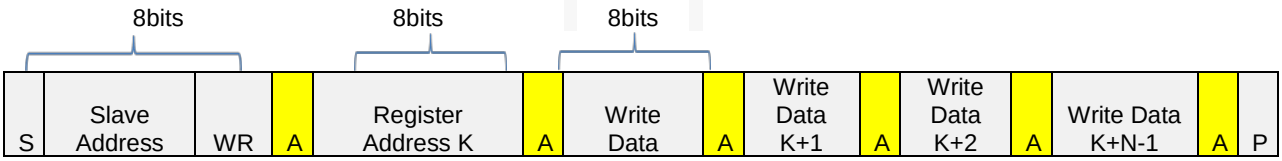
3. I²C

The FSA88x integrates a full fast-mode I²C slave controller compliant with the I²C specification version 2.1. The FSA88x I²C interface runs up to 400 kHz.

The slave address is shown in Table 2. Status information and configuration occurs via the I²C interface. *Please see Table 7 for more information.*

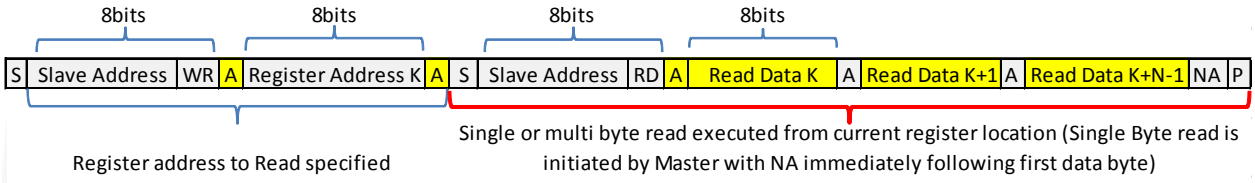
Table 2. I²C Slave Address

Name	Size (Bits)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Slave Address	8	0	1	0	0	1	0	1	Read / Write



Note: Single-byte write is initiated by Master with P immediately following first data byte.

Figure 5. I²C Write Sequence



Note: If Register is not specified Master will begin read from current register. In this case only sequence showing in Red bracket is needed

Figure 6. I²C Read Sequence

From Master to Slave
From Slave to Master
S Start Condition
A Acknowledge (SDA Low)
NA NOT Acknowledge (SDA High)
WR Write=0
RD Read =1
P Stop Condition

4. Configuration

FSA88x requires minimal configuration for proper detection and reporting. The following steps provide full configuration.

1. Write Control register (02h) to configure manual or automatic switching modes.
   a. If using manual switching modes, write Manual SW 1 register (13h) to configure switches.
2. Write Control register (02h) to clear INT Mask bit. This enables interrupts to the baseband.

5. Detection

The FSA88x monitors both V_{BUS_IN} and ID_CON to detect accessories. The ID_CON detection is a "resistive detection" that reads the resistance to GND on the ID_CON pin to determine the accessory attached. Table 3 shows the assignment of accessories based on resistor values. FSA88x can also detect accessories with ID resistances outside the specified ranges. The FSA88x detects these unknown accessories in the same manner as the defined accessories and interrupts the baseband processor and provides the correct ADC value, as shown in Table 3.

Table 3. ID_CON Accessory Detection

ADC Code					Equivalent R_{ID}			Description
4	3	2	1	0	Min.	Target	Max.	
1	0	1	0	1	117.4 kΩ	121 kΩ	124.6 kΩ	Unknown Accessory
1	0	1	1	0	145.5 kΩ	150 kΩ	154.5 kΩ	Unknown Accessory
1	0	1	1	1	176.4 kΩ	200 kΩ(4)	206 kΩ	Travel Adapter (TA) or Car Kit Type 1 Charger
1	1	0	0	0	247.3 kΩ	255 kΩ	262.7 kΩ	Factory Mode Boot OFF-USB
1	1	0	0	1	291.9 kΩ	301 kΩ	310.1 kΩ	Factory Mode Boot ON-USB
1	1	0	1	0	354 kΩ	365 kΩ	375.9 kΩ	Unknown Accessory
1	1	0	1	1	428.7 kΩ	442 kΩ(4)	455.3 kΩ	Unknown Accessory
1	1	1	0	0	507.3 kΩ	523 kΩ	538.7 kΩ	Factory Mode Boot OFF-UART
1	1	1	0	1	600.4 kΩ	619 kΩ	637.6 kΩ	Factory Mode Boot ON-UART
1	1	1	1	0	750 kΩ	1000 kΩ	1030 kΩ	Unknown Accessory
Not 'h1F or any code above					3 MΩ	None of the above ranges		Unknown Accessory

Note:
4. These accessories need VBUS to be valid in order to be detected since they are charger accessories.

5.1. Factory Cable Detection

Factory modes are initiated with the attachment of special test hardware, called a "JIG box" for factory testing. The FSA88x automatically configures switch paths to any of the factory-mode accessories when the appropriate resistor is sensed on the ID_CON pin. A change of resistor on the ID_CON pin dynamically switches between factory modes and auto-configures the appropriate switch paths without detaching and attaching the cable.

The different factory mode accessories with the associated resistor values (1% standard resistors) on the ID_CON pin and the JIG and BOOT logic states are listed in Table 4. The FSA88x allows both HS USB and FS USB in addition to UART signals to be passed on both ports with matched performance. This allows greater flexibility when designing with the FSA88x.

JIG output signals when a factory mode accessory is plugged in and BOOT output signals the mobile phone to boot up. The switch paths for factory modes are shown in Table 4.

Table 4. ID_CON Factory Cable Detection

Configuration Type		DP_CON	DM_CON	ID_CON			BOOT	FSA880 JIG	FSA881 JIG
Factory Mode Jig: UART	Boot_On	DP_HOST1	DM_HOST1	600kΩ	619kΩ	637kΩ	HIGH	LOW	HIGH
	Boot_Off	DP_HOST1	DM_HOST1	507kΩ	523kΩ	538kΩ	LOW	LOW	HIGH
Factory Mode Jig: USB	Boot_On	DP_Host	DM_Host	292kΩ	301kΩ	310kΩ	HIGH	LOW	HIGH
	Boot_Off	DP_Host	DM_Host	247kΩ	255kΩ	262kΩ	LOW	LOW	HIGH

The FSA88x detection algorithms monitor both the V_{BUS} and ID pins of the USB interface. Based on the detection results, multiple registers are updated and the INTB pin is asserted to indicate to the baseband processor that an accessory was detected and to read the registers for the complete information. The detection algorithm allows the application to control the timing of the detection algorithm and the configuration of the internal switches. The flow diagram in Figure 7 shows the operation of the detection algorithm.

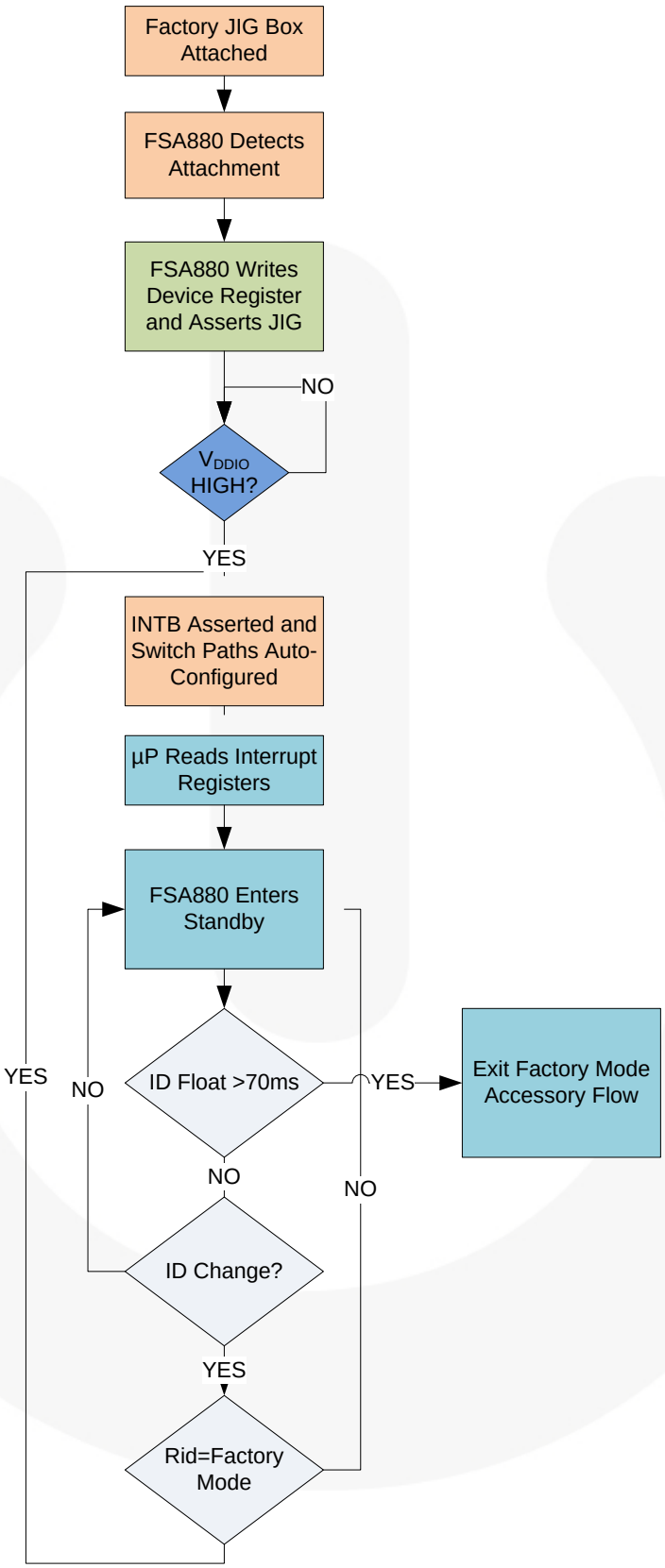


Figure 7. Factory Cable Detection Flow Chart (FSA880)

5.2. USB Port Detection

The multiple types of USB 2.0 ports the FSA88x can detect are summarized in Table 5.

Table 5. ID_CON and VBUS Detection Table for USB Devices

V_{BUS_IN}	DP_CON	DM_CON	ID_CON resistance to GND			Accessory Detected[5]
			Min.	Typ.	Max.	
5V	Not Checked	Not Checked	174.6 kΩ	200 kΩ	206 kΩ	TA (travel adapter) Charger (180 kΩ) and Car Kit Charger Type 1 only (200 kΩ)[6]
5V	Shorted to DM_CON	Shorted to DP_CON	3 MΩ	Open	Open	USB Dedicated Charging Port, Travel Adapter or Dedicated Charger (DCP)[6]
5V	DP_HOST	DM_HOST	3 MΩ	Open	Open	USB Charging Downstream Port (CDP)[6]
5V	DP_HOST	DM_HOST	3 MΩ	Open	Open	USB Standard Downstream Port (SDP)[6]

Notes:

5. The accessory type is reported in the Device Type 1 (0Ah) register for each valid accessory detected.
6. The FSA88x follows the Battery Charging 1.1 specification, which uses DP_CON and DM_CON to determine the USB accessory attached. *Refer to Battery Charging 1.1 specification for further details.*

For SDP and CDP USB accessories, the following pin mapping is automatically configured:

- DP_HOST = DP_CON
- DM_HOST = DM_CON

For DCP charger, the DP_HOST and DM_HOST switches are open. For all USB accessories V_{BUS_IN} is Over-Voltage Tolerance (OVT) up to 28 V.

6. Processor Communication

Typical communication steps between the processor and the FSA88x during accessory detection are:

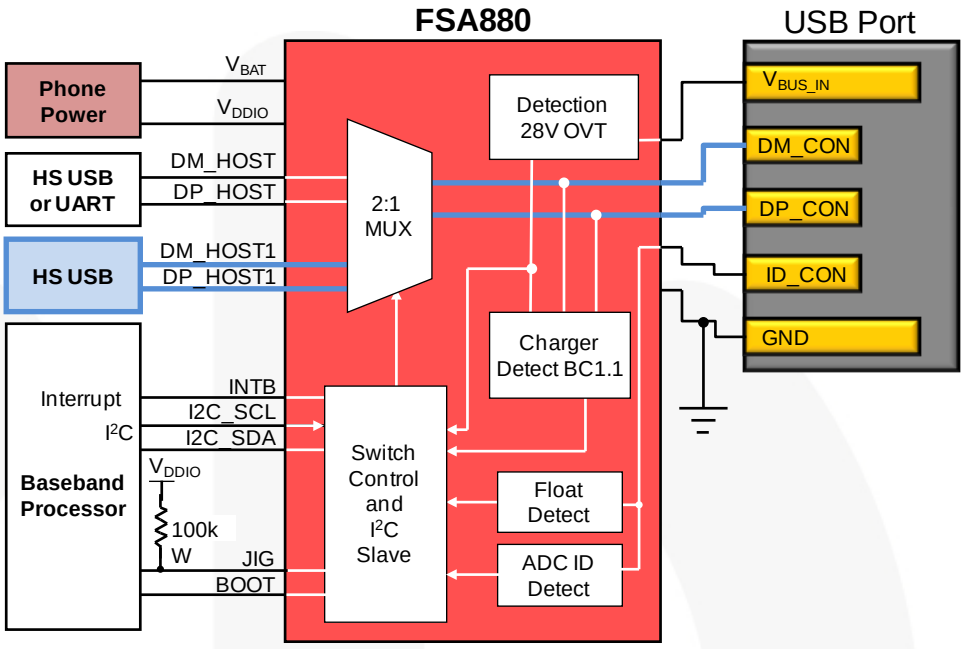
1. INTB is asserted LOW, indicating change in accessory detection.
2. Processor reads Interrupt 1 (03h) register to determine if an attach or detach event was detected.
3. Processor reads Status registers to determine the exact accessory detected.
   a. Device Type 1 (0Ah): Indicates which USB, Car Kit CDP, or DCP accessory was detected.
   b. Device Type 2 (0Bh): Indicates which factory mode or unknown accessory was detected.

7. Switch Configuration

FSA88x devices have two modes of operation when configuring the internal switches. The FSA88x can auto-configure the switches or the switches can be configured manually by the processor. Typical applications use Auto-Configuration Mode and do not require interaction with the baseband to configure the switches correctly.

7.1. Configurations

USB Accessories and Factory Cables:
DP_CON=DP_HOST
DM_CON=DM_HOST



UART Factory Cables:
DP_CON=DP_HOST1
DM_CON=DM_HOST1

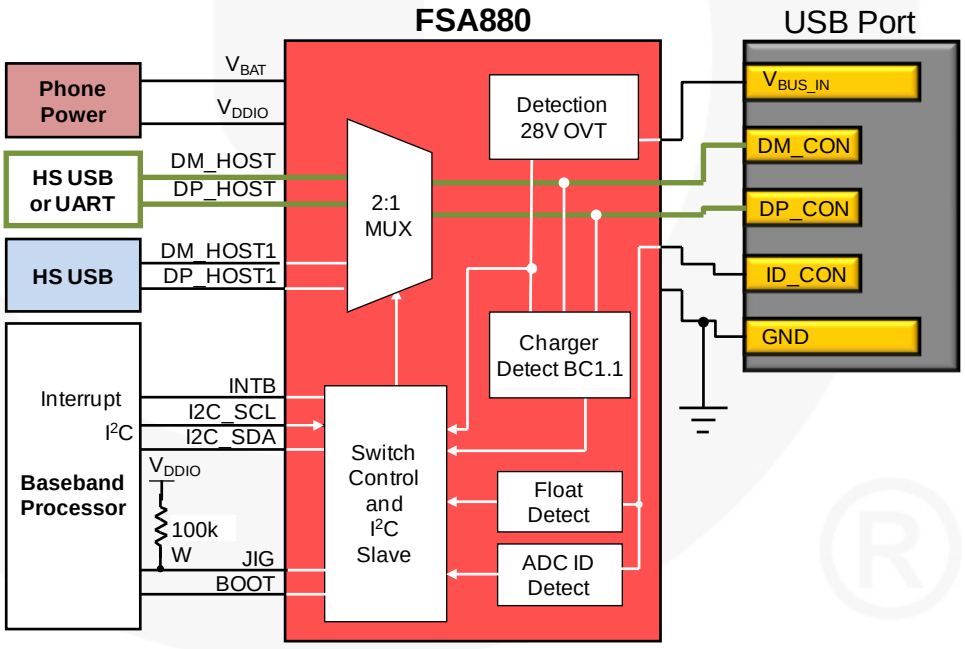


Figure 8. Switch Configurations

7.2. Manual Switching

Manual switching is enabled by writing the following registers:

- Manual Switch 1 (13h): Configures the switches for DM_CON, and DP_CON.
- Manual Switch 2 (14h): Configures the BOOT, and JIG pins.

8. Active Signal Performance

8.1. HS USB Data

8.1.1. DP_HOST/DM_HOST

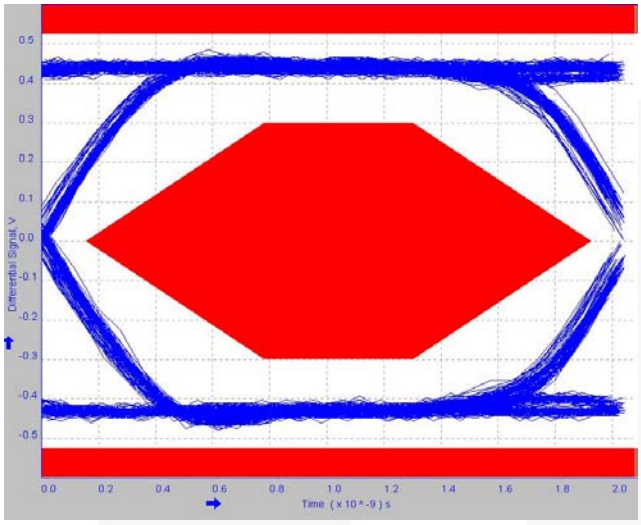


Figure 9. Pass Through Eye Compliance Testing Input Signal

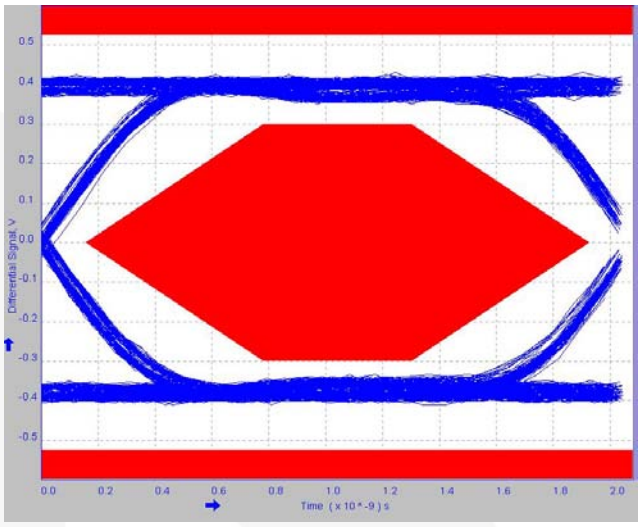


Figure 10. USB 2.0 Eye Compliance Test Results at Output

8.1.2. DP_HOST1/DM_HOST1

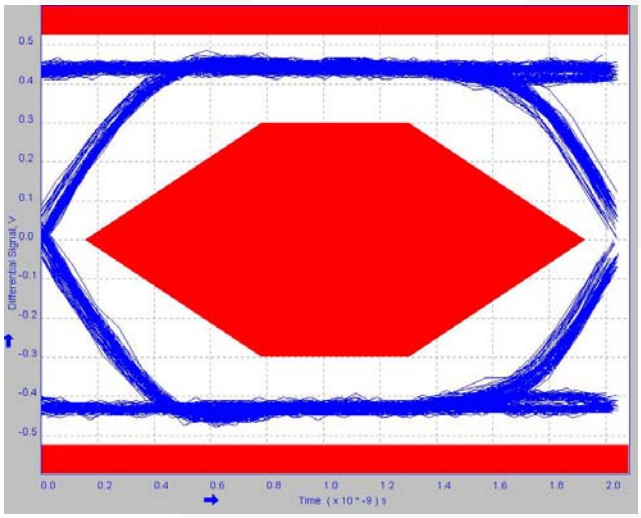


Figure 11. Pass-Through Eye Compliance Testing Input Signal

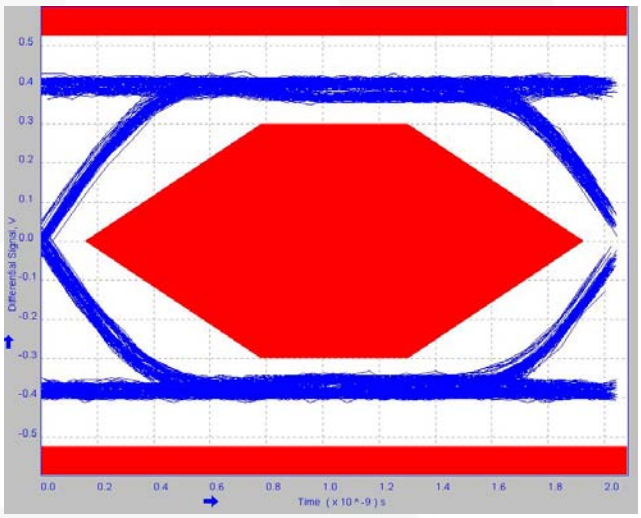


Figure 12. USB 2.0 Eye Compliance Test Results at Output

8.2. Full-Speed USB

8.2.1. DP_HOST/DM_HOST

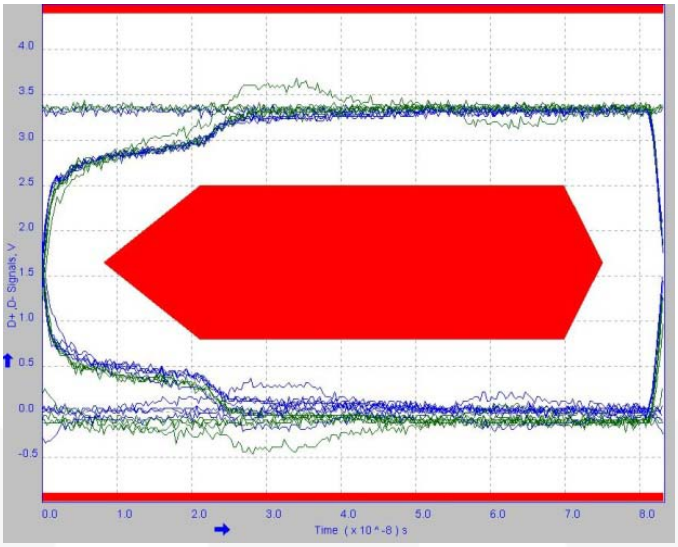


Figure 13. USB FS Eye Compliance Testing

8.2.2. DP_HOST1/DM_HOST1

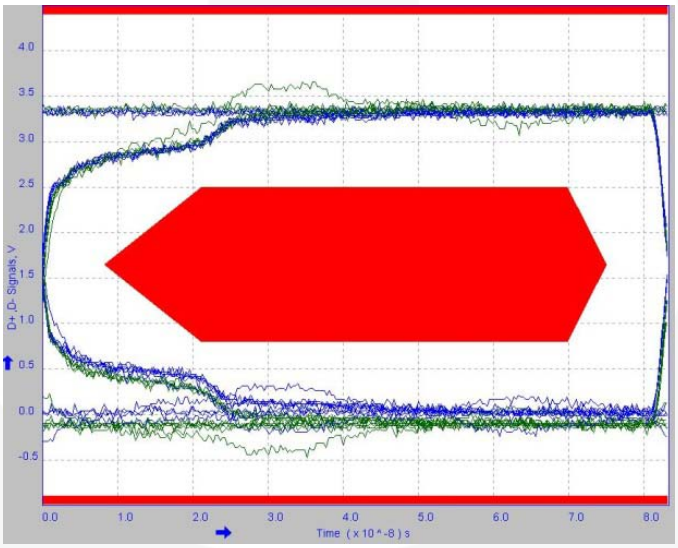


Figure 14. USB FS Eye Compliance Testing

9. Product Specifications

9.1. Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter			Min.	Max.	Unit
V_{BAT}	Supply Voltage from Battery			-0.5	6.0	V
V_{BUS_IN}	Supply Voltage from USB Connector			-0.5	28.0	V
V_{SW}	Switch I/O Voltage	USB		-1.0	6.0	V
		UART		-1.0	6.0	
I_{IK}	Input Clamp Diode Current			-50		mA
I_{SW}	Switch I/O Current (Continuous)	USB at T_A=85°C			25	mA
		UART at T_A=85°C			12	
I_{SWPEAK}	Peak Switch Current (Pulsed at 1ms Duration, <10% Duty Cycle)				150	mA
T_{STG}	Storage Temperature Range			-65	+150	°C
T_J	Maximum Junction Temperature				+150	°C
T_L	Lead Temperature (Soldering, 10 Seconds)				+260	°C
ESD	IEC 61000-4-2 System ESD	USB Connector Pins (DP_CON, DM_CON, V_{BUS_IN}, ID_CON) to GND	Air Gap	15		kV
			Contact	8		
	Human Body Model, JEDEC JESD22-A114		All Pins	4		
	Charged Device Model, JEDEC JESD22-C101		All Pins	2		

9.2. Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{BAT}	Battery Supply Voltage		3.0		4.4	V
V_{BUSIN}	V_{BUS_IN} Voltage		4.0		5.5	V
V_{DDIO}	Processor Supply Voltage		1.8		3.6	V
V_{SW}	Switch I/O Voltage	USB Path Active	0		3.6	V
		UART Path Active	0		3.6	
ID_{CAP}	Capacitive Load on ID_CON Pin for Reliable Accessory Detection				1.0	nF
T_A	Operating Temperature		-40		+85	ºC

9.3. Switch Path DC Electrical Characteristics

All typical values are at T_A=25°C unless otherwise specified.

Symbol	Parameter	V_{BAT} (V)	Conditions	T_A = -40 to +85°C			Unit
				Min.	Typ.	Max.	
Host Interface Pins (BOOT, JIG, INTB)							
V_{OH}	Output High Voltage (FSA881 JIG Output)	3.0 to 4.4	I_{OH}=-2 mA	0.8•V_{BAT}			V
V_{OH}	Output High Voltage (just BOOT & INTB Outputs)(7)	3.0 to 4.4	I_{OH}=-2 mA	0.7•V_{DDIO}			V
V_{OL}	Output Low Voltage (INTB, JIG & BOOT Outputs)	3.0 to 4.4	I_{OL}=3 mA			0.4	V
I^2C Interface Pins – Fast Mode (I2C_SDA, I2C_SCL)							
V_{IL}	Low-Level Input Voltage	3.0 to 4.4				0.3•V_{DDIO}	V
V_{IH}	High-Level Input Voltage	3.0 to 4.4		0.7•V_{DDIO}			V
V_{HYS}	Hysteresis of Schmitt Trigger Inputs	3.0 to 4.4	V_{DDIO}>2 V	0.05 V_{DDIO}			V
			V_{DDIO}<2 V	0.1 V_{DDIO}			V
V_{OL1}	Low-Level Output Voltage at 3 mA Sink Current (Open-Drain)	3.0 to 4.4	V_{DDIO}>2 V			0.4	
			V_{DDIO}<2 V			0.2•V_{DDIO}	V
I_{I2C}	Input Current of I2C_SDA and I2C_SCL Pins	3.0 to 4.4	Input Voltage 0.26 V to 2.34 V	-10		10	µA
Switch OFF Characteristics							
I_{OFF}	Power-Off Leakage Current	0	All Data Ports V_{SW}=0 V to 4.4 V			10	µA
$I_{NO(OFF)}$	Off Leakage Current	3.0 to 4.4	V_{BAT}=4.4 V; I/O Pins=0.3 V, 4.1 V, or Floating	-0.100	0.001	0.100	µA
I_{IDSHRT}	Short-Circuit Current	3.0 to 4.4	Current Limit if ID_CON=0 V		1		mA
USB Switch ON Path							
R_{ONUSB}	USB Switch On Resistance(8)	3.0 to 4.4	$V_{D+/D-}$=0 V, 0.4 V; I_{ON}=8 mA		8	10	Ω
			V_{SW}=0 V, 3.6 V; I_{ON}=30 mA		25	30	Ω
VBUS Path							
V_{BUSIN}	V_{BUS_IN} Valid Threshold			0.8		4.0	V
R_{BUS}	V_{BUS_IN} Resistance to GND				3		MΩ
UART Switch ON Paths							
V_{ASR_UART}	Analog Signal Range	3.0 to 4.4		0		3.6	V
R_{ONUART}	UART Switch On Resistance	3.0 to 4.4	$V_{D+/D-}$=0 V, 0.4 V; I_{ON}=8 mA		8	10	Ω
			V_{SW}=0 V, 3.6 V; I_{ON}=30 mA		25	30	
Total Current Consumption							
I_{CCSL}	Battery Supply Standby Mode Current (No Accessory Attached)	3.0 to 4.4	No Accessory, Static Current During Standby Mode		15	25	µA
I_{CCSLWA}	Battery Supply Standby Mode Current with Accessory Attached(7)	3.0 to 4.4	With non-Factory Mode Accessories Attached		30	40	µA
			With Factory Mode Accessories Attached(9)		100	120	µA

Notes:

7. Limits based on electrical characterization data.
8. On resistance is the voltage drop between the two terminals at the indicated current through the switch.
9. Factory mode accessories leave the detection circuitry active after attach to allow detection of ID changes without an attach.

9.4. Capacitance

Symbol	Parameter	V_{BAT} (V)	Conditions	T_A = -40 to +85°C			Unit
				Min.	Typ.	Max.	
C_{ON}	DP_CON, DM_CON On Capacitance	3.8	V_{BIAS}=0.2 V, f=1 MHz		6		pF
C_I	Capacitance for Each I/O Pin	3.8			5		pF

9.5. I²C DC Electrical Characteristics

Symbol	Parameter	V_{BAT} (V)	Conditions	T_A = -40 to +85°C		Unit
				Min.	Max.	
Fast Mode (I2C_SDA, I2C_SCL)						
V_{IL}	Low-Level Input Voltage	3.0 to 4.4			0.3•V_{DDIO}	V
V_{IH}	High-Level Input Voltage	3.0 to 4.4		0.7•V_{DDIO}		V
V_{hys}	Hysteresis of Schmitt Trigger Inputs	3.0 to 4.4	V_{DDIO}>2 V	0.05 V_{DDIO}		V
			V_{DDIO}<2 V	0.1 V_{DDIO}		V
V_{OL1}	Low-Level Output Voltage at 3 mA Sink Current (Open-Drain)	3.0 to 4.4	V_{DDIO}>2 V		0.4	
			V_{DDIO}<2 V		0.2•V_{DDIO}	V
I_{i2C}	Input Current of I2C_SDA and I2C_SCL Pins	3.0 to 4.4	Input Voltage 0.26 V to 2.34 V	-10	10	µA

9.6. I²C AC Electrical Characteristics

Symbol	Parameter	Fast Mode		Unit
		Min.	Max.	
f_{SCL}	I2C_SCL Clock Frequency	0	400	kHz
$t_{HD;STA}$	Hold Time (Repeated) START Condition	0.6		µs
t_{LOW}	LOW Period of I2C_SCL Clock	1.3		µs
t_{HIGH}	HIGH Period of I2C_SCL Clock	0.6		µs
$t_{SU;STA}$	Set-up Time for Repeated START Condition	0.6		µs
$t_{HD;DAT}$	Data Hold Time	0	0.9	µs
$t_{SU;DAT}$	Data Set-up Time[10]	100		ns
t_r	Rise Time of I2C_SDA and I2C_SCL Signals[10,11]	20+0.1C_b	300	ns
t_f	Fall Time of I2C_SDA and I2C_SCL Signals[10,11]	20+0.1C_b	300	ns
$t_{SU;STO}$	Set-up Time for STOP Condition	0.6		µs
t_{BUF}	BUS-Free Time between STOP and START Conditions	1.3		µs
t_{SP}	Pulse Width of Spikes that Must Be Suppressed by the Input Filter	0	50	ns

Notes:

10. A fast-mode I²C Bus® device can be used in a Standard-Mode I²C Bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must be met. This is automatically the case if the device does not stretch the LOW period of the I2C_SCL signal. If a device does stretch the LOW period of the I2C_SCL signal, it must output the next data bit to the I2C_SDA line $t_{r\_max} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-Mode I²C bus specification) before the I2C_SCL line is released.
11. C_b equals the total capacitance of one bus line in pF. If mixed with high-speed devices, faster fall times are allowed by the I²C specification.

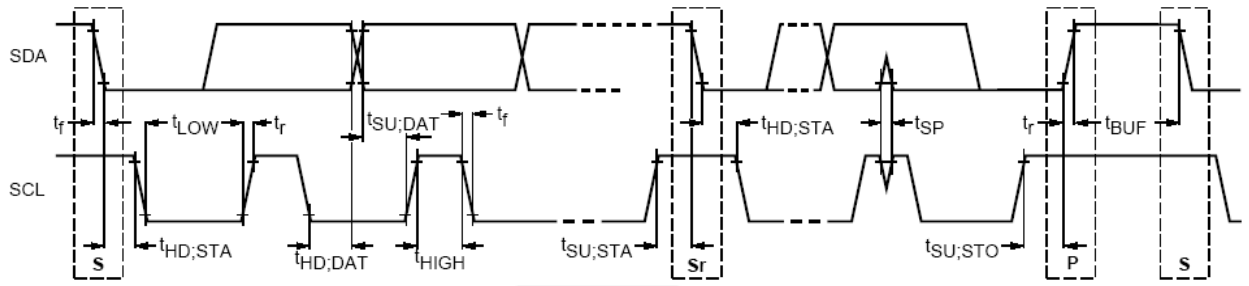


Figure 15. Definition of Timing for Full-Speed Mode Devices on the I²C Bus®

Table 6. I²C Slave Address

Name	Size (Bits)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Slave Address	8	0	1	0	0	1	0	1	R/W

9.7. Switch Path AC Electrical Characteristics

All typical values are for V_{BAT}=3.8 V at T_A=25°C unless otherwise specified.

Symbol	Parameter		Conditions	Min.	Typ.	Max.	Unit
Xtalk	Active Channel Crosstalk DP_CON to DM_CON	USB Mode	f=1 MHz, R_T=50 Ω, C_L=0 pF		-60		dB
			f=240 MHz, R_T=50 Ω, C_L=0 pF		-30		
O_{IRR}	Off Isolation	USB Mode	f=1 MHz, R_T=50 Ω, C_L=0 pF		-60		dB
$t_{SK(P)}$	Skew of Opposite Transitions of the Same Output (USB Mode)		t_r=t_f=750 ps (10-90%) at 240 MHz, C_L=0 pF, R_L=50 Ω		35		ps
t_{SW}	Time after *INT Mask* Cleared to “0” until INTB Goes LOW to Signal the Interrupt after Interruptible Event while *INT Mask* Bit Set to “1”		*See Figure 16 and Figure 17*		10		ms
t_{SDPDET}	Time from V_{BUS_IN} Valid to USB Switches Closed for USB Standard Downstream Port		*See Figure 17*		130		ms
t_{CHGOUT}	Time from V_{BUS_IN} Valid to USB Switches Closed for USB Charging Downstream Port (CDP)		*See Figure 18*		170		ms
$t_{JIGVBUS}$	Time from V_{BUS_IN} Valid to JIG LOW for Factory Mode Operation with V_{BUS_IN} Present		*See Figure 20*		200		ms
$t_{JIGVBUS}$	Time from V_{BUS_IN} Valid to JIG LOW for Factory Mode Operation without V_{BUS_IN} Present		*See Figure 21*		200		ms

9.8. Timing Diagrams

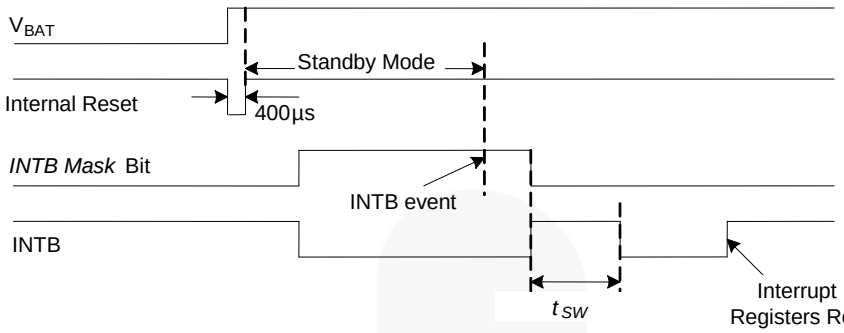


Figure 16. INT Mask to INTB Interrupt at Power-Up Timing Diagram

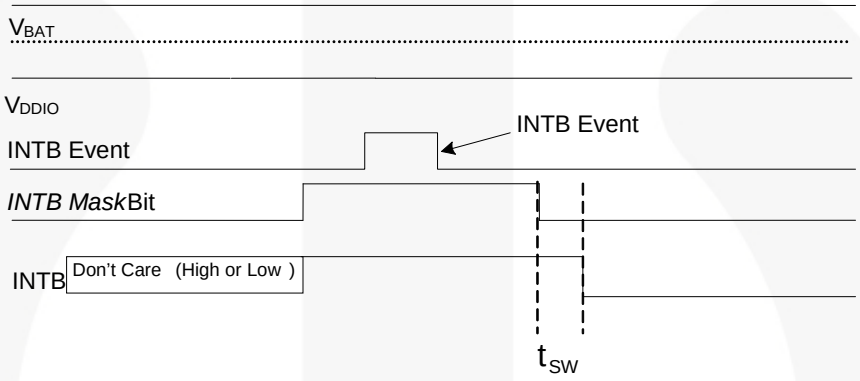


Figure 17. INT Mask to INTB Interrupt During Operation Timing Diagram

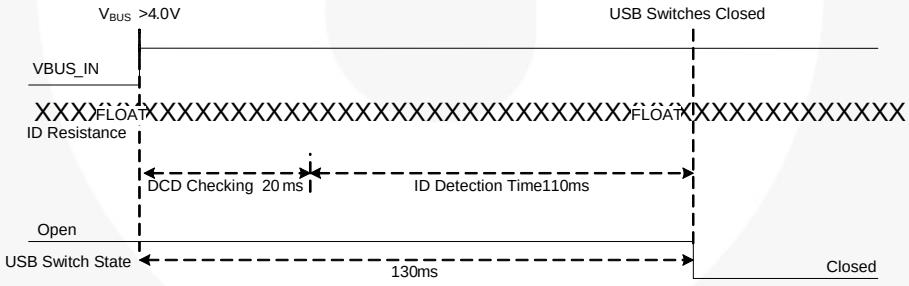


Figure 18. USB Standard Downstream Port Attach Timing

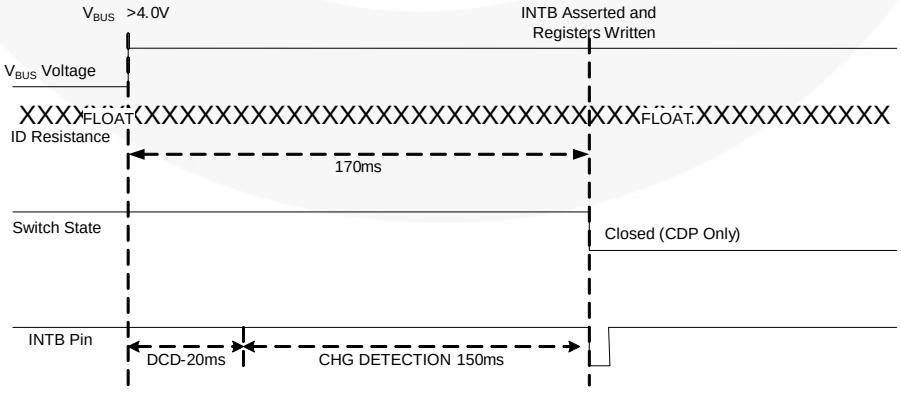


Figure 19. USB Charging Ports (DCP & CDP) Attach Timing

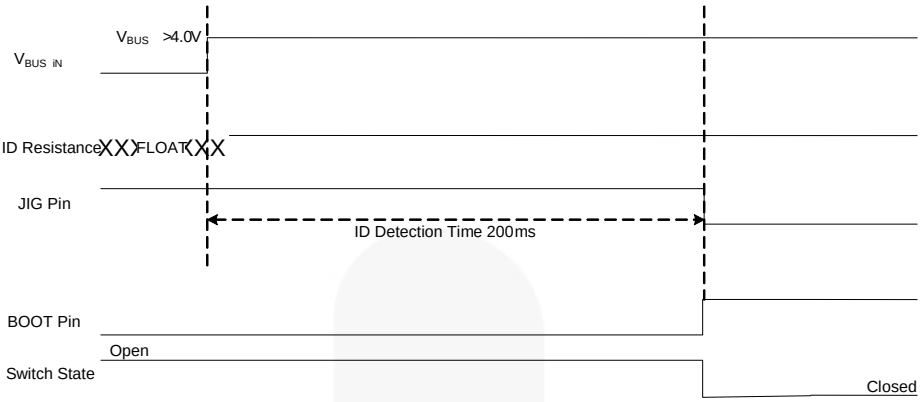


Figure 20. Jig Box Attach Timing (V_{BUS_IN} Valid)

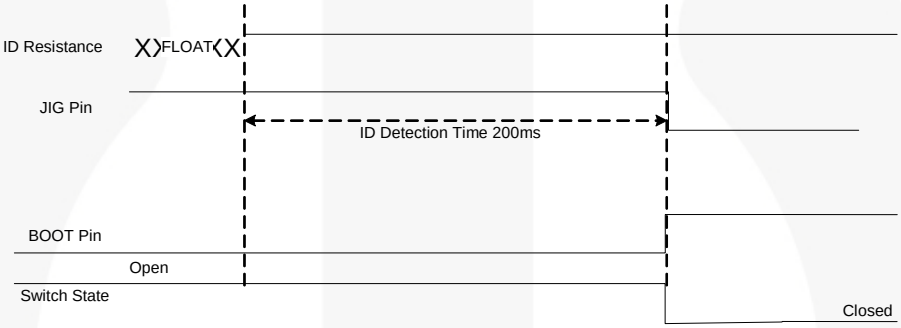


Figure 21. JIG Box Attach Timing without V_{BUS_IN}

9.9. Programmability Tables

Table 7. I²C Register Map

Address	Register	Type	Reset Value[12,13]	Bit 7[14]	Bit 6[14]	Bit 5[14]	Bit 4[14]	Bit 3[14]	Bit 2[14]	Bit 1[14]	Bit 0[14]
01H	Device ID	R	N/A	Revision Number					Vendor ID		
02H	Control	R/W	xxx0x1x1				Switch Open		Auto Config		INT Mask
03H	Interrupt	R/C	xxxxxx00							Detach	Attach
07H	ADC	R	xxx11111				ADC Value				
0AH	Device Type 1	R	x000x0xx		Dedicated Charger (DCP)	USB Charger (CDP)	Car Kit Type 1 & TA Charger		Standard USB (SDP)		
0BH	Device Type 2	R	0xxx0000	Unknown Accessory				Jig UART Off	Jig UART On	Jig USB Off	Jig USB On
13H	Manual SW 1	R/W	000000xx	D- Switching			D+ Switching				
14H	Manual SW 2	R/W	xxxx00xx					BOOT SW	JIG ON		
1BH	Reset	R/W	xxxxxxx0								Reset

Notes:
12. Write “0” to undefined register bits.
13. Values read from undefined register bits are not defined and invalid.
14. Do not use undefined register locations.

Table 8. Device ID

Address: 01h

Type: Read

Bit #	Name	Size (Bits)	Description
7:3	Revision Number	5	Rev 0.0 = 00000
2:0	Vendor ID	3	000: Fairchild Semiconductor

Table 9. Control

Address: 02h

Reset Value: xxx0x1x1

Type: Read/Write

Bit #	Name	Size (Bits)	Description
7:5	DoNotUse	3	N/A
4	Switch Open	1	1: Open all switches 0: Automatic switching by accessory status
3	DoNotUse	1	N/A
2	Auto Config	1	1: Automatic switching (also called auto-configuration) 0: Manual switching
1	DoNotUse	1	N/A
0	INT Mask	1	1: Mask interrupt – do not interrupt baseband processor 0: Unmask interrupt – interrupt baseband processor on change of state in Interrupt register

Table 10. Interrupt

Address: 03h

Reset Value: xxxxxx00

Type: Read/Clear

Bit #	Name	Size (Bits)	Description
7:2	DoNotUse	6	N/A
1	Detach	1	1: Accessory detached 0: Accessory not detached
0	Attach	1	1: Accessory attached 0: Accessory not attached

Table 11. Device Type 1

Address: 07h

Reset Value: xxx11111

Type: Read

Bit #	Name	Size (Bits)	Description
7:5	Reserved	3	NA
4:0	ADC Value	5	ADC value read from ID

Table 12. Device Type 1

Address: 0Ah

Reset Value: x00x00xx

Type: Read

Bit #	Name	Size (Bits)	Description
7	DoNotUse	1	N/A
6	Dedicated Charger (DCP)	1	1: USB dedicated charging port (DCP) charger detected 0: USB dedicated charging port (DCP) charger not detected
5	USB Charger (CDP)	1	1: USB charging downstream port (CDP) charger detected 0: USB charging downstream port (CDP) charger not detected
4	Car Kit Type 1 & TA Charger	1	1: Car Kit Type 1 or Travel Adapter (TA) detected 0: Car Kit Type 1 or Travel Adapter (TA) not detected
3	DoNotUse	1	N/A
2	Standard USB (SDP)	1	1: USB standard downstream port (SDP) detected 0: USB standard downstream port (SDP) not detected
1:0	DoNotUse	2	N/A

Table 13. Device Type 2

Address: 0Bh

Reset Value: 0xxx0000

Type: Read

Bit #	Name	Size (Bits)	Description
7	Unknown Accessory	1	1: Any accessory detected as unknown or an accessory that cannot be detected as being valid even though ID_CON is not floating 0: Unknown accessory not detected
6:4	DoNotUse	4	N/A
3	JIG_UART_OFF	1	1: Factory mode BOOT-OFF-UART detected 0: Factory mode BOOT-OFF-UART not detected

Bit #	Name	Size (Bits)	Description
2	JIG_UART_ON	1	1: Factory mode cable UART path with BOOT ON detected 0: Factory mode cable UART path with BOOT ON not detected
1	JIG_USB_OFF	1	1: Factory mode cable USB path with BOOT OFF detected 0: Factory mode cable USB path with BOOT OFF not detected
0	JIG_USB_ON	1	1: Factory mode cable USB path with BOOT ON detected 0: Factory mode cable USB path with BOOT ON not detected

Table 14. Manual S/W 1[15]

Address: 13h

Reset Value: 000000xx

Type: Read/Write

Bit #	Name	Size (Bits)	Description
7:5	DM_CON Switching	3	000: Open switch 001: DM_CON connected to DM_HOST of USB port 011: DM_CON connected to DM_HOST1 of UART port All other values: DoNotUse
4:2	DP_CON Switching	3	000: Open switch 001: DP_CON connected to DP_HOST of USB port 011: DP_CON connected to DP_HOST1 of UART port All other values: DoNotUse
1:0	DoNotUse	2	N/A

Note:

15. When switching between manual switch configurations on a single attach, the accessory must pass through an “000: Open Switch” state between configurations. Manual Modes must have an accessory attached prior to operation. The FSA88x does not configure per the Manual Modes register if an accessory has not been previously attached.

Table 15. Manual S/W 2

Address: 14h

Reset Value: xxxx00xx

Type: Read/Write

Bit #	Name	Size (Bits)	Description
7:4	DoNotUse	4	N/A
3	BOOT_SW	1	1: HIGH 0: LOW
2	JIG_ON	1	1: JIG output=GND (FSA880) or JIG output=HIGH (FSA881) 0: JIG output=High impedance (FSA880) or JIG output=LOW (FSA881)
1:0	DoNotUse	2	N/A

Table 16. Reset

Address: 1Bh

Reset Value: xxxxxx0

Type: Read/Write

Bit #	Name	Size (Bits)	Description
7:1	DoNotUse	6	N/A
0	Reset	1	1: Resets the FSA88x 0: Does not reset the FSA88x

10. Layout Guidelines

10.1. PCB Layout Guidelines for High-Speed USB Signal Integrity

1. Place FSA88x as close to the USB controller as possible. Shorter traces mean less loss, less chance of picking up stray noise, and less radiated EMI.
   a) Keep the distance between the USB controller and the device less than 25 mm (< one inch).
   b) For best results, this distance should be <18mm. This keeps it less than one quarter (¼) of the transmission electrical length.
2. Use an impedance calculator to ensure 90 Ω differential impedance for DP_CON and DM_CON lines.
3. Select the best transmission line for the application.
   a) For example, for a densely populated board, select an edge-coupled differential stripline.
4. Minimize the use of vias and keep HS USB lines on same plane in the stack.
   a) Vias are an interruption in the impedance of the transmission line and should be avoided.
   b) Try to avoid routing schemes that generally force the use of at least two vias: one on each end to get the signal to and from the surface.
5. Cross lines, only if necessary, orthogonally to avoid noise coupling (traces running in parallel couple).
6. If possible, separate HS USB lines with GND to improve isolation.
   a) Routing GND, power, or components close to the transmission lines can create impedance discontinuities.
7. Match transmission line pairs as much as possible to improve skew performance.
8. Avoid sharp bends in PCB traces; a chamfer or rounding is generally preferred.
9. Place decoupling for power pins as close to the device as possible.
   a) Use low-ESR capacitors for decoupling if possible.
   b) A tuned PI filter should be used to negate the effects of switching power supplies and other noise sources if needed.

10.2. Layout for GSM / TDMA Buzz Reduction

There are two possible mechanisms for TDMA / GSM noise to negatively impact FSA88x performance. The first is the result of large current draw by the phone transmitter during active signaling when the transmitter is at full or almost-full power. With the phone transmitter dumping large amounts of current in the phone GND plane; it is possible for there to be temporary voltage excursions in the GND plane if not properly designed. This noise can be coupled back through the GND plane into the FSA88x device and, although the FSA88x has very good isolation; if the GND noise amplitude is large enough, it can result in noise coupling to the FSA88x. The second path for GSM noise is through electromagnetic coupling onto the signal lines themselves.

In most cases, the noise introduced as a result is on the V_{BAT} and / or GND supply rails. Following are recommendations for PCB board design that help address these two sources of TDMA / GSM noise.

1. Provide a wide, low-impedance GND return path to both the FSA88x and to the power amplifier that sources the phone transmit block.
2. Provide separate GND connections to PCB GND plane for each device. Do not share GND return paths among devices.
3. Add as large a decoupling capacitor as possible (≥1µF) between the V_{BAT} pin and GND to shunt any power supply noise away from the FSA88x. Also add decoupling capacitance at the PA *(see the reference application schematic in Figure 22 for recommended decoupling capacitor values)*.
4. Add 33 pF shunt capacitors on any PCB nodes with the potential to collect radiated energy from the phone transmitter.
5. Add a series R_{BAT} resistor prior to the decoupling capacitor on the V_{BAT} pin to attenuate noise prior to reaching the FSA88x.

11. Reference Schematic

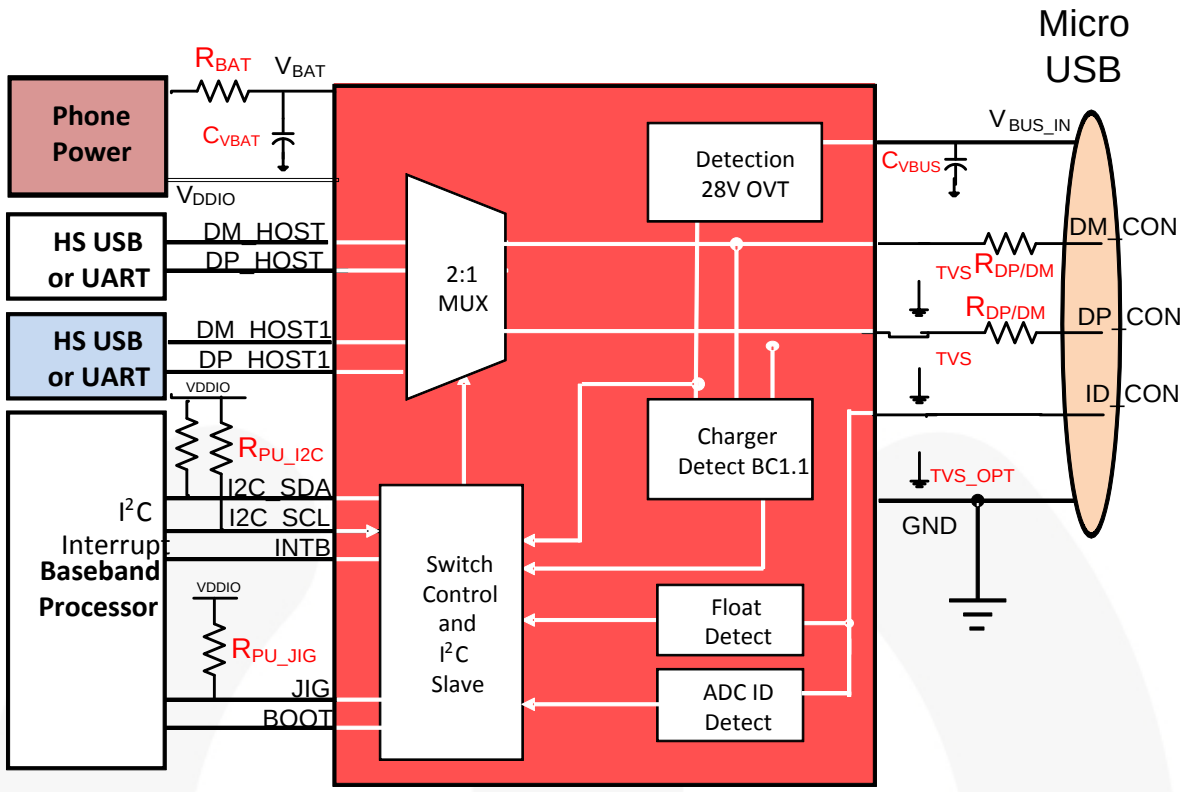
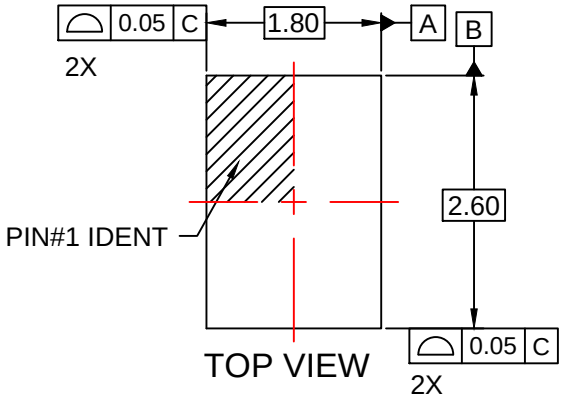


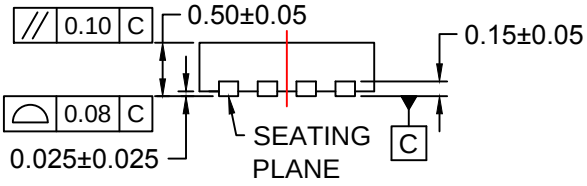
Figure 22. Reference Schematic

Table 17. Reference Schematic Component Values

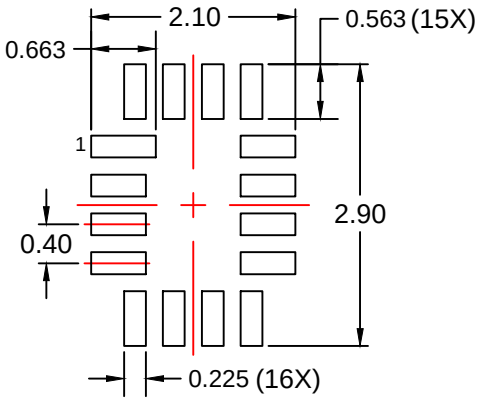
Symbol	Parameter	Recommended Value			Unit	Notes
		Min.	Typ.	Max.		
C_{VBUS}	V_{BUS_IN} Decoupling	1.0	4.7	10.0	µF	This is the recommended capacitance in the USB standard (for the downstream port V_{BUS} capacitance specification).
C_{VBAT}	V_{BAT} Decoupling Capacitance		1	10	µF	Increasing this capacitance can help reduce GSM / TDMA noise.
R_{BAT}	V_{BAT} Series Resistance		50	100	Ω	Adding series resistance can help reduce GSM / TDMA noise. Ensure that resistance is small enough to not reduce V_{BAT} levels under normal operation.
R_{PU_I2C}	I^2C Pull-up Resistance		4.7		kΩ	The actual value used must allow compliance to I^2C specification based on V_{DDIO} and bus capacitance.
R_{PU_JIG}	JIG Pull-up Resistance (FSA880 ONLY)		100		kΩ	Pull-up resistance for open-drain JIG pin.
$R_{DP/DM}$	DP_CON/DM_CON Series Resistance		2.2		Ω	Series resistance to improve surge performance of high-speed USB path.
TVS	High-Speed TVS Diodes		1		pF	Recommended high-speed TVS diodes to improve ESD performance.
TVS_OPT	Optional High-Speed TVS Diodes		1		pF	Optional high-speed TVS diodes to improve ESD performance.



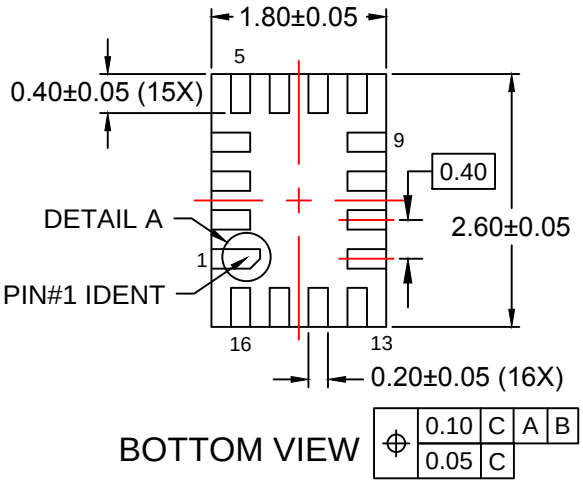
TOP VIEW



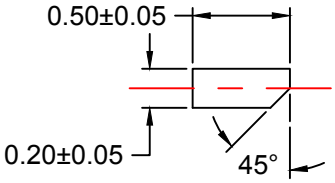
SIDE VIEW



RECOMMENDED
LAND PATTERN



BOTTOM VIEW



DETAIL A
SCALE : 2X

LEAD SHAPE AT PACKAGE EDGE

LEAD
OPTION 1
SCALE : 2X

LEAD
OPTION 2
SCALE : 2X

NOTES:

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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.fairchildsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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