FAIRCHILD SEMICONDUCTOR™

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74ABT16543
16-Bit Registered Transceiver with 3-STATE Outputs

General Description

The ABT16543 16-bit transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow. Each byte has separate control inputs, which can be shorted together for full 16-bit operation.

Features

- Back-to-back registers for storage
- Bidirectional data path
- A and B outputs have current sourcing capability of 32 mA and current sinking capability of 64 mA
- Separate control logic for each byte
- 16-bit version of the ABT543
- Separate controls for data flow in each direction
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability

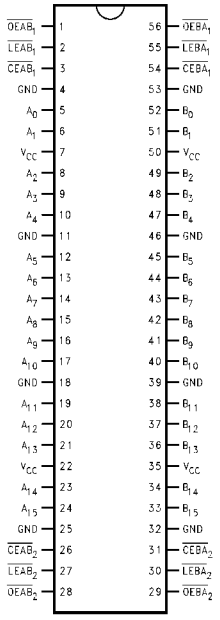
Ordering Code:

Order Number	Package Number	Package Description
74ABT16543CSSC	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74ABT16543CMTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

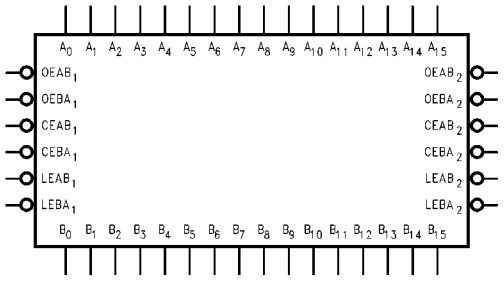
Pin Assignment for SSOP and TSSOP



Pin Descriptions

Pin Names	Description
$\overline{OEAB}_n$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}_n$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}_n$	A-to-B Enable Input (Active LOW)
$\overline{CEBA}_n$	B-to-A Enable Input (Active LOW)
$\overline{LEAB}_n$	A-to-B Latch Enable Input (Active LOW)
$\overline{LEBA}_n$	B-to-A Latch Enable Input (Active LOW)
A_0–A_{15}	A-to-B Data Inputs or B-to-A 3-STATE Outputs
B_0–B_{15}	B-to-A Data Inputs or A-to-B 3-STATE Outputs

Logic Symbol



Data I/O Control Table

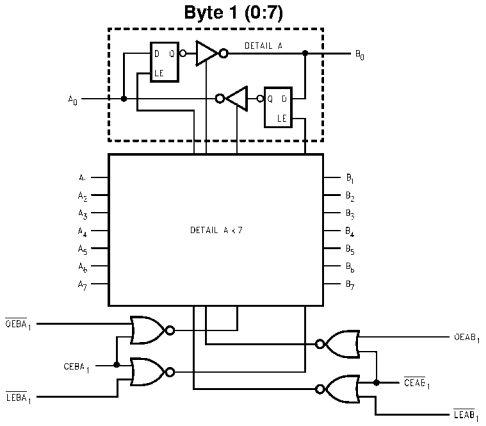
Inputs			Latch Status	Output Buffers
$\overline{CEAB}_n$	$\overline{LEAB}_n$	$\overline{OEAB}_n$	(Byte n)	(Byte n)
H	X	X	Latched	HIGH Z
X	H	X	Latched	—
L	L	X	Transparent	—
X	X	H	—	HIGH Z
L	X	L	—	Driving

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
A-to-B data flow shown;
B-to-A flow control is the same, except using $\overline{CEBA}_n$, $\overline{LEBA}_n$ and $\overline{OEBA}_n$

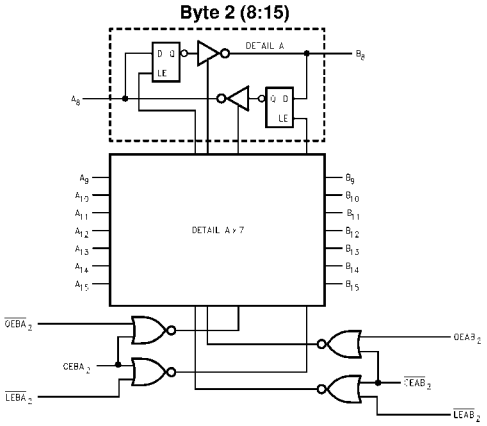
Functional Description

The ABT16543 contains two sets of D-type latches, with separate input and output controls for each. For data flow from A to B, for example, the A to B Enable ($\overline{CEAB}$) input must be low in order to enter data from the A port or take data from the B-Port as indicated in the Data I/O Control Table. With $\overline{CEAB}$ low, a low signal on ($\overline{LEAB}$) input makes the A to B latches transparent; a subsequent low to high transition of the $\overline{LEAB}$ line puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both low, the B output buffers are active and reflect the data present on the output of the A latches. Control of data flow from B to A is similar, but using the $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$. Each byte has separate control inputs, allowing the device to be used as two 8-bit transceivers or as one 16-bit transceiver.

Logic Diagrams



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

Storage Temperature	–65°C to +150°C
Ambient Temperature under Bias	–55°C to +125°C
Junction Temperature under Bias	–55°C to +150°C
V_{CC} Pin Potential to Ground Pin	–0.5V to +7.0V
Input Voltage (Note 2)	–0.5V to +7.0V
Input Current (Note 2)	–30 mA to +5.0 mA
Voltage Applied to Any Output in the Disable or Power-Off State	–0.5V to +5.5V
in the HIGH State	–0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current	–500 mA
Over Voltage Latchup (I/O)	10V

Recommended Operating Conditions

Free Air Ambient Temperature	–40°C to +85°C
Supply Voltage	+4.5V to +5.5V
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
Data Input	50 mV/ns
Enable Input	20 mV/ns
Clock Input	100 mV/ns

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage			–1.2	V	Min	I_{IN} = –18 mA (Non I/O Pins)
V_{OH}	Output HIGH Voltage	2.5 2.0					I_{OH} = –3 mA, (A_n, B_n) I_{OH} = –32 mA, (A_n, B_n)
V_{OL}	Output LOW Voltage			0.55	V	Min	I_{OL} = 64 mA, (A_n, B_n)
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 µA, (Non-I/O Pins) All Other Pins Grounded
I_{IH}	Input HIGH Current			1 1	µA	Max	V_{IN} = 2.7V (Non-I/O Pins) ((Note 3) V_{IN} = V_{CC} (Non-I/O Pins)
I_{BVI}	Input HIGH Current Breakdown Test			7	µA	Max	V_{IN} = 7.0V (Non-I/O Pins)
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)			100	µA	Max	V_{IN} = 5.5V (A_n, B_n)
I_{IL}	Input LOW Current			–1 –1	µA	Max	V_{IN} = 0.5V (Non-I/O Pins) (Note 3) V_{IN} = 0.0V (Non-I/O Pins)
$I_{IH} + I_{OZH}$	Output Leakage Current			10	µA	0V–5.5V	V_{OUT} = 2.7V (A_n, B_n); $\overline{OEAB}$ or $\overline{CEAB}$ = 2V
$I_{IL} + I_{OZL}$	Output Leakage Current			–10	µA	0V–5.5V	V_{OUT} = 0.5V (A_n, B_n); $\overline{OEAB}$ or $\overline{CEAB}$ = 2V
I_{OS}	Output Short-Circuit Current	–100		–275	mA	Max	V_{OUT} = 0V (A_n, B_n)
I_{CEX}	Output HIGH Leakage Current			50	µA	Max	V_{OUT} = V_{CC} (A_n, B_n)
I_{ZZ}	Bus Drainage Test			100	µA	0.0V	V_{OUT} = 5.5V (A_n, B_n); All Others GND
I_{CCH}	Power Supply Current			1.0	mA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current			60	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current			1.0	mA	Max	Outputs 3-STATE All Others at V_{CC} or GND
I_{CCT}	Additional I_{CC}/Input			2.5	mA	Max	V_I = V_{CC} – 2.1V All Others at V_{CC} or GND
I_{CCD}	Dynamic I_{CC} No Load (Note 3)			0.25	mA/MHz	Max	Outputs Open, $\overline{CEAB}$, $\overline{OEAB}$, $\overline{LEAB}$ = GND, $\overline{CEBA}$ = V_{CC}, One Bit Toggling, 50% Duty Cycle

Note 3: Guaranteed but not tested.

AC Electrical Characteristics

Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			$T_A = -55°C$ to $+85°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay A_n to B_n or B_n to A_n	1.5	3.0	5.7	1.5	5.7	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEAB_n}$ to B_n, $\overline{LEBA_n}$ to A_n	1.5	3.0	5.5	1.5	5.5	ns
t_{PZH} t_{PZL}	Enable Time $\overline{OEBA_n}$ or $\overline{OEAB_n}$ to A_n or B_n	1.5	2.8	5.2	1.5	5.2	ns
t_{PHZ} t_{PLZ}	Disable Time $\overline{OEAB_n}$ or $\overline{OEBA_n}$ to A_n or B_n	1.6	3.1	6.0	1.6	6.0	ns
t_{PZH} t_{PZL}	Enable Time $\overline{CEBA_n}$ or $\overline{CEAB_n}$ to A_n or B_n	1.5	3.1	6.2	1.5	6.2	ns
t_{PHZ} t_{PLZ}	Disable Time $\overline{CEBA_n}$ or $\overline{CEAB_n}$ to A_n or B_n	1.7	3.2	6.3	1.7	6.3	ns

AC Operating Requirements

(SSOP Package)

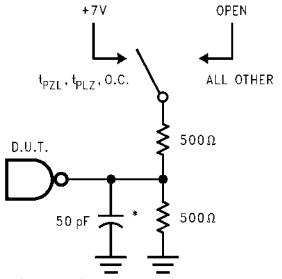
Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF		$T_A = -55°C$ to $+85°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 50$ pF		Units
		Min	Max	Min	Max	
$t_S(H)$ $t_S(L)$	Setup Time, HIGH or LOW A_n or B_n to $\overline{LEBA_n}$ or $\overline{LEAB_n}$	2.0 2.0		2.0 2.0		ns
$t_H(H)$ $t_H(L)$	Hold Time, HIGH or LOW A_n or B_n to $\overline{LEBA_n}$ or $\overline{LEAB_n}$	1.0 1.0		1.0 1.0		ns
$t_W(L)$	Pulse Width, LOW	3.0		3.0		ns

Capacitance

Symbol	Parameter	Typ	Units	Conditions $T_A = 25°C$
C_{IN}	Input Capacitance	5.0	pF	$V_{CC} = 0V$ (non I/O pins)
$C_{I/O}$ (Note 4)	Output Capacitance	11.0	pF	$V_{CC} = 5.0V$ (A_n, B_n)

Note 4: $C_{I/O}$ is measured at frequency, f = 1 MHz, per MIL-STD-883, Method 3012.

AC Loading



*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

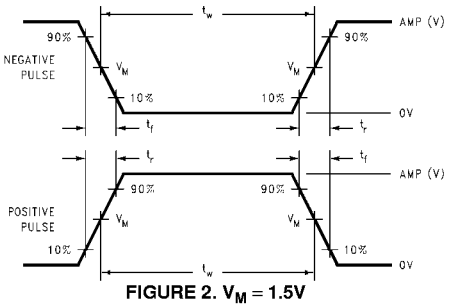


FIGURE 2. V_M = 1.5V

Input Pulse Requirements

Amplitude	Rep. Rate	t_W	t_r	t_f
3V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Test Input Signal Requirements

AC Waveforms

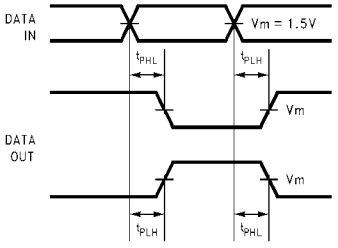


FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

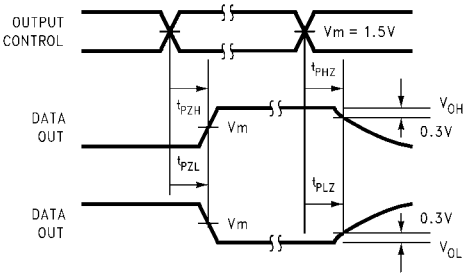


FIGURE 6. 3-STATE Output HIGH and LOW Enable and Disable Times

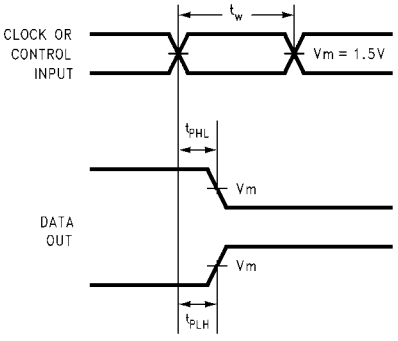


FIGURE 5. Propagation Delay, Pulse Width Waveforms

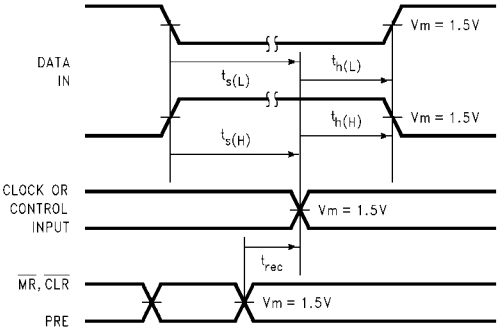
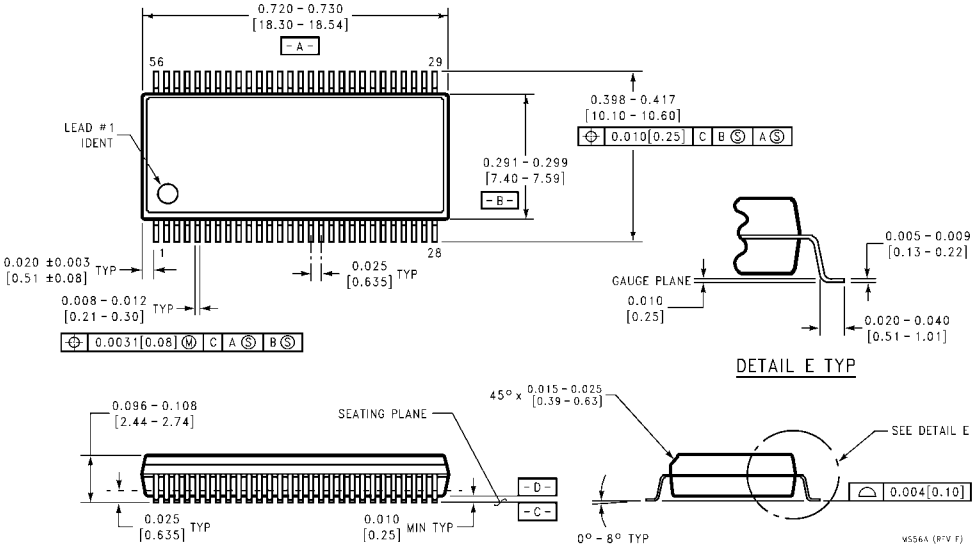


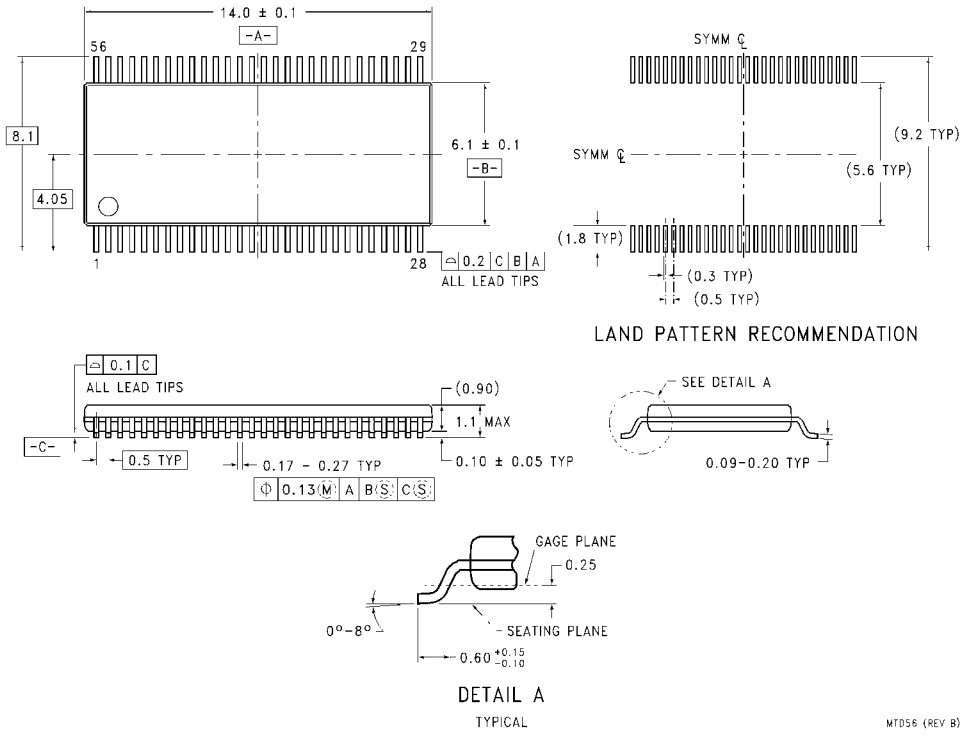
FIGURE 7. Setup Time, Hold Time and Recovery Time Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted



56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
Package Number MS56A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56

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