Comparator, High Speed, 50 ns, Low Voltage, Rail-to-Rail

NCS2250, NCV2250, NCS2252, NCV2252

The NCS2250 and NCS2252 low voltage comparators feature fast response time and rail−to−rail input and output. The extended common mode input voltage range allows input signals 200 mV above and below the rails, allowing voltage detection at ground or the supply. A propagation delay of 50 ns with a 100 mV overdrive makes this comparator suitable for applications requiring faster response times.

These single channel devices are available with a complementary push−pull output in the NCS2250 or with an open drain output in the NCS2252. Both options are offered in TSOP−5 (SOT23−5) and SC−88A (SC70−5) packages. Automotive qualified devices are also available, denoted by the NCV prefix.

Features

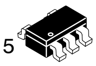
- Propagation Delay: 50 ns with 100 mV Overdrive
- Rail−to−rail Input: V_{SS} − 200 mV to V_{DD} + 200 mV
- Supply Voltage: 1.8 V to 5.5 V
- Supply Current: 150 μA Typical at 5 V Supply
- Available with Push−pull or Open Drain Output
- Packages: TSOP−5 (SOT23−5) and SC−88A (SC70−5)
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Voltage Threshold Detector
- Zero−crossing Detectors
- High−speed Sampling Circuits
- Logic Level Shifting / Translation
- Clock and Data Signal Restoration

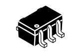
End Products

- Automotive
- Lighting
- Smartphones, cell phones
- Portable and battery−powered systems
- Power supplies

5

1

SCALE 2:1

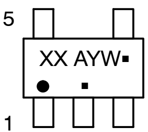
TSOP−5
(SOT23−5)
CASE 483



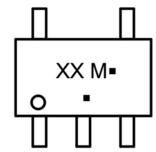
SCALE 2:1

SC−88A
(SC70−5)
CASE 419A−02

MARKING DIAGRAMS

5


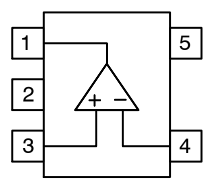
1



XX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN DIAGRAM

OUT
VSS
IN+


VDD
IN−

TSOP−5 (SOT23−5) and
SC−88A (SC70−5) pinout

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

Table 1. ORDERING INFORMATION

Automotive	Output	Device (Note 1)	Package	Marking	Shipping †
No	Push−Pull	NCS2250SQ2T2G	SC−88A (SC70−5)	5C	3000 / Tape & Reel
		NCS2250SN2T1G	TSOP−5 (SOT23−5)	5A	3000 / Tape & Reel
	Open Drain	NCS2252SQ2T2G	SC−88A (SC70−5)	5F	3000 / Tape & Reel
		NCS2252SN2T1G	TSOP−5 (SOT23−5)	5D	3000 / Tape & Reel
Yes	Push−Pull	NCV2250SQ2T2G	SC−88A (SC70−5)	5C	3000 / Tape & Reel
		NCV2250SN2T1G	TSOP−5 (SOT23−5)	5A	3000 / Tape & Reel
	Open Drain	NCV2252SQ2T2G	SC−88A (SC70−5)	5F	3000 / Tape & Reel
		NCV2252SN2T1G	TSOP−5 (SOT23−5)	5D	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.
1. Contact local sales office for more information.

Table 2. PIN DESCRIPTION

Name	Type	Description
V_{DD}	Power	Positive supply pin. Connect to positive rail. A bypass capacitor of at least 0.1 μF is recommended as close as possible to the V_{DD} pin
V_{SS}	Power	Negative supply pin. Connect to ground or negative rail. If not connected to ground, a bypass capacitor of at least 0.1 μF is recommended as close as possible to the V_{SS} pin
OUT	Output	Output pin. NCS2250 has a complementary push−pull output stage. NCS2252 has an open drain output stage which requires an external pull−up resistor
IN−	Input	Inverting input
IN+	Input	Non−inverting input

Table 3. ABSOLUTE MAXIMUM RATINGS (Note 2)

Rating	Symbol	Value	Units
Supply Voltage Range (V_{DD} – V_{SS})	V_S	0 to 6	V
Input Voltage Range	V_{IN}	V_{SS} – 0.3 to V_{DD} + 0.3	V
Output Voltage Range	V_O	V_{SS} – 0.3 to V_{DD} + 0.3	V
Output Short Circuit Current (Note 3)	I_{SC}	Continuous	mA
Maximum Junction Temperature (Note 4)	$T_{J(max)}$	+150	°C
Storage Temperature Range	Tstg	−65 to +150	°C
ESD Capability (Note 5) Human Body Model Machine Model	 HBM MM	 2000 50	V
Latch−up Current (Note 6)	I_{LU}	100	mA
Moisture Sensitivity Level (Note 7)	MSL	Level 1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
2. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
3. Applies to both single−supply and split−supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±50 mA over long term may adversely affect reliability.
4. See APPLICATION INFORMATION for Safe Operating Area.
5. This device series incorporates ESD protection and is tested by the following methods:
   – ESD Human Body Model tested per JEDEC standard JESD22−A114 (AEC−Q100−002)
   – ESD Machine Model tested per JEDEC standard JESD22−A115 (AEC−Q100−003)
6. Latch−up Current per JEDEC standard JESD78.
7. Moisture Sensitivity Level tested per IPC/JEDEC standard J−ST−020A.

Table 4. THERMAL INFORMATION

Parameter	Symbol	Package	Single Layer Board (Note 8)	Units
Junction−to−Ambient Thermal Resistance	θ_{JA}	TSOP−5 (SOT23−5)	150	°C/W
		SC−88A (SC70−5)	162	

8. Values based on a single layer 1S standard PCB with 1.0 oz copper and a 50 mm^2 copper area.

Table 5. OPERATING RANGES (Note 9)

Parameter	Symbol	Min	Max	Units
Power Supply Voltage	V_S	1.8	5.5	V
Input Common Mode Voltage Range	V_{CM}	V_{SS} – 0.2	V_{DD} + 0.2	V
Ambient Temperature	T_A	−40	125	°C

9. See APPLICATION INFORMATION for Safe Operating Area.

Table 6. ELECTRICAL CHARACTERISTICS AT 5 V SUPPLY

Typical values are referenced to T_A = 25°C, V_{DD} = 5 V, V_{SS} = 0 V, V_{CM} = mid−supply, C_L = 50 pF, unless otherwise noted. NCS2252 is connected to $R_{PULL-UP}$ = 10 kΩ to V_{DD}, unless otherwise noted. Boldface numbers apply from T_A = −40°C to 125°C (Notes 10, 11)

Parameter	Test Conditions		Symbol	Min	Typ	Max	Units
SUPPLY CHARACTERISTICS							
Quiescent Supply Current	No load		I_{DD}		150	200	µA
						250	
Power Supply Rejection Ratio			PSRR		88		dB
				62.5			
INPUT CHARACTERISTICS							
Input Offset Voltage			V_{OS}		0.5	6	mV
						6	
Input Bias Current	(Note 11)		I_{IB}		20		pA
						1000	
Input Offset Current	(Note 11)		I_{OS}		20		pA
						1000	
Common Mode Rejection Ratio			CMRR		81		dB
				59			
Input Capacitance			C_{IN}		3.8		pF
OUTPUT CHARACTERISTICS							
Output Voltage High	NCS2250, I_{OUT} = 4 mA		V_{OH}		V_{DD} − 0.1		V
				V_{DD} − 0.3			
Output Voltage Low	I_{OUT} = 4 mA		V_{OL}		V_{SS} + 0.09		V
						V_{SS} + 0.3	
Output Current Capability	NCS2250, Sourcing		I_O		48		mA
	Sinking				52		
Output Leakage Current	NCS2252, V_S = 5.5 V		I_{LEAK}		1		nA
Output Rise Time	NCS2250, 10% to 90%, V_{OD} = 100 mV		t_{rise}		4		ns
Output Fall Time	NCS2250, 90% to 10%, V_{OD} = 100 mV		t_{fall}		4		ns
	NCS2252, 90% to 10%, V_{OD} = 100 mV				5.5		
Propagation Delay (Note 11)	NCS2250	V_{OD} = 100 mV	t_{pLH}, t_{pHL}		50	64	ns
		V_{OD} = 50 mV			60		
		V_{OD} = 20 mV			90		
	NCS2252 (Note 12)	V_{OD} = 100 mV	t_{pHL}		50	64	ns
		V_{OD} = 50 mV			60		
		V_{OD} = 20 mV			90		
Propagation Delay Skew (NCS2250)	V_{OD} = 100 mV, C_L = 50 pF		t_{SKEW}		6		ns
	V_{OD} = 50 mV, C_L = 50 pF				2		
	V_{OD} = 20 mV, C_L = 50 pF				1		

10. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.
11. Performance guaranteed over the indicated operating temperature range by design and/or characterization.
12. Typical values are provided for NCS2252 output high−to−low propagation delay. NCS2252 is an open drain comparator. Output low−to−high propagation delay is a function of the RC time constant, which is dependent on the pull−up resistor.

Table 7. ELECTRICAL CHARACTERISTICS AT 1.8 V SUPPLY

Typical values are referenced to T_A = 25°C, V_{DD} = 1.8 V, V_{SS} = 0 V, V_{CM} = mid−supply, C_L = 50 pF, unless otherwise noted. NCS2252 is connected to $R_{PULL-UP}$ = 10 kΩ to V_{DD}, unless otherwise noted. Boldface numbers apply from T_A = −40°C to 125°C (Notes 13, 14)

Parameter	Test Conditions		Symbol	Min	Typ	Max	Units
SUPPLY CHARACTERISTICS							
Quiescent Supply Current	No load		I_{DD}		145	200	µA
						250	
Power Supply Rejection Ratio			PSRR		82		dB
				62.5			
INPUT CHARACTERISTICS							
Input Offset Voltage			V_{OS}		0.5	6	mV
						6	
Input Bias Current	(Note 14)		I_{IB}		20		pA
						1000	
Input Offset Current	(Note 14)		I_{OS}		20		pA
						1000	
Common Mode Rejection Ratio			CMRR		76		dB
				55			
Input Capacitance			C_{IN}		4.4		pF
OUTPUT CHARACTERISTICS							
Output Voltage High	NCS2250, I_{OUT} = 4 mA		V_{OH}		V_{DD} − 0.14		V
				V_{DD} − 0.3			
Output Voltage Low	I_{OUT} = 4 mA		V_{OL}		V_{SS} + 0.12		V
						V_{SS} + 0.3	
Output Current Capability	NCS2250, Sourcing		I_O		25		mA
	Sinking				42		
Output Leakage Current	NCS2252, V_S = 5.5 V		I_{LEAK}		1		nA
Output Rise Time	NCS2250, 10% to 90%, V_{OD} = 100 mV		t_{rise}		7		ns
Output Fall Time	NCS2250, 90% to 10%, V_{OD} = 100 mV		t_{fall}		6		ns
	NCS2252, 90% to 10%, V_{OD} = 100 mV				7		
Propagation Delay (Note 14)	NCS2250	V_{OD} = 100 mV	t_{pLH}, t_{pHL}		56	68	ns
		V_{OD} = 50 mV			71		
		V_{OD} = 20 mV			106		
	NCS2252 (Note 15)	V_{OD} = 100 mV	t_{pHL}		56	68	ns
		V_{OD} = 50 mV			71		
		V_{OD} = 20 mV			106		
Propagation Delay Skew (NCS2250)	V_{OD} = 100 mV, C_L = 50 pF		t_{SKEW}		5		ns
	V_{OD} = 50 mV, C_L = 50 pF				2		
	V_{OD} = 20 mV, C_L = 50 pF				1		

13. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.
14. Performance guaranteed over the indicated operating temperature range by design and/or characterization.
15. Typical values are provided for NCS2252 output high−to−low propagation delay. NCS2252 is an open drain comparator. Output low−to−high propagation delay is a function of the RC time constant, which is dependent on the pull−up resistor.

GRAPHS

Typical performance at T_A = 25°C, unless otherwise noted.

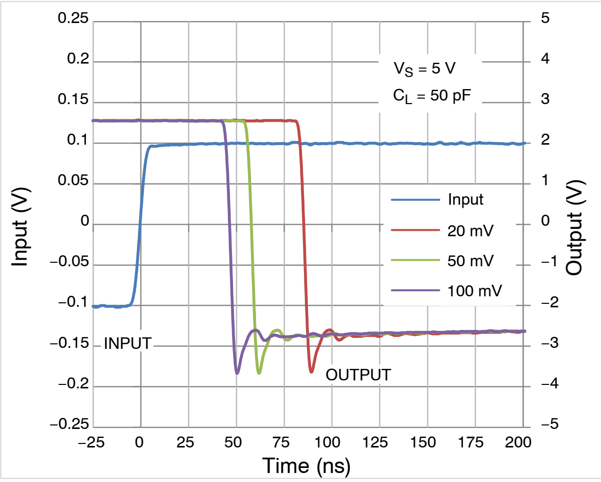


Figure 1. Transient Response at 5 V Supply with Varying Input Overdrive Voltages

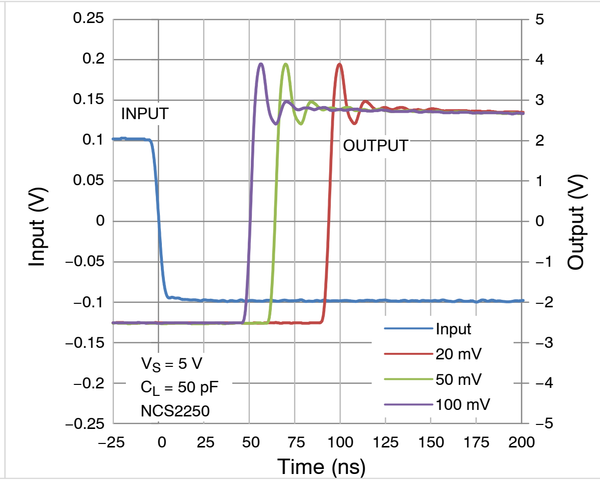


Figure 2. Transient Response at 5 V Supply with Varying Input Overdrive Voltages

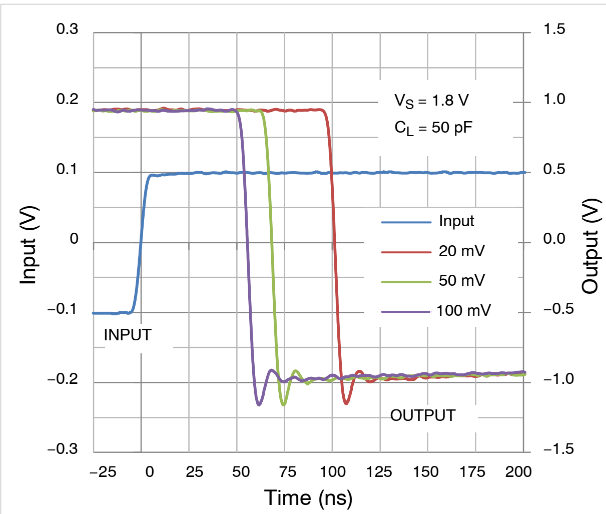


Figure 3. Transient Response at 1.8 V Supply with Varying Input Overdrive Voltages

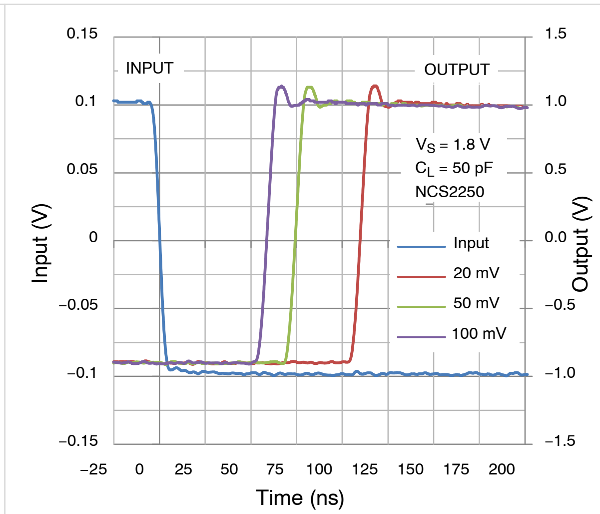


Figure 4. Transient Response at 1.8 V Supply with Varying Input Overdrive Voltages

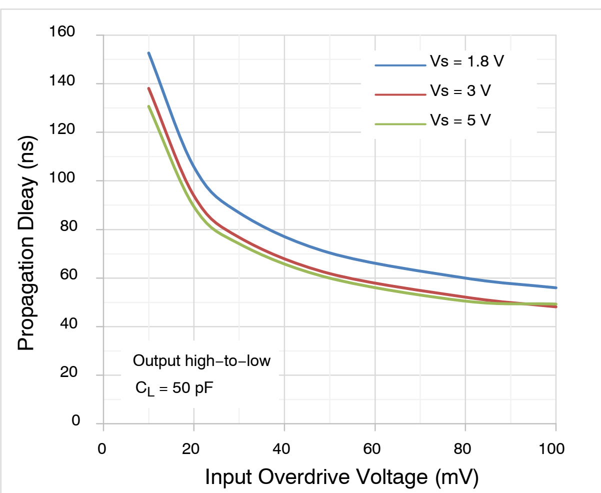


Figure 5. Output High−to−Low Propagation Delay vs. Input Overdrive Voltage

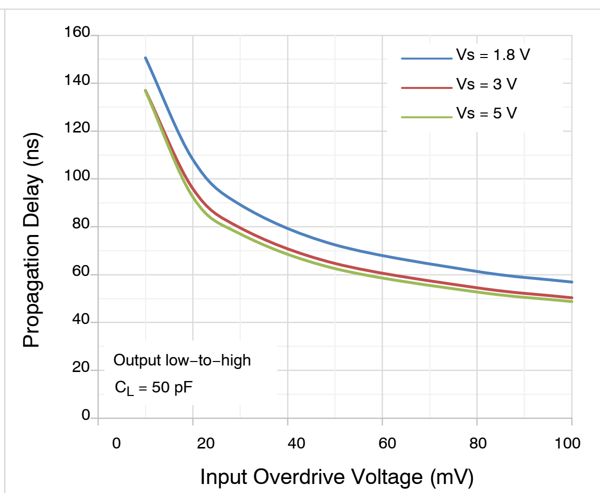


Figure 6. Output Low−to−High Propagation Delay vs. Input Overdrive Voltage

GRAPHS (continued)

Typical performance at T_A = 25°C, unless otherwise noted.

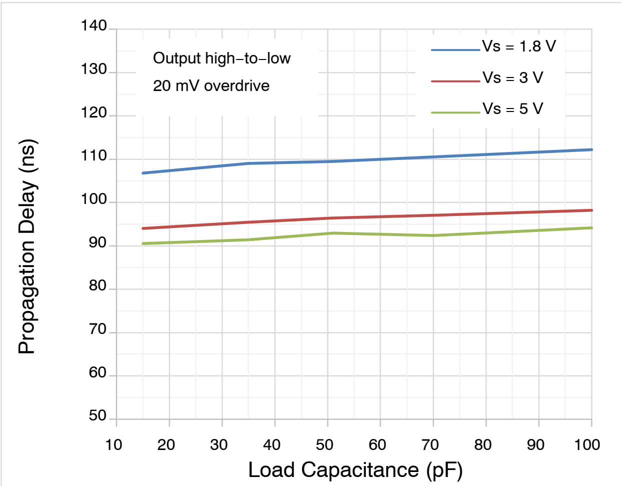


Figure 7. Output High−to−Low Propagation Delay vs. Load Capacitance

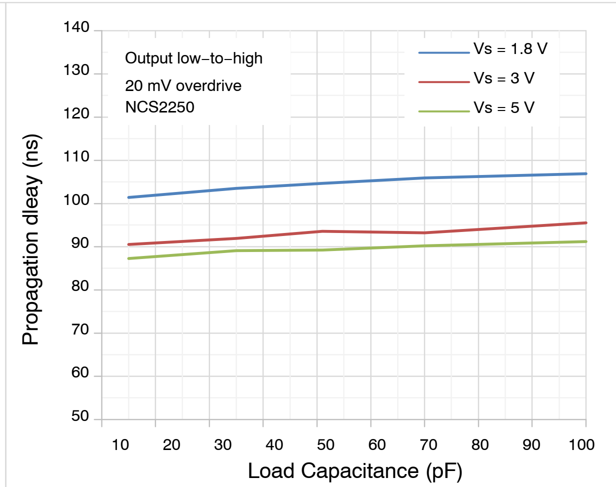


Figure 8. Output Low−to−High Propagation Delay vs. Load Capacitance

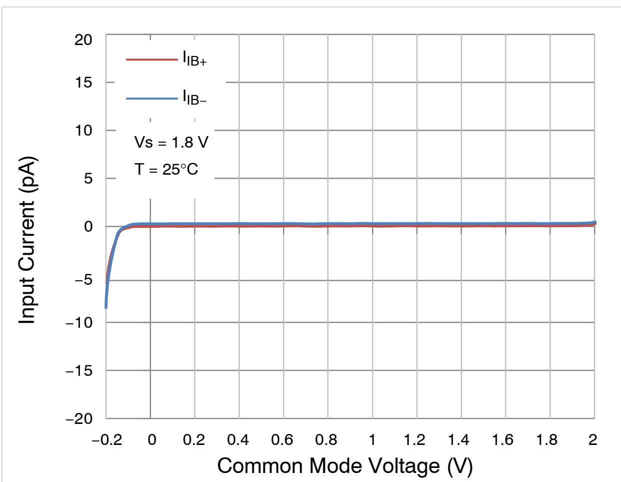


Figure 9. Input Current vs. Common Mode Voltage at 1.8 V Supply

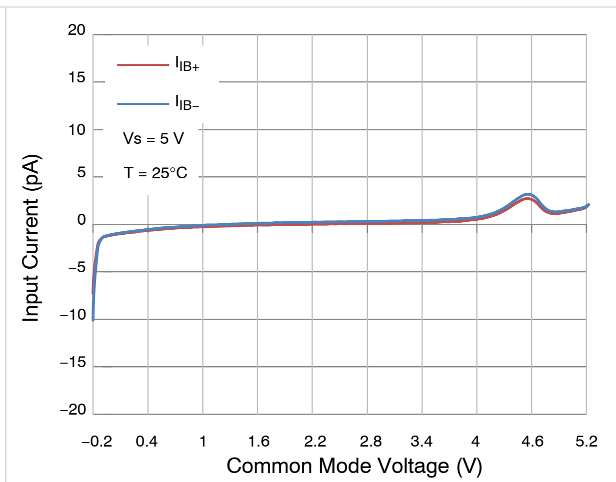


Figure 10. Input Current vs. Common Mode Voltage at 5 V Supply

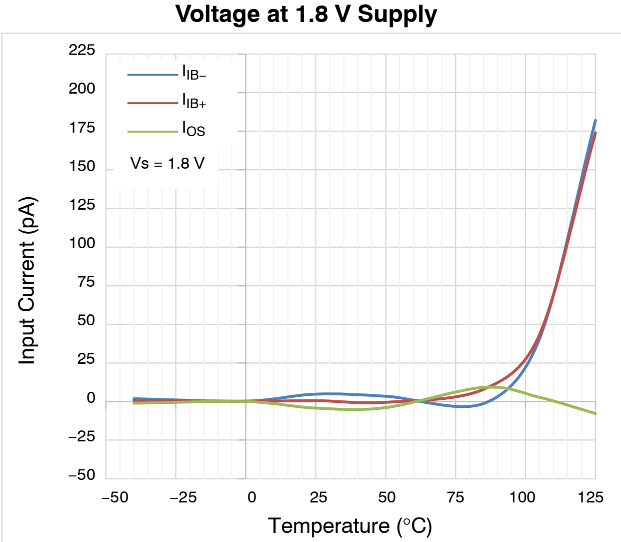


Figure 11. Input Current vs. Temperature at 1.8 V Supply

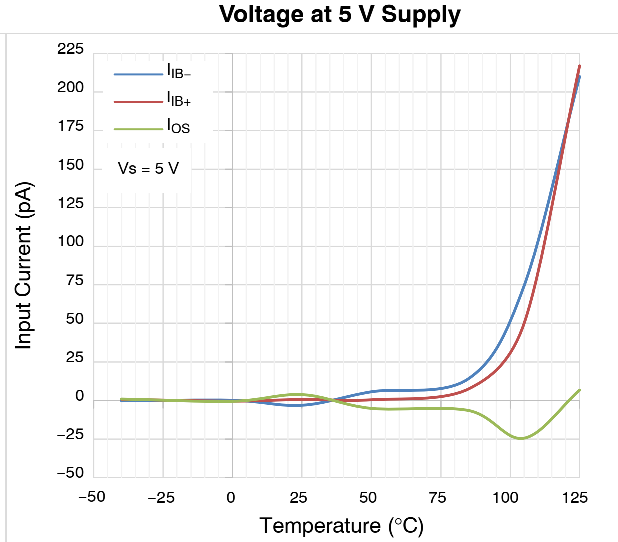


Figure 12. Input Current vs. Temperature at 5 V Supply

GRAPHS (continued)

Typical performance at T_A = 25°C, unless otherwise noted.

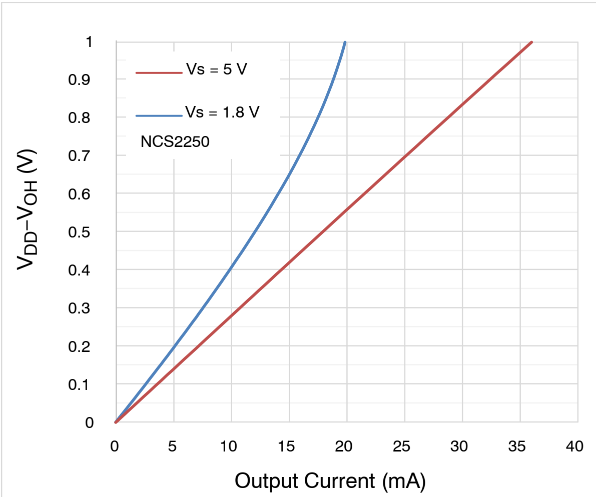


Figure 13. Output Voltage High (Relative to V_{DD}) vs. Output Current

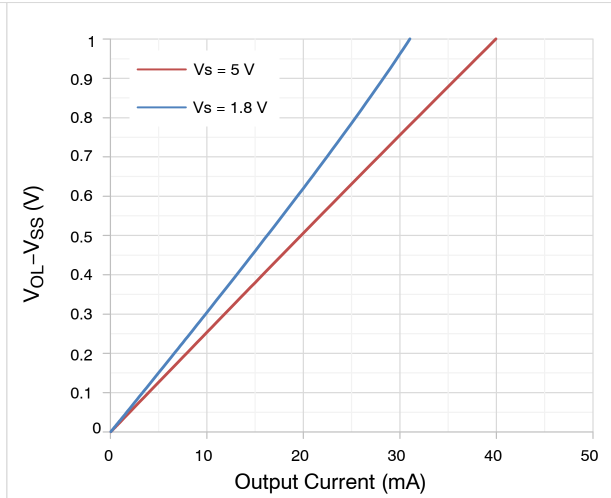


Figure 14. Output Voltage Low (Relative to V_{SS}) vs. Output Current

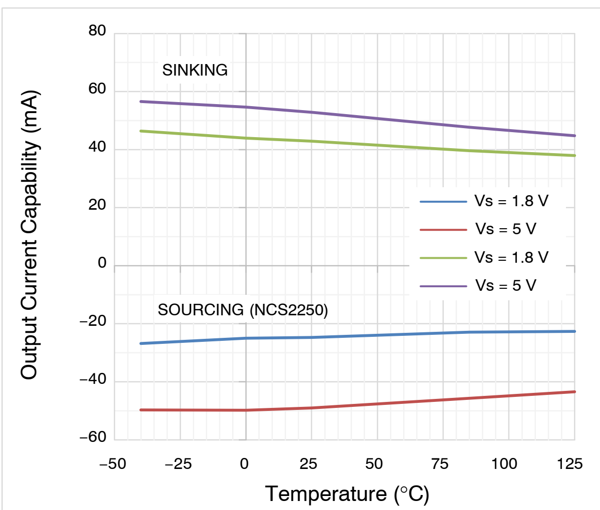


Figure 15. Output Current Capability vs. Temperature

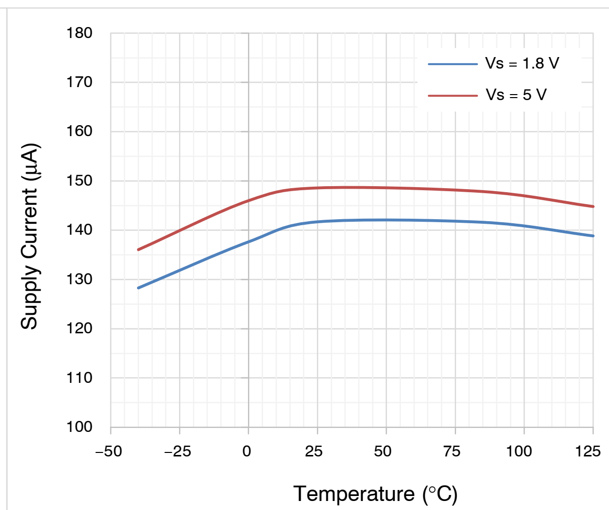


Figure 16. Supply Current vs. Temperature

APPLICATION INFORMATION

Input Stage

The NCS2250 and NCS2252 have rail−to−rail inputs. The input common mode voltage range of these comparators extend 200 mV beyond the rails, allowing voltage sensing at ground or at the supply voltage.

Output Stage

The NCS2250 has a complementary, push−pull output stage. When the output transitions between high and low states, a low resistance path is created between the positive and negative supply rails, temporarily increasing the supply current during the transition.

The NCS2252 has an open−drain output stage. This allows the output to be connected through a pull−up resistor to another supply voltage for applications where level translation or level shifting is needed. The output resistor can be connected to voltages below V_{DD} or up to V_{DD} + 0.3 V. Since the NCS2252 relies on an external pull−up resistor to provide sourcing current, the timing of the output low−to−high transition is determined by the RC time constant of the pull−up resistor and the load capacitance.

Hysteresis

When the inputs are near the same voltage, slight voltage fluctuations due to noise can cause the output to oscillate between high and low states. If noise−induced switching behavior is observed at the output, hysteresis should be added through an external resistor network. This is particularly the case for NCS2250, as sustained output oscillations causing increased supply current will result in elevated junction temperature.

Hysteresis can be added to the circuit by adding one or two external resistors depending on whether an inverting or non−inverting configuration is needed. Figure 17 shows the inverting configuration. In this configuration, the output voltage adjusts the threshold at the IN+ pin.

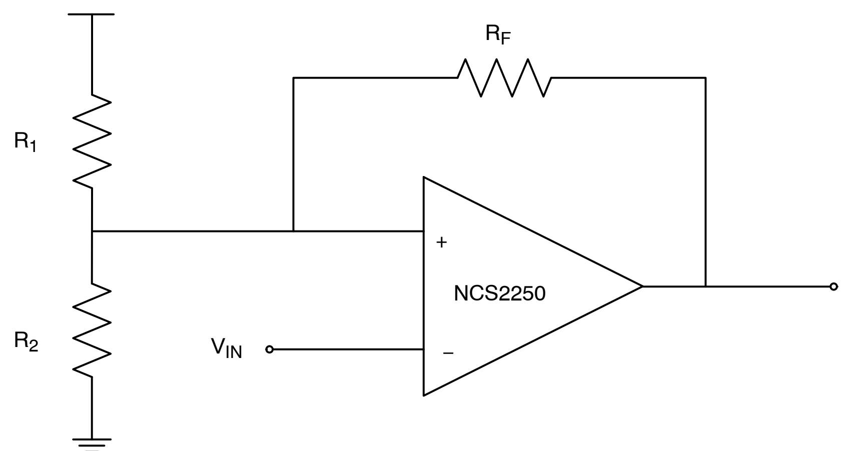


Figure 17. Comparator with Hysteresis, Inverting Configuration

For the inverting configuration, the value of the high−level input voltage which triggers the output to switch from high to low is given by the following equation:

$$V_{IN\_high} = \frac{R_2 \times R_F + R_1 \times R_2}{R_1 \times R_F + R_1 \times R_2 + R_2 \times R_F} \times V_{DD} \qquad \text{(eq. 1)}$$

The value of the low−level input voltage which triggers the output to switch from low to high is given by the following equation:

$$V_{IN\_low} = \frac{R_2 \times R_F}{R_1 \times R_F + R_1 \times R_2 + R_2 \times R_F} \times V_{DD} \qquad \text{(eq. 2)}$$

Figure 18 shows the non−inverting configuration. For the non−inverting configuration, the threshold V_{th} set by R_1 and R_2 is fixed. The output adjusts the input signal on IN+.

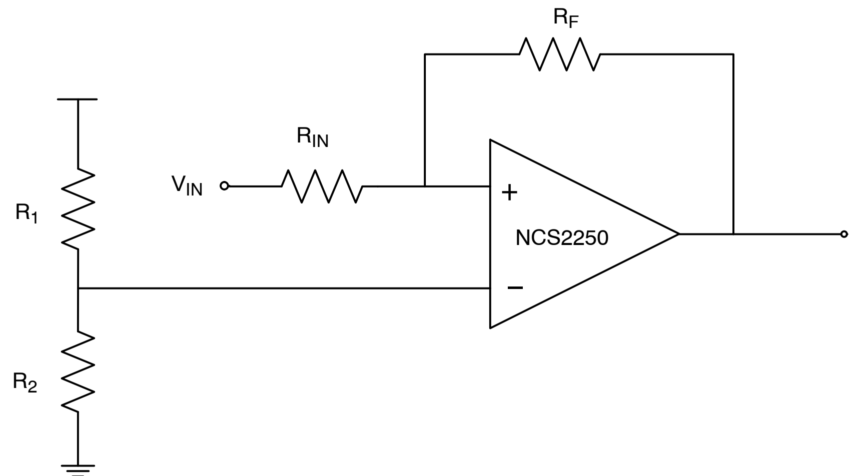


Figure 18. Comparator with Hysteresis, Non−Inverting Configuration

The value of the high−level input voltage which triggers the output to switch from low to high is given by the following equation:

$$V_{IN\_high} = \frac{V_{th} \times (R_{IN} + R_F)}{R_F} \qquad \text{(eq. 3)}$$

The value of the low−level input voltage which triggers the output to switch from high to low is given by the following equation:

$$V_{IN\_low} = \frac{V_{th} \times (R_{IN} + R_F) - R_{IN} \times V_{DD}}{R_F} \qquad \text{(eq. 4)}$$

Power dissipation

The absolute maximum junction temperature is 150°C. The junction temperature can be calculated using the power dissipation P, thermal resistance θ_{JA}, and ambient temperature T_A.

$$T_J = \theta_{JA} \times P + T_A \qquad \text{(eq. 5)}$$

Layout Techniques

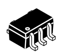
High speed layout techniques are recommended for the best performance.

Bypass capacitors of at least 0.1 μF must be placed as close as possible to supply pins.

The traces on the input pins should be short to minimize any noise on the high impedance inputs. In general, shorter traces will reduce parasitic capacitance, inductance, and resistance.

Identify and keep sensitive traces away from possible noise sources such as clocks. Crosstalk can be reduced by increasing the distance between traces. Do not let traces run parallel for long distances. Take advantage of routing layers to separate traces that would otherwise run parallel. Ground or DC voltage supplies can be used to separate a sensitive trace from a noise source.

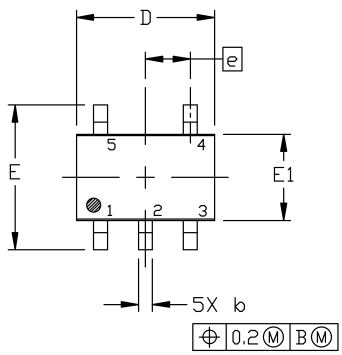
Avoid floating nodes as these will pick up noise.

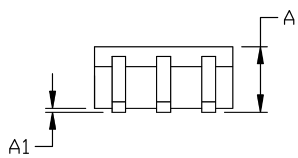


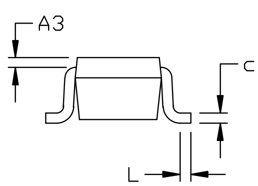
SCALE 2:1

SC−88A (SC−70−5/SOT−353)
CASE 419A−02
ISSUE M

DATE 11 APR 2023

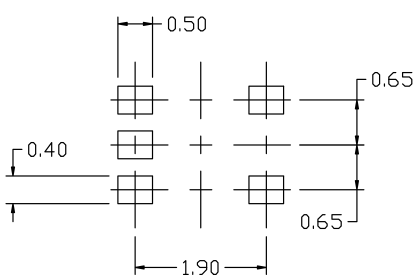






NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.1016MM PER SIDE.

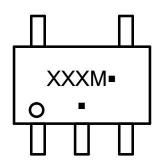
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.95	1.10
A1	---	---	0.10
A3	0.20 REF		
b	0.10	0.20	0.30
c	0.10	---	0.25
D	1.80	2.00	2.20
E	2.00	2.10	2.20
E1	1.15	1.25	1.35
e	0.65 BSC		
L	0.10	0.15	0.30



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. EMITTER
3. BASE
4. COLLECTOR
5. CATHODE

STYLE 3:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. CATHODE 1

STYLE 4:
PIN 1. SOURCE 1
2. DRAIN 1/2
3. SOURCE 1
4. GATE 1
5. GATE 2

STYLE 5:
PIN 1. CATHODE
2. COMMON ANODE
3. CATHODE 2
4. CATHODE 3
5. CATHODE 4

STYLE 6:
PIN 1. EMITTER 2
2. BASE 2
3. EMITTER 1
4. COLLECTOR
5. COLLECTOR 2/BASE 1

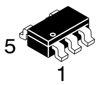
STYLE 7:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 8:
PIN 1. CATHODE
2. COLLECTOR
3. N/C
4. BASE
5. EMITTER

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. ANODE
5. ANODE

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

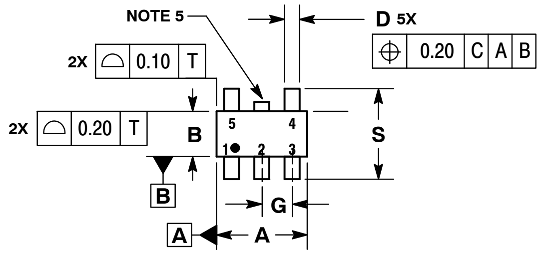
DOCUMENT NUMBER:	98ASB42984B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	SC−88A (SC−70−5/SOT−353)	PAGE 1 OF 1



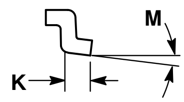
SCALE 2:1

TSOP−5
CASE 483
ISSUE N

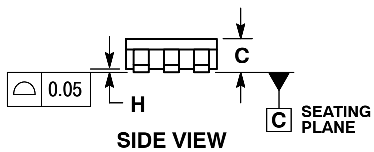
DATE 12 AUG 2020



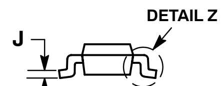
TOP VIEW



DETAIL Z



SIDE VIEW

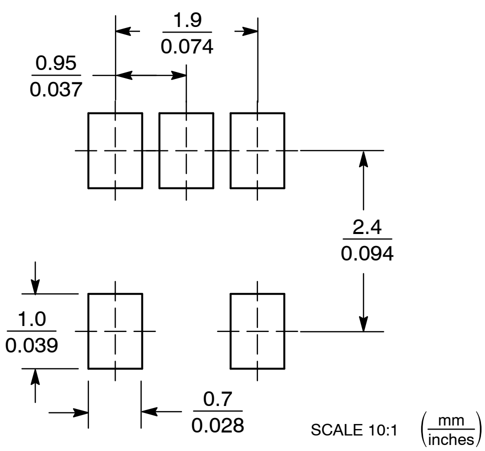


END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

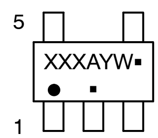
	MILLIMETERS	
DIM	**MIN**	**MAX**
A	2.85	3.15
B	1.35	1.65
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
M	0 °	10 °
S	2.50	3.00

SOLDERING FOOTPRINT*

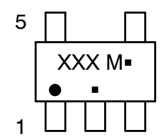


*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



Analog



Discrete/Logic

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

DOCUMENT NUMBER:	**98ARB18753C**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**TSOP−5**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales