

# DTC114E Series

Preferred Devices

## Bias Resistor Transistor

### NPN Silicon Surface Mount Transistor with Monolithic Bias Resistor Network

This new series of digital transistors is designed to replace a single device and its external resistor bias network. The BRT (Bias Resistor Transistor) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space. The device is housed in the TO-92 package which is designed for through hole applications.

#### MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Base Voltage	$V_{CBO}$	50	Vdc
Collector-Emitter Voltage	$V_{CEO}$	50	Vdc
Collector Current	$I_C$	100	mAdc
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (Note 1.) Derate above $25^\circ\text{C}$	$P_D$	350 2.81	mW mW/ $^\circ\text{C}$

#### THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Ambient (surface mounted)	$R_{\theta JA}$	357	$^\circ\text{C}/\text{W}$
Operating and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$
Maximum Temperature for Soldering Purposes, Time in Solder Bath	$T_L$	260 10	$^\circ\text{C}$ Sec

#### DEVICE MARKING AND RESISTOR VALUES

Device	Marking	R1 (K)	R2 (K)	Shipping
DTC114E	DTC114E	10	10	5000/Box
DTC124E	DTC124E	22	22	
DTC144E	DTC144E	47	47	
DTC114Y	DTC114Y	10	47	
DTC114T	DTC114T	10	$\infty$	
DTC143T	DTC143T	4.7	$\infty$	
DTD113E	DTD113E	1.0	1.0	
DTC123E	DTC123E	2.2	2.2	
DTC143E	DTC143E	4.7	4.7	
DTC143Z	DTC143Z	4.7	47	

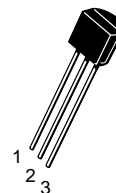
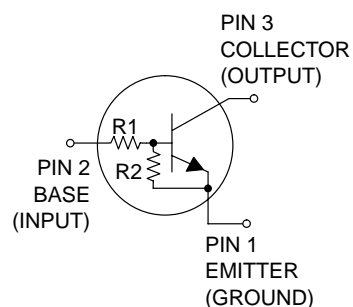
- Device mounted on a FR-4 glass epoxy printed circuit board using the minimum recommended footprint.



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### NPN SILICON BIAS RESISTOR TRANSISTOR



CASE 29  
TO-92 (TO-226)  
STYLE 1

#### MARKING DIAGRAM



DTC1 = Specific Device Code  
xxx = (See Table)  
Y = Year  
WW = Work Week

Preferred devices are recommended choices for future use and best overall value.

## DTC114E Series

### ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Collector–Base Cutoff Current ( $V_{CB} = 50\text{ V}$ , $I_E = 0$ )	$I_{CBO}$	–	–	100	nAdc
Collector–Emitter Cutoff Current ( $V_{CE} = 50\text{ V}$ , $I_B = 0$ )	$I_{CEO}$	–	–	500	nAdc
Emitter–Base Cutoff Current ( $V_{EB} = 6.0\text{ V}$ , $I_C = 0$ )	$I_{EBO}$	–	–	0.5	mAdc
DTC114E		–	–	0.2	
DTC124E		–	–	0.1	
DTC144E		–	–	0.2	
DTC114Y		–	–	0.9	
DTC114T		–	–	1.9	
DTC143T		–	–	4.3	
DTD113E		–	–	2.3	
DTC123E		–	–	1.5	
DTC143E		–	–	0.18	
DTC143Z		–	–		
Collector–Base Breakdown Voltage ( $I_C = 10\ \mu\text{A}$ , $I_E = 0$ )	$V_{(BR)CBO}$	50	–	–	Vdc
Collector–Emitter Breakdown Voltage (Note 2.) ( $I_C = 2.0\text{ mA}$ , $I_B = 0$ )	$V_{(BR)CEO}$	50	–	–	Vdc

### ON CHARACTERISTICS (Note 2.)

DC Current Gain ( $V_{CE} = 10\text{ V}$ , $I_C = 5.0\text{ mA}$ )	DTC114E DTC124E DTC144E DTC114Y DTC114T DTC143T DTD113E DTC123E DTC143E DTC143Z	$h_{FE}$	35 60 80 80 160 160 3.0 8.0 15 80	60 100 140 140 350 350 5.0 15 30 200	– – – – – – – – – –	
Collector–Emitter Saturation Voltage ( $I_C = 10\text{ mA}$ , $I_E = 0.3\text{ mA}$ ) DTC144E/DTC114Y DTD113E/DTC143E ( $I_C = 10\text{ mA}$ , $I_B = 5\text{ mA}$ ) DTC123E ( $I_C = 10\text{ mA}$ , $I_B = 1\text{ mA}$ ) DTC114T/DTC143T/ DTC143Z/DTC124E		$V_{CE(sat)}$	–	–	0.25	Vdc
Output Voltage (on) ( $V_{CC} = 5.0\text{ V}$ , $V_B = 2.5\text{ V}$ , $R_L = 1.0\text{ k}\Omega$ )          ( $V_{CC} = 5.0\text{ V}$ , $V_B = 3.5\text{ V}$ , $R_L = 1.0\text{ k}\Omega$ )	DTC114E DTC124E DTC114Y DTC114T DTC143T DTD113E DTC123E DTC143E DTC143Z DTC144E	$V_{OL}$	– – – – – – – – – –	– – – – – – – – – –	0.2 0.2 0.2 0.2 0.2 0.2 0.2 0.2 0.2 0.2	Vdc

2. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty Cycle < 2.0%

## DTC114E Series

### ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise noted) (Continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (off) ( $V_{CC} = 5.0\text{ V}$ , $V_B = 0.5\text{ V}$ , $R_L = 1.0\text{ k}\Omega$ )  ( $V_{CC} = 5.0\text{ V}$ , $V_B = 0.05\text{ V}$ , $R_L = 1.0\text{ k}\Omega$ ) ( $V_{CC} = 5.0\text{ V}$ , $V_B = 0.25\text{ V}$ , $R_L = 1.0\text{ k}\Omega$ )  DTC114E DTC124E DTC144E DTC114Y DTC123E DTC143E DTD113E DTC114T DTC143T DTC143Z	$V_{OH}$	4.9	–	–	Vdc
Input Resistor  DTC114E DTC124E DTC144E DTC114Y DTC114T DTC143T DTD113E DTC123E DTC143E DTC143Z	R1	7.0 15.4 32.9 7.0 7.0 3.3 0.7 1.5 3.3 3.3	10 22 47 10 10 4.7 1.0 2.2 4.7 4.7	13 28.6 61.1 13 13 6.1 1.3 2.9 6.1 6.1	$\text{k}\Omega$
Resistor Ratio DTC114E/DTC124E/DTC144E DTC114Y DTC114T/DTC143T DTD113E/DTC123E/DTC143E DTC143Z	$R_1/R_2$	0.8 0.17 – 0.8 0.055	1.0 0.21 – 1.0 0.1	1.2 0.25 – 1.2 0.185	

# DTC114E Series

## TYPICAL ELECTRICAL CHARACTERISTICS DTC114E

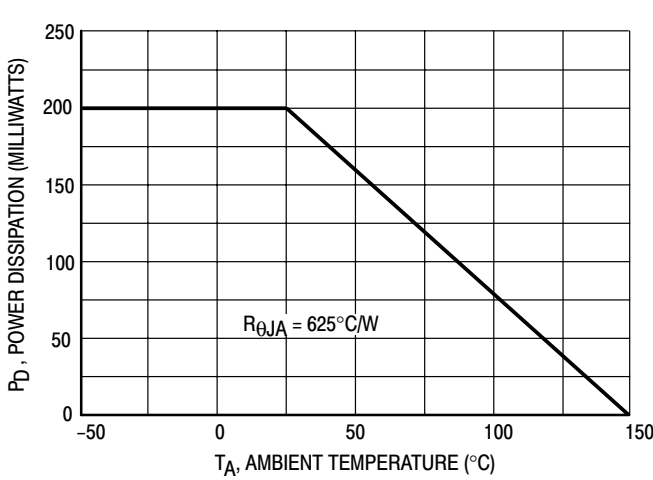


Figure 1. Derating Curve

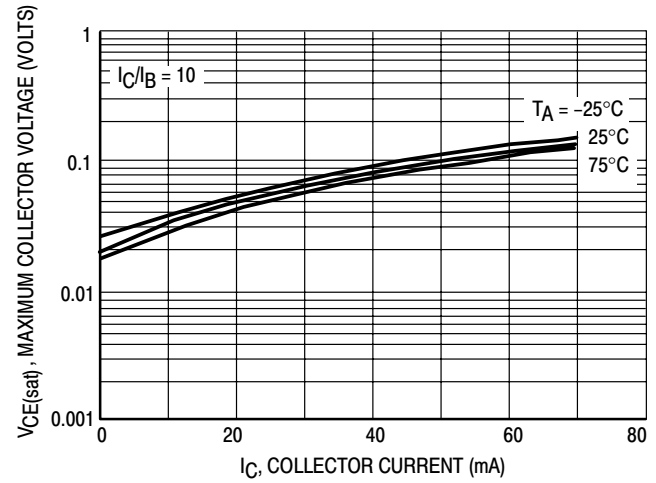


Figure 2.  $V_{CE(sat)}$  versus  $I_C$

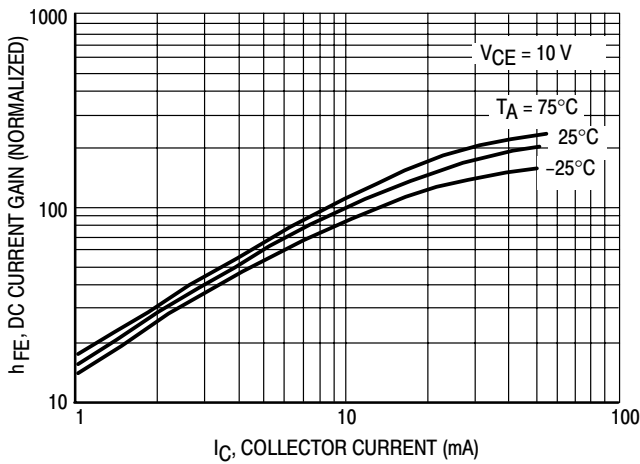


Figure 3. DC Current Gain

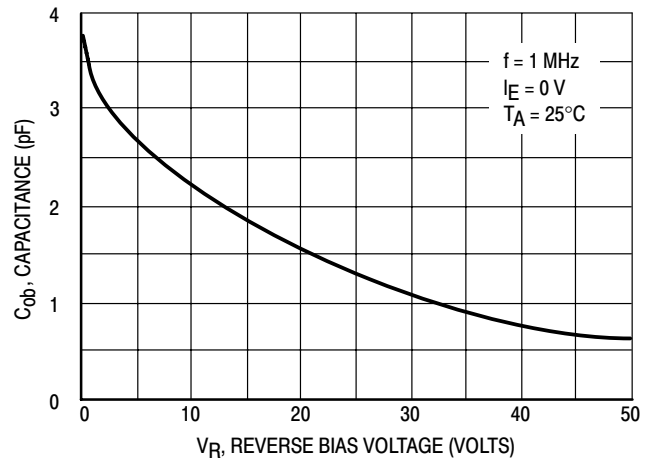


Figure 4. Output Capacitance

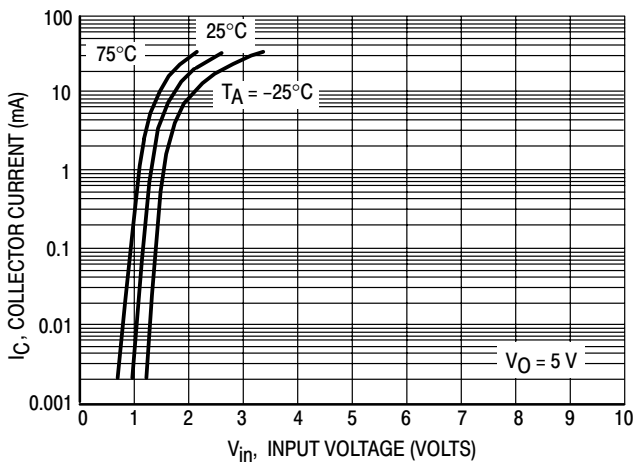


Figure 5.  $V_{CE(sat)}$  versus  $I_C$

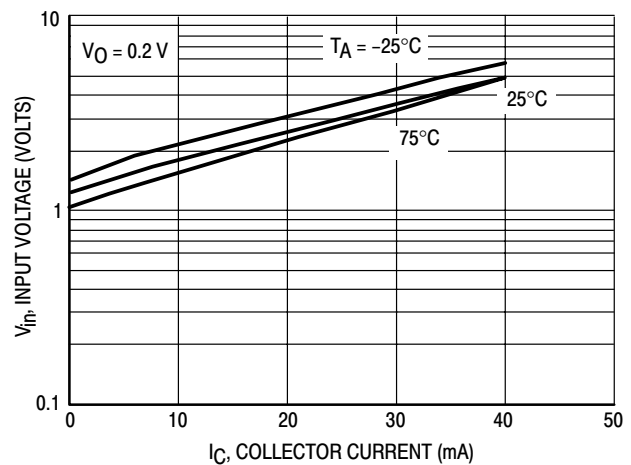


Figure 6.  $V_{CE(sat)}$  versus  $I_C$

# DTC114E Series

## TYPICAL ELECTRICAL CHARACTERISTICS DTC124E

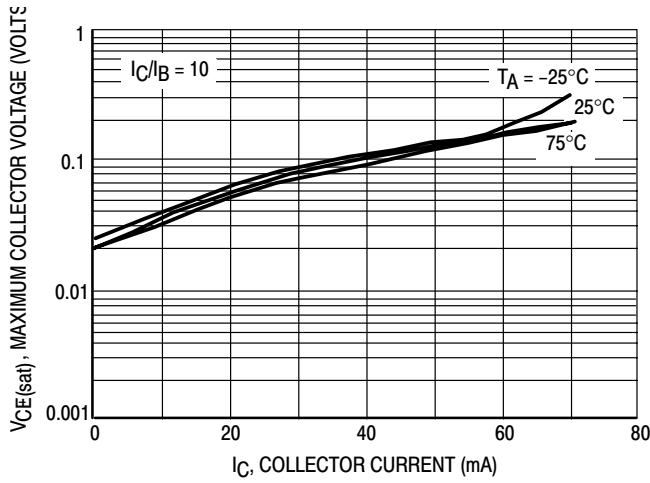


Figure 7.  $V_{CE(sat)}$  versus  $I_C$

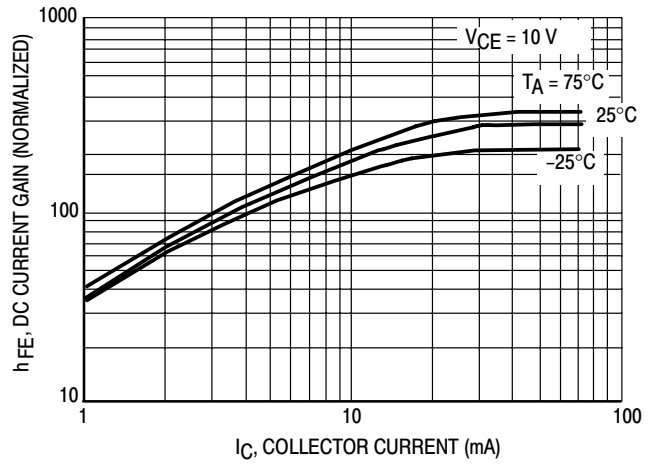


Figure 8. DC Current Gain

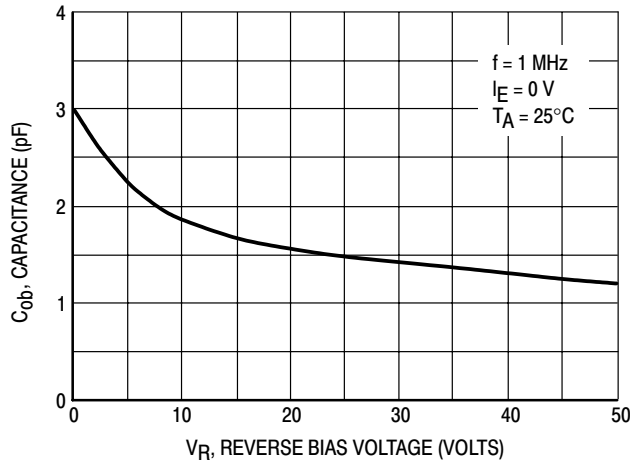


Figure 9. Output Capacitance

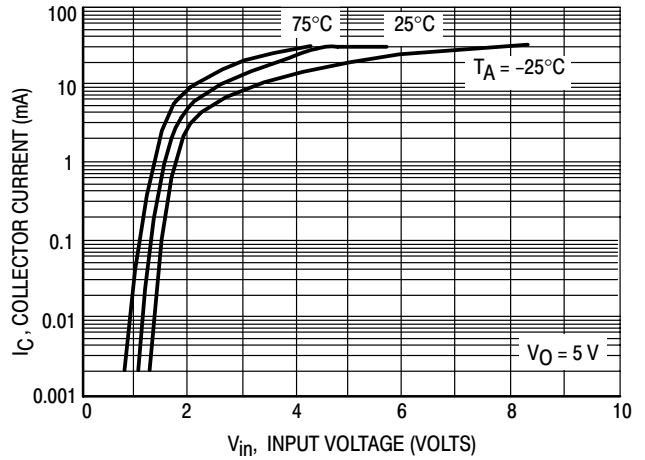


Figure 10. Output Current versus Input Voltage

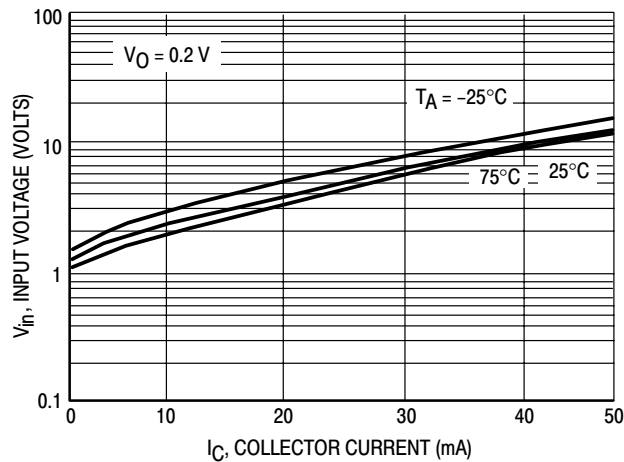


Figure 11. Input Voltage versus Output Current

# DTC114E Series

## TYPICAL ELECTRICAL CHARACTERISTICS DTC144E

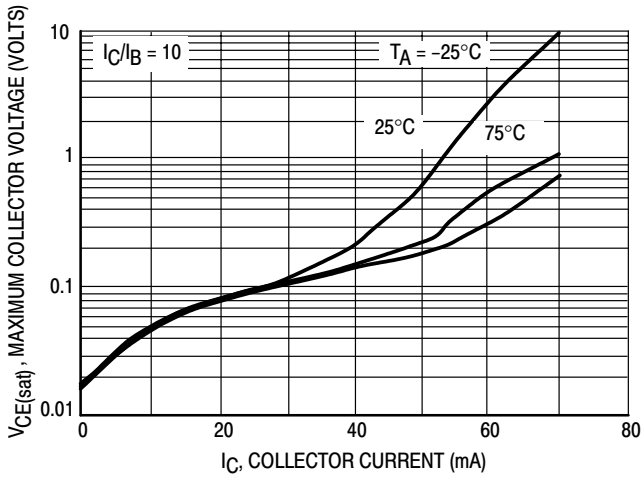


Figure 12.  $V_{CE(sat)}$  versus  $I_C$

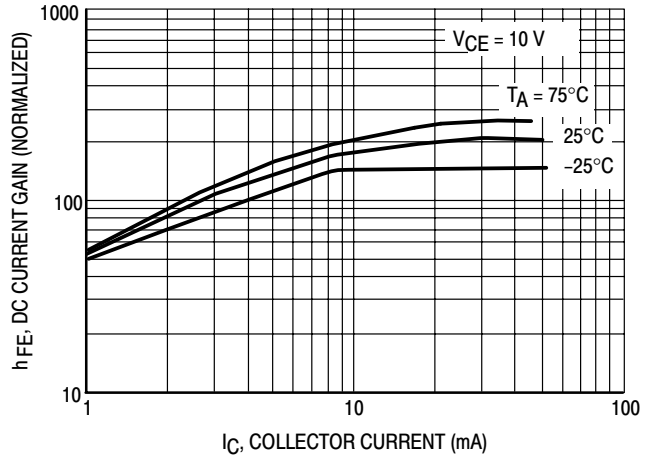


Figure 13. DC Current Gain

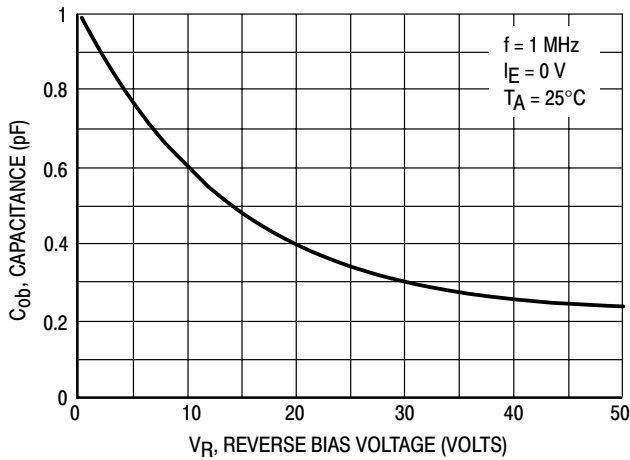


Figure 14. Output Capacitance

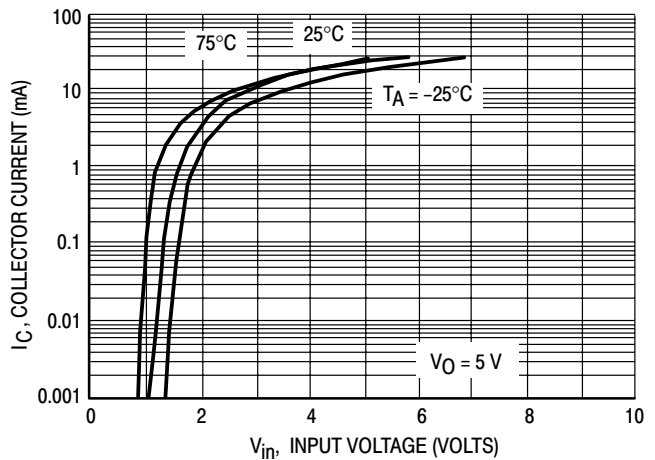


Figure 15. Output Current versus Input Voltage

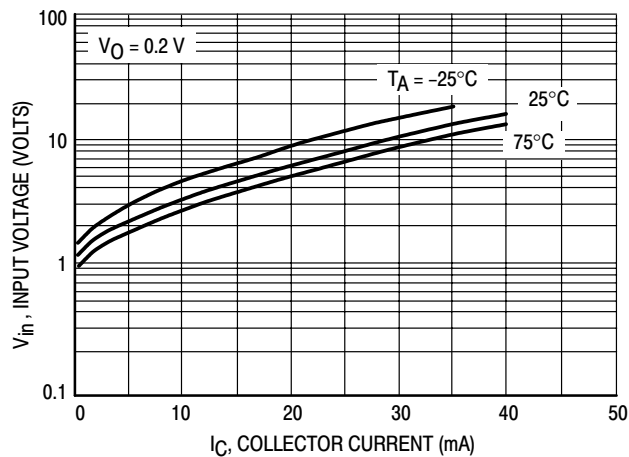


Figure 16. Input Voltage versus Output Current

# DTC114E Series

## TYPICAL ELECTRICAL CHARACTERISTICS DTC114Y

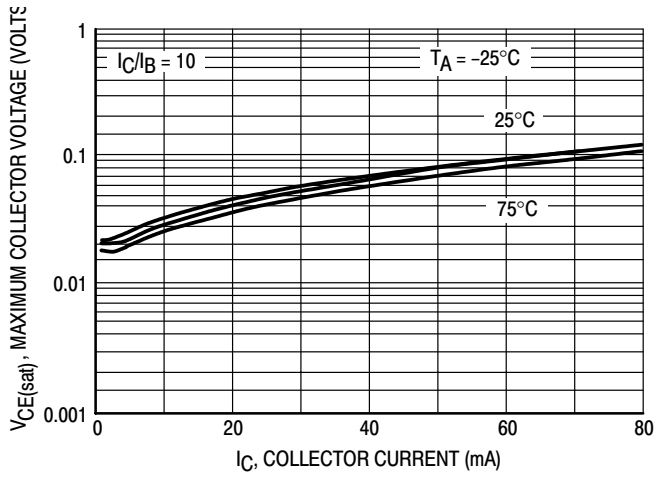


Figure 17.  $V_{CE(sat)}$  versus  $I_C$

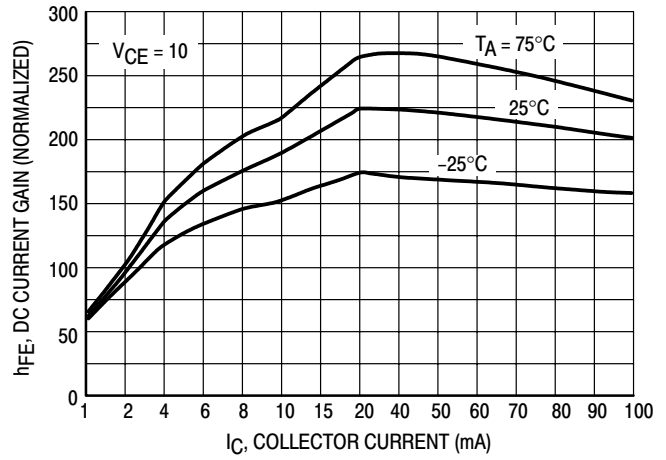


Figure 18. DC Current Gain

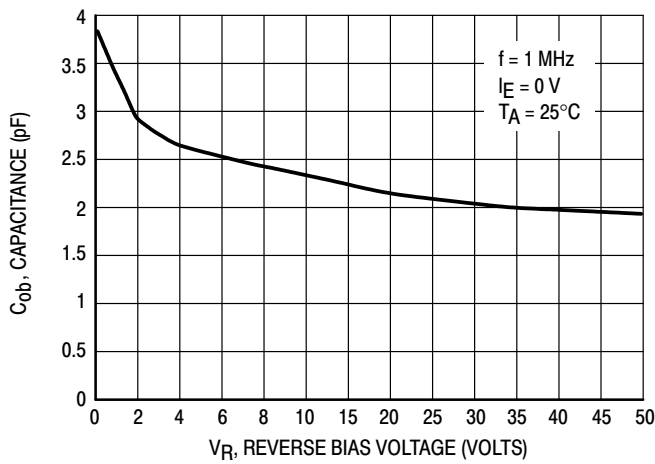


Figure 19. Output Capacitance

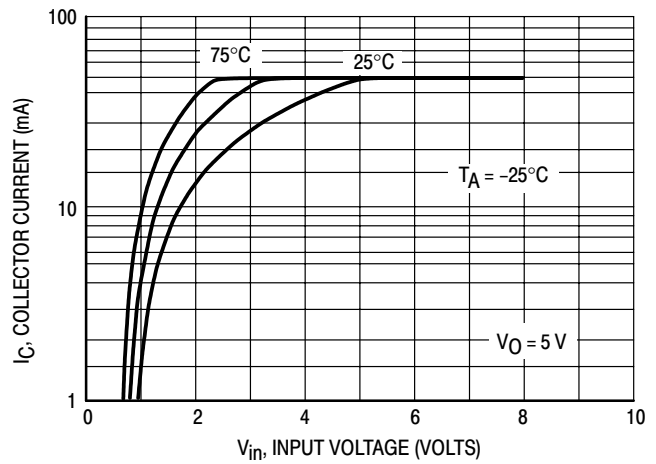


Figure 20. Output Current versus Input Voltage

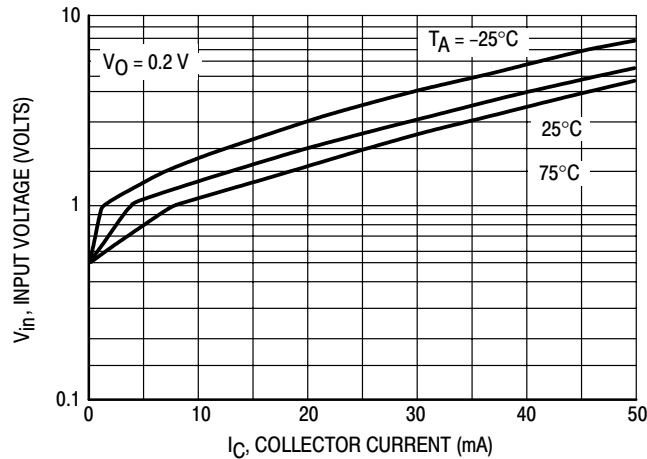


Figure 21. Input Voltage versus Output Current

# DTC114E Series

## TYPICAL APPLICATIONS FOR NPN BRTs

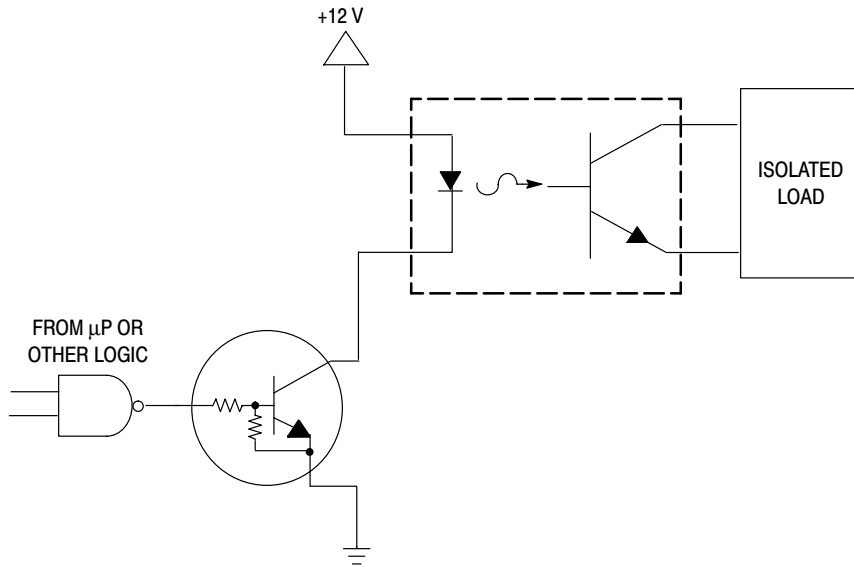


Figure 22. Level Shifter: Connects 12 or 24 Volt Circuits to Logic

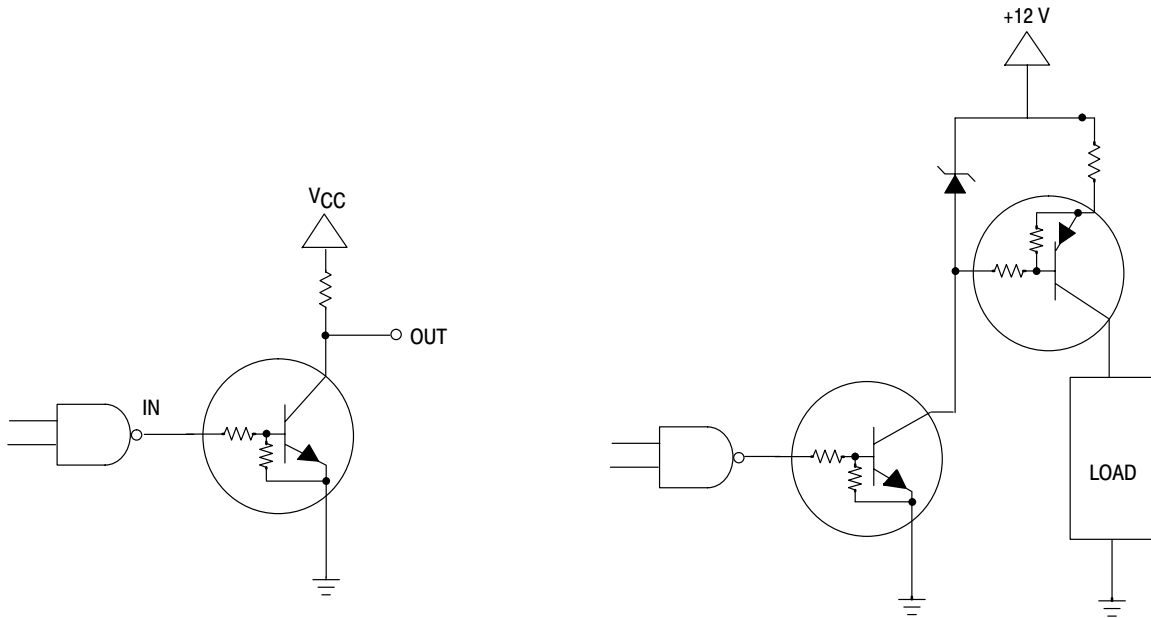


Figure 23. Open Collector Inverter: Inverts the Input Signal

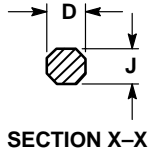
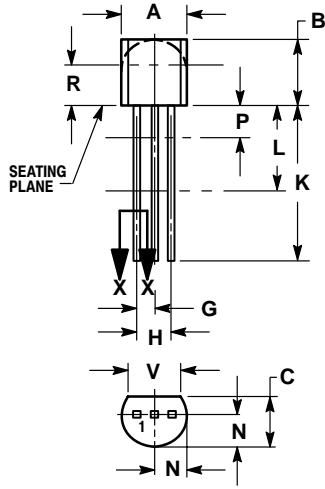
Figure 24. Inexpensive, Unregulated Current Source



# DTC114E Series

## PACKAGE DIMENSIONS

TO-92  
TO-226AA  
CASE 29-11  
ISSUE AL



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.021	0.407	0.533
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.115	---	2.93	---
V	0.135	---	3.43	---


STYLE 1:

- PIN 1. EMITTER
2. BASE
3. COLLECTOR

**Notes**

**Notes**

## DTC114E Series

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