

NSBC114EPDXV6T1, NSBC114EPDXV6T5

Preferred Devices

Dual Bias Resistor Transistors

NPN and PNP Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

The BRT (Bias Resistor Transistor) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. These digital transistors are designed to replace a single device and its external resistor bias network. The BRT eliminates these individual components by integrating them into a single device. In the NSBC114EPDXV6T1 series, two complementary BRT devices are housed in the SOT-563 package which is ideal for low power surface mount applications where board space is at a premium.

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- Available in 8 mm, 7 inch Tape and Reel
- Lead Free Solder Plating

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted, common for Q_1 and Q_2 , - minus sign for Q_1 (PNP) omitted)

| Rating | Symbol | Value | Unit |
|---------------------------|-----------|-------|------|
| Collector-Base Voltage | V_{CB0} | 50 | Vdc |
| Collector-Emitter Voltage | V_{CEO} | 50 | Vdc |
| Collector Current | I_C | 100 | mAdc |

THERMAL CHARACTERISTICS

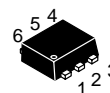
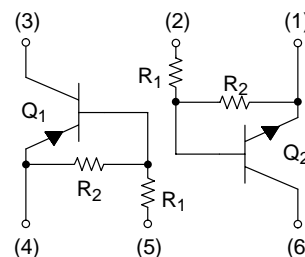
| Characteristic (One Junction Heated) | Symbol | Max | Unit |
|--|-----------------|------------------------------------|----------------------------|
| Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above 25°C | P_D | 357 (Note 1) 2.9 (Note 1) | mW mW/ $^\circ\text{C}$ |
| Thermal Resistance Junction-to-Ambient | $R_{\theta JA}$ | 350 (Note 1) | $^\circ\text{C}/\text{W}$ |
| Characteristic (Both Junctions Heated) | Symbol | Max | Unit |
| Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above 25°C | P_D | 500 (Note 1) 4.0 (Note 1) | mW mW/ $^\circ\text{C}$ |
| Thermal Resistance Junction-to-Ambient | $R_{\theta JA}$ | 250 (Note 1) | $^\circ\text{C}/\text{W}$ |
| Junction and Storage Temperature | T_J, T_{stg} | -55 to +150 | $^\circ\text{C}$ |

1. FR-4 @ Minimum Pad



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<http://onsemi.com>



SOT-563
CASE 463A
PLASTIC

MARKING DIAGRAM



xx = Specific Device Code
(see table on page 2)
D = Date Code

ORDERING INFORMATION

| Device | Package | Shipping |
|-----------------|---------|--------------------------------|
| NSBC114EPDXV6T1 | SOT-563 | 4 mm pitch 4000/Tape & Reel |
| NSBC114EPDXV6T5 | SOT-563 | 2 mm pitch 8000/Tape & Reel |

DEVICE MARKING INFORMATION

See specific marking information in the device marking table on page 2 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

NSBC114EPDXV6T1, NSBC114EPDXV6T5

DEVICE MARKING AND RESISTOR VALUES

| Device | Package | Marking | R1 (kΩ) | R2 (kΩ) |
|--------------------------|---------|---------|---------|---------|
| NSBC114EPDXV6T1 | SOT-563 | 11 | 10 | 10 |
| NSBC124EPDXV6T1 | SOT-563 | 12 | 22 | 22 |
| NSBC144EPDXV6T1 | SOT-563 | 13 | 47 | 47 |
| NSBC114YPDXV6T1 | SOT-563 | 14 | 10 | 47 |
| NSBC114TPDXV6T1 (Note 2) | SOT-563 | 15 | 10 | ∞ |
| NSBC143TPDXV6T1 (Note 2) | SOT-563 | 16 | 4.7 | ∞ |
| NSBC113EPDXV6T1 (Note 2) | SOT-563 | 30 | 1.0 | 1.0 |
| NSBC123EPDXV6T1 (Note 2) | SOT-563 | 31 | 2.2 | 2.2 |
| NSBC143EPDXV6T1 (Note 2) | SOT-563 | 32 | 4.7 | 4.7 |
| NSBC143ZPDXV6T1 (Note 2) | SOT-563 | 33 | 4.7 | 47 |
| NSBC124XPDXV6T1 (Note 2) | SOT-563 | 34 | 22 | 47 |
| NSBC123JPDXV6T1 (Note 2) | SOT-563 | 35 | 2.2 | 47 |

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted, common for Q₁ and Q₂, – minus sign for Q₁ (PNP) omitted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|----------------|--------|-----|-----|-----|------|
|----------------|--------|-----|-----|-----|------|

OFF CHARACTERISTICS

| | | | | | |
|--|----------------------|----|---|------|------|
| Collector-Base Cutoff Current (V _{CB} = 50 V, I _E = 0) | I _{CBO} | – | – | 100 | nAdc |
| Collector-Emitter Cutoff Current (V _{CE} = 50 V, I _B = 0) | I _{CEO} | – | – | 500 | nAdc |
| Emitter-Base Cutoff Current (V _{EB} = 6.0 V, I _C = 0) | I _{EBO} | – | – | 0.5 | mAdc |
| | NSBC114EPDXV6T1 | – | – | 0.2 | |
| | NSBC124EPDXV6T1 | – | – | 0.1 | |
| | NSBC144EPDXV6T1 | – | – | 0.2 | |
| | NSBC114YPDXV6T1 | – | – | 0.9 | |
| | NSBC114TPDXV6T1 | – | – | 1.9 | |
| | NSBC143TPDXV6T1 | – | – | 4.3 | |
| | NSBC113EPDXV6T1 | – | – | 2.3 | |
| | NSBC123EPDXV6T1 | – | – | 1.5 | |
| | NSBC143EPDXV6T1 | – | – | 0.18 | |
| | NSBC143ZPDXV6T1 | – | – | 0.13 | |
| | NSBC124XPDXV6T1 | – | – | 0.2 | |
| | NSBC123JPDXV6T1 | – | – | | |
| Collector-Base Breakdown Voltage (I _C = 10 μA, I _E = 0) | V _{(BR)CBO} | 50 | – | – | Vdc |
| Collector-Emitter Breakdown Voltage (Note 3) (I _C = 2.0 mA, I _B = 0) | V _{(BR)CEO} | 50 | – | – | Vdc |

ON CHARACTERISTICS (Note 3)

| | | | | | | |
|--|--|----------------------|--|---|--|-----|
| DC Current Gain (V _{CE} = 10 V, I _C = 5.0 mA) | NSBC114EPDXV6T1 NSBC124EPDXV6T1 NSBC144EPDXV6T1 NSBC114YPDXV6T1 NSBC114TPDXV6T1 NSBC143TPDXV6T1 NSBC113EPDXV6T1 NSBC123EPDXV6T1 NSBC143EPDXV6T1 NSBC143ZPDXV6T1 NSBC124XPDXV6T1 NSBC123JPDXV6T1 | h _{FE} | 35 60 80 80 160 160 3.0 8.0 15 80 80 80 | 60 100 140 140 350 350 5.0 15 30 200 150 140 | – – – – – – – – – – – – | |
| Collector-Emitter Saturation Voltage (I _C = 10 mA, I _B = 0.3 mA) (I _C = 10 mA, I _B = 5 mA) NSBC113EPDXV6T1/NSBC123EPDXV6T1 (I _C = 10 mA, I _B = 1 mA) NSBC114TPDXV6T1/NSBC143TPDXV6T1 NSBC143EPDXV6T1/NSBC143ZPDXV6T1/NSBC124XPDXV6T1 | | V _{CE(sat)} | – | – | 0.25 | Vdc |

2. New resistor combinations. Updated curves to follow in subsequent data sheets.
3. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%

NSBC114EPDXV6T1, NSBC114EPDXV6T5

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted, common for Q₁ and Q₂, – minus sign for Q₁ (PNP) omitted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|-----------------|-------|-------|-------|------|
| ON CHARACTERISTICS (Note 3) | | | | | |
| Output Voltage (on) (V _{CC} = 5.0 V, V _B = 2.5 V, R _L = 1.0 kΩ) | V _{OL} | – | – | 0.2 | Vdc |
| NSBC114EPDXV6T1 | | – | – | 0.2 | |
| NSBC124EPDXV6T1 | | – | – | 0.2 | |
| NSBC114YPDXV6T1 | | – | – | 0.2 | |
| NSBC114TPDXV6T1 | | – | – | 0.2 | |
| NSBC143TPDXV6T1 | | – | – | 0.2 | |
| NSBC113EPDXV6T1 | | – | – | 0.2 | |
| NSBC123EPDXV6T1 | | – | – | 0.2 | |
| NSBC143EPDXV6T1 | | – | – | 0.2 | |
| NSBC143ZPDXV6T1 | | – | – | 0.2 | |
| NSBC124XPDXV6T1 | | – | – | 0.2 | |
| NSBC123JPDXV6T1 | | – | – | 0.2 | |
| (V _{CC} = 5.0 V, V _B = 3.5 V, R _L = 1.0 kΩ) | | – | – | 0.2 | |
| NSBC144EPDXV6T1 | | – | – | 0.2 | |
| Output Voltage (off) (V _{CC} = 5.0 V, V _B = 0.5 V, R _L = 1.0 kΩ) (V _{CC} = 5.0 V, V _B = 0.050 V, R _L = 1.0 kΩ) (V _{CC} = 5.0 V, V _B = 0.25 V, R _L = 1.0 kΩ) | V _{OH} | 4.9 | – | – | Vdc |
| NSBC113EPDXV6T1 | | | | | |
| NSBC114TPDXV6T1 | | | | | |
| NSBC143TPDXV6T1 | | | | | |
| NSBC143ZPDXV6T1 | | | | | |
| Input Resistor | R1 | 7.0 | 10 | 13 | k Ω |
| NSBC114EPDXV6T1 | | 15.4 | 22 | 28.6 | |
| NSBC124EPDXV6T1 | | 32.9 | 47 | 61.1 | |
| NSBC144EPDXV6T1 | | 7.0 | 10 | 13 | |
| NSBC114YPDXV6T1 | | 7.0 | 10 | 13 | |
| NSBC114TPDXV6T1 | | 3.3 | 4.7 | 6.1 | |
| NSBC143TPDXV6T1 | | 0.7 | 1.0 | 1.3 | |
| NSBC113EPDXV6T1 | | 1.5 | 2.2 | 2.9 | |
| NSBC123EPDXV6T1 | | 3.3 | 4.7 | 6.1 | |
| NSBC143EPDXV6T1 | | 3.3 | 4.7 | 6.1 | |
| NSBC143ZPDXV6T1 | | 15.4 | 22 | 28.6 | |
| NSBC124XPDXV6T1 | | 1.54 | 2.2 | 2.86 | |
| NSBC123JPDXV6T1 | | | | | |
| Resistor Ratio | R1/R2 | 0.8 | 1.0 | 1.2 | |
| NSBC114EPDXV6T1/NSBC124EPDXV6T1/NSBC144EPDXV6T1 | | 0.17 | 0.21 | 0.25 | |
| NSBC114YPDXV6T1 | | – | – | – | |
| NSBC114TPDXV6T1/NSBC143TPDXV6T1 | | 0.8 | 1.0 | 1.2 | |
| NSBC113EPDXV6T1/NSBC123EPDXV6T1/NSBC143EPDXV6T1 | | 0.055 | 0.1 | 0.185 | |
| NSBC143ZPDXV6T1 | | 0.38 | 0.47 | 0.56 | |
| NSBC124XPDXV6T1 | | 0.038 | 0.047 | 0.056 | |
| NSBC123JPDXV6T1 | | | | | |

2. New resistor combinations. Updated curves to follow in subsequent data sheets.

3. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%

NSBC114EPDXV6T1, NSBC114EPDXV6T5

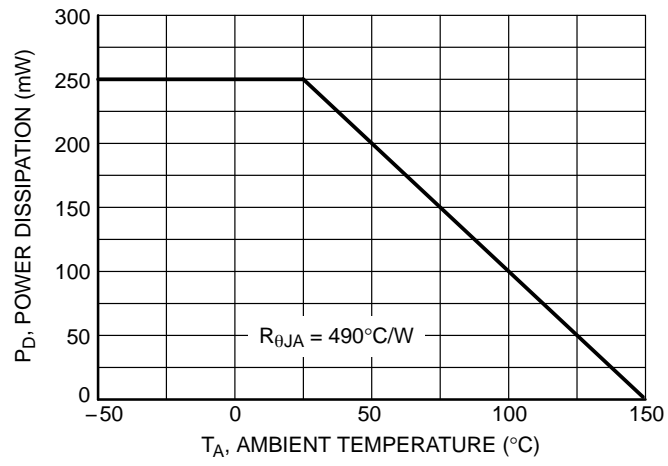


Figure 1. Derating Curve

NSBC114EPDXV6T1, NSBC114EPDXV6T5

TYPICAL ELECTRICAL CHARACTERISTICS – NSBC114EPDXV6T1 NPN TRANSISTOR

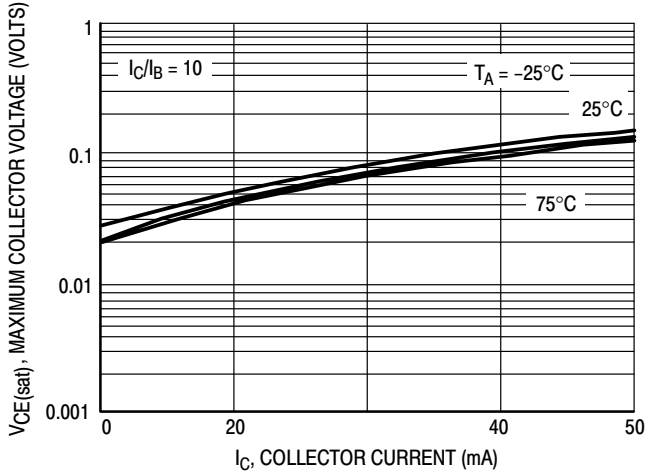


Figure 2. $V_{CE(sat)}$ versus I_C

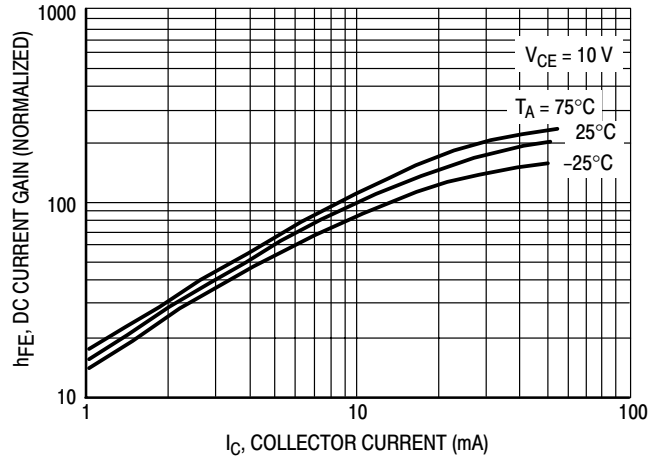


Figure 3. DC Current Gain

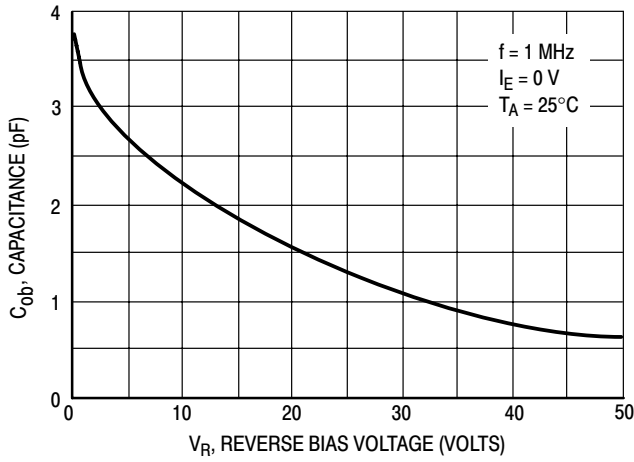


Figure 4. Output Capacitance

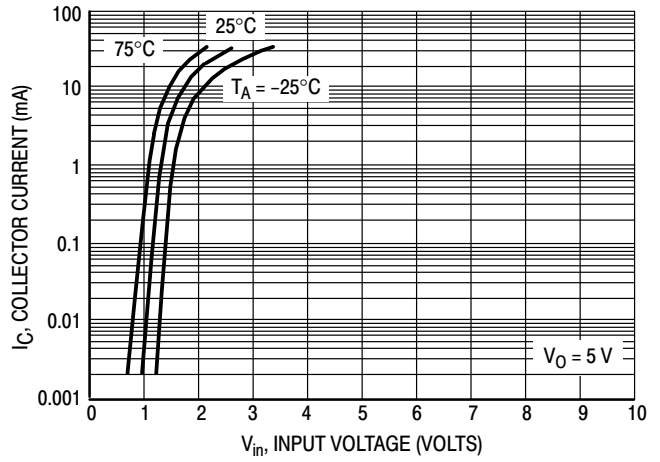


Figure 5. Output Current versus Input Voltage

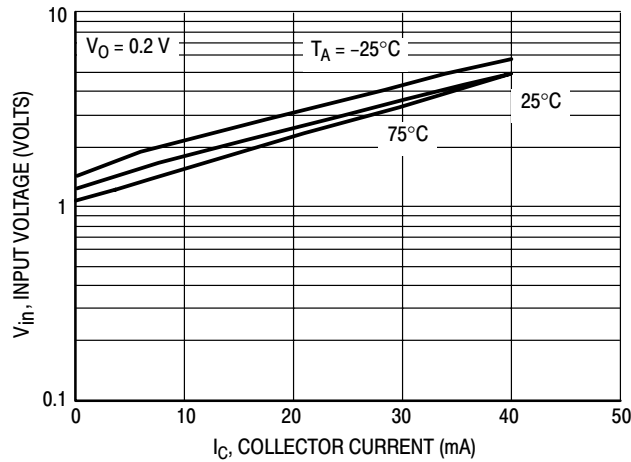


Figure 6. Input Voltage versus Output Current

NSBC114EPDXV6T1, NSBC114EPDXV6T5

TYPICAL ELECTRICAL CHARACTERISTICS – NSBC114EPDXV6T1 PNP TRANSISTOR

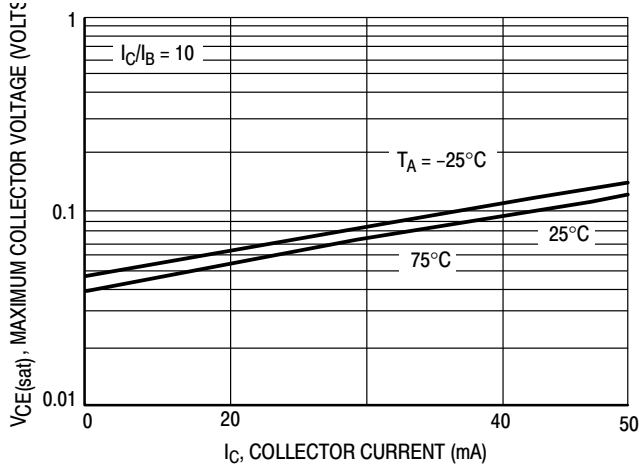


Figure 7. $V_{CE(sat)}$ versus I_C

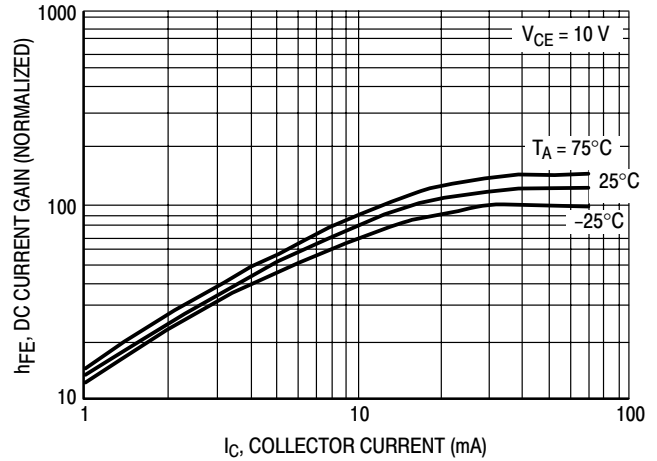


Figure 8. DC Current Gain

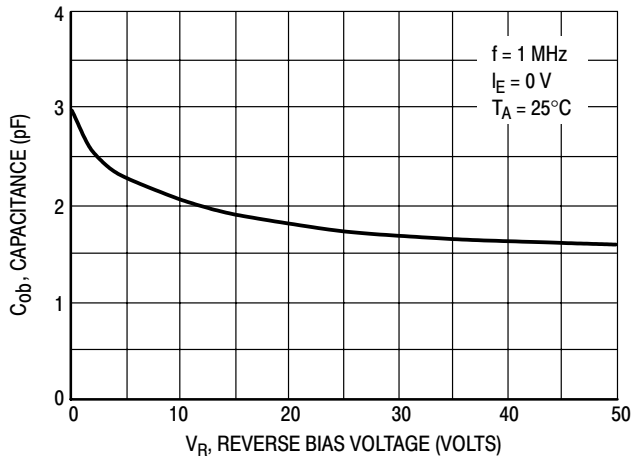


Figure 9. Output Capacitance

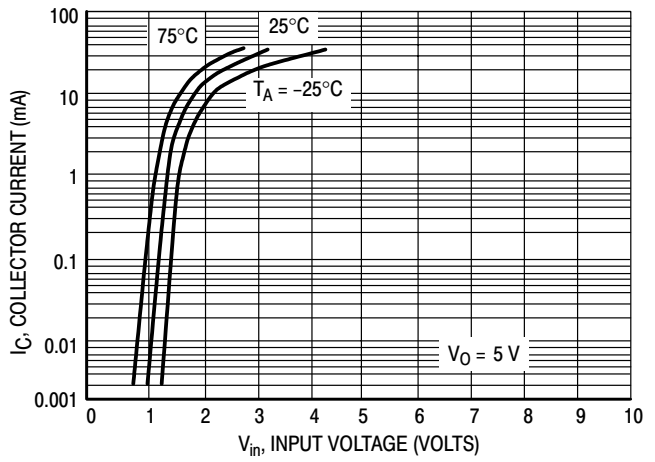


Figure 10. Output Current versus Input Voltage

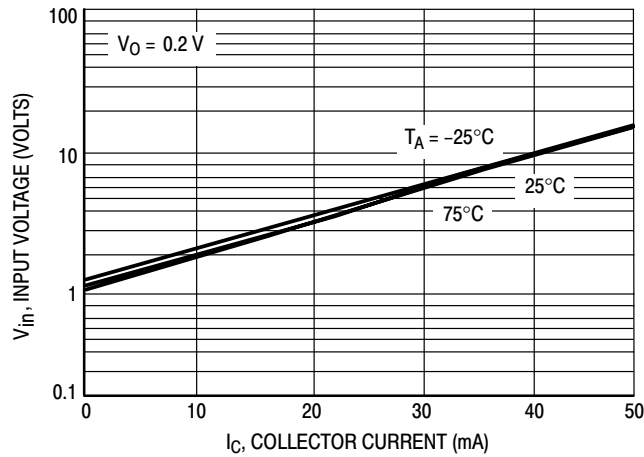


Figure 11. Input Voltage versus Output Current

NSBC114EPDXV6T1, NSBC114EPDXV6T5

TYPICAL ELECTRICAL CHARACTERISTICS – NSBC124EPDXV6T1 NPN TRANSISTOR

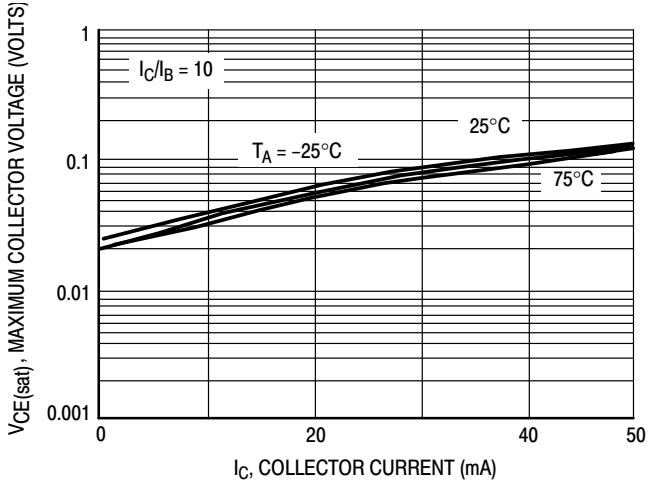


Figure 12. $V_{CE(sat)}$ versus I_C

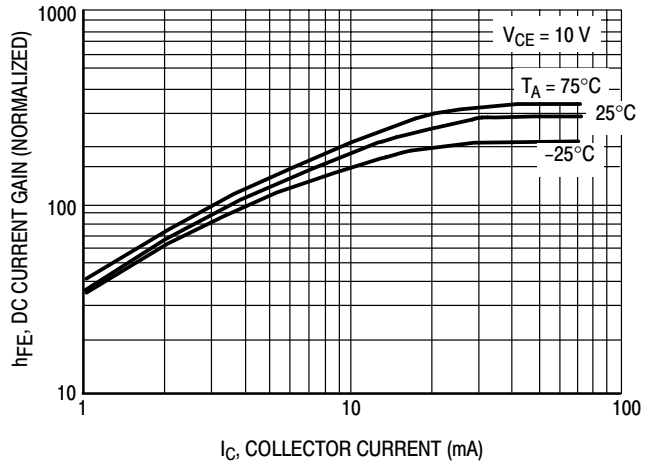


Figure 13. DC Current Gain

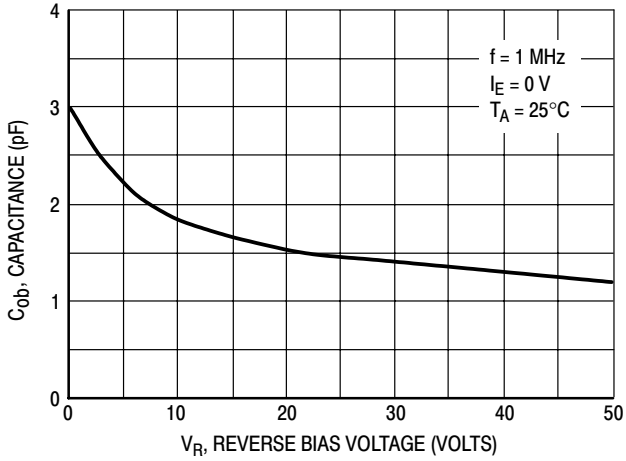


Figure 14. Output Capacitance

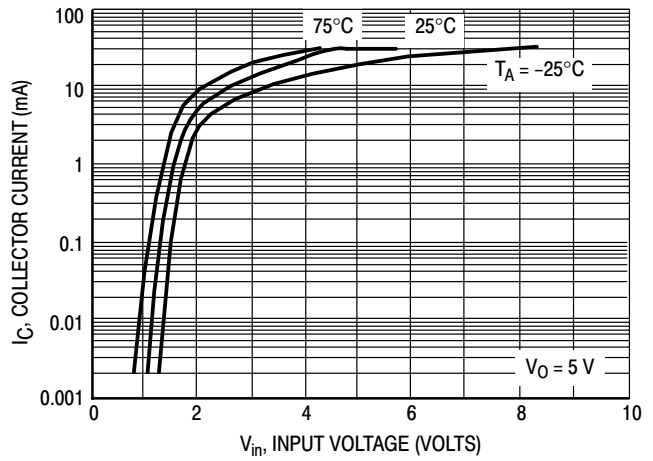


Figure 15. Output Current versus Input Voltage

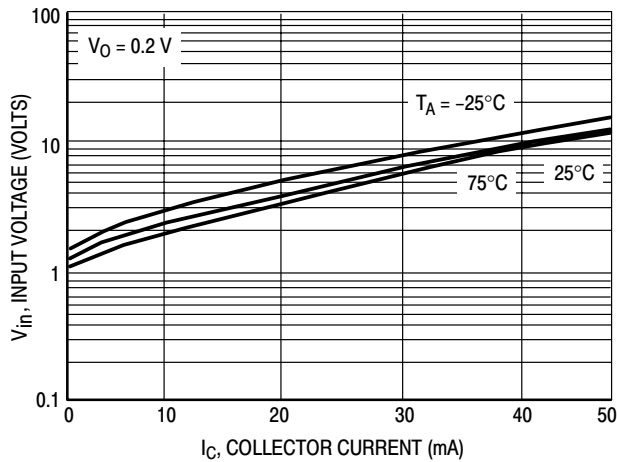


Figure 16. Input Voltage versus Output Current

NSBC114EPDXV6T1, NSBC114EPDXV6T5

TYPICAL ELECTRICAL CHARACTERISTICS – NSBC124EPDXV6T1 PNP TRANSISTOR

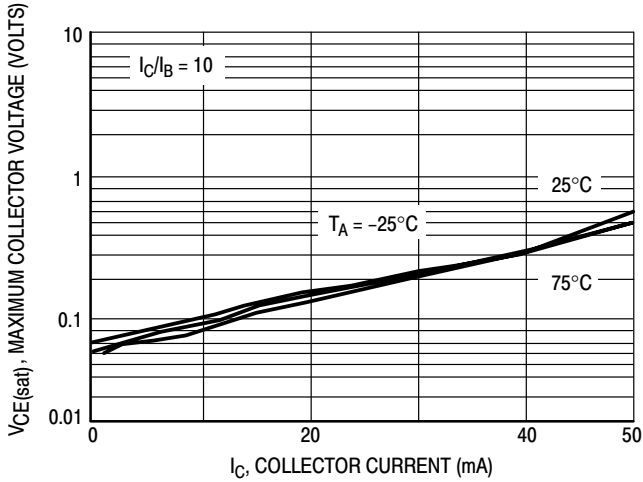


Figure 17. $V_{CE(sat)}$ versus I_C

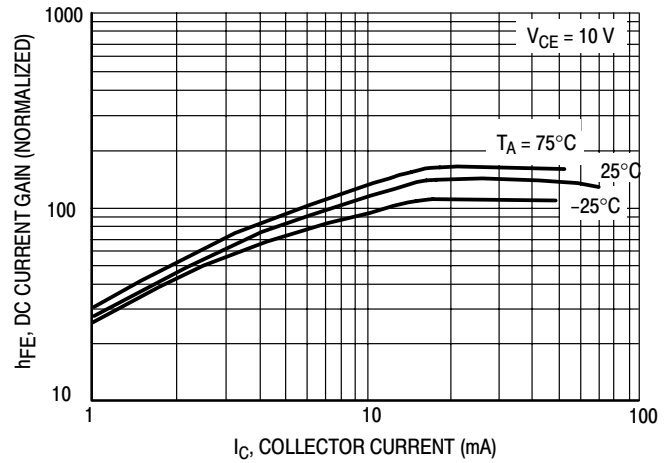


Figure 18. DC Current Gain

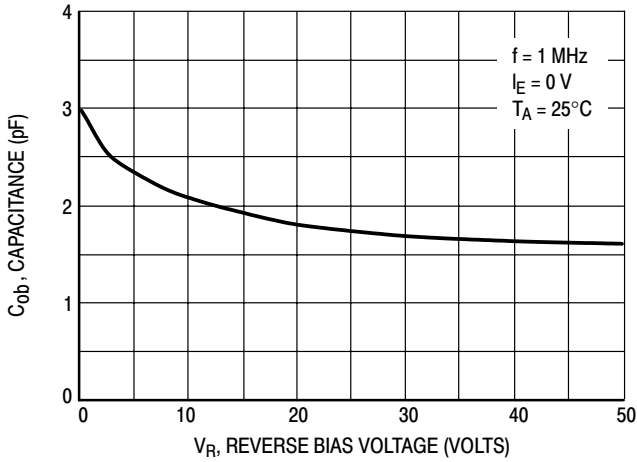


Figure 19. Output Capacitance

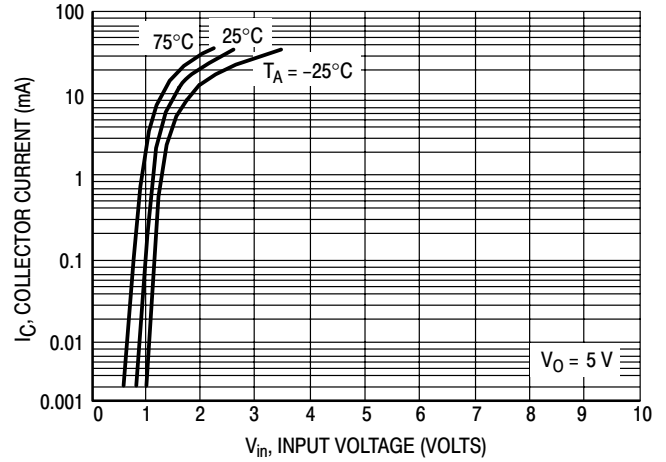


Figure 20. Output Current versus Input Voltage

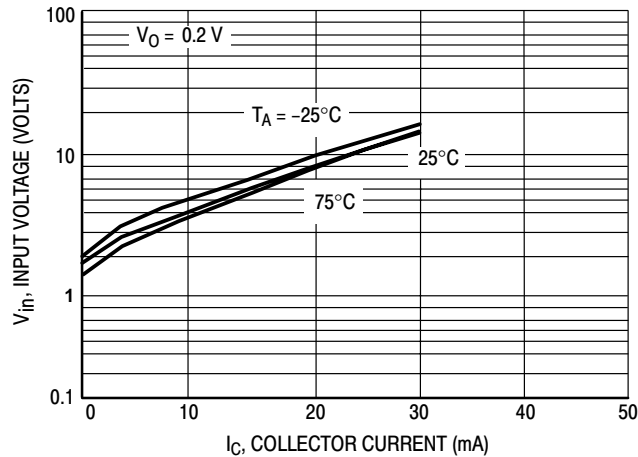


Figure 21. Input Voltage versus Output Current

NSBC114EPDXV6T1, NSBC114EPDXV6T5

TYPICAL ELECTRICAL CHARACTERISTICS – NSBC144EPDXV6T1 NPN TRANSISTOR

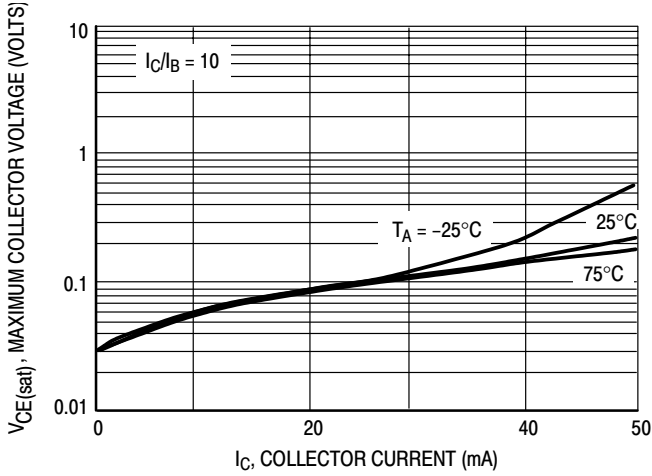


Figure 22. $V_{CE(sat)}$ versus I_C

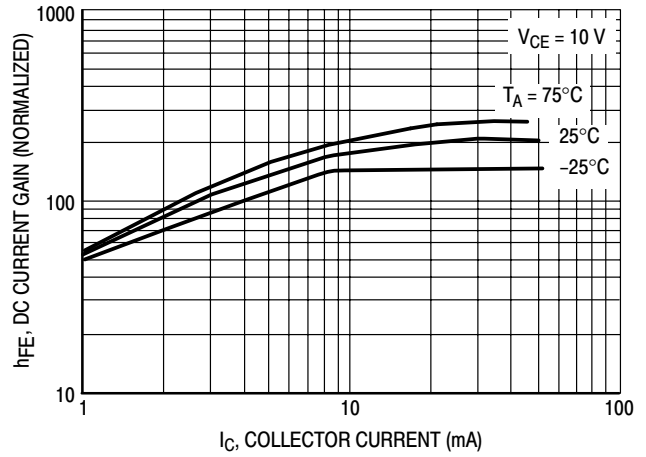


Figure 23. DC Current Gain

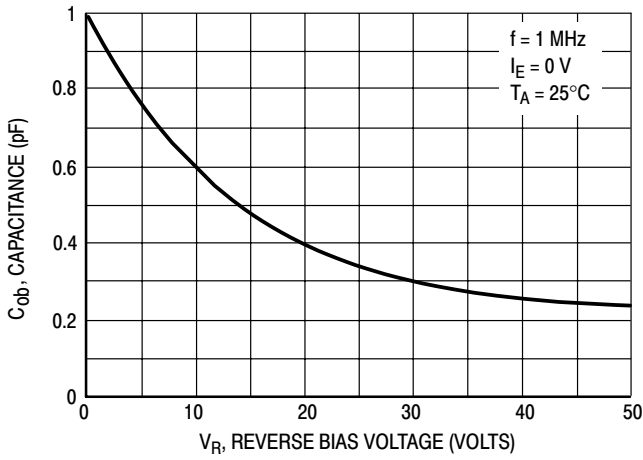


Figure 24. Output Capacitance

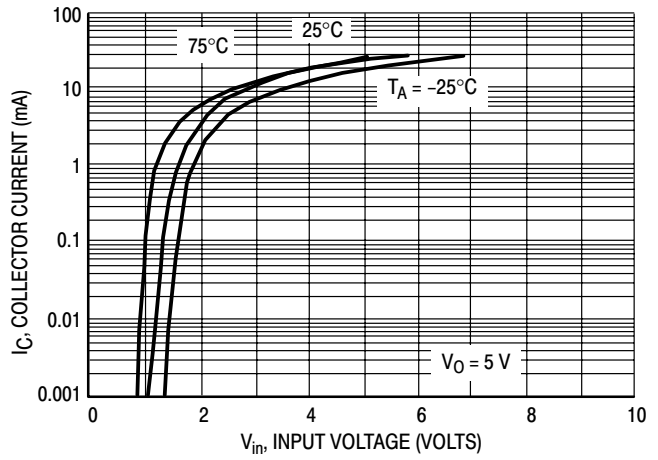


Figure 25. Output Current versus Input Voltage

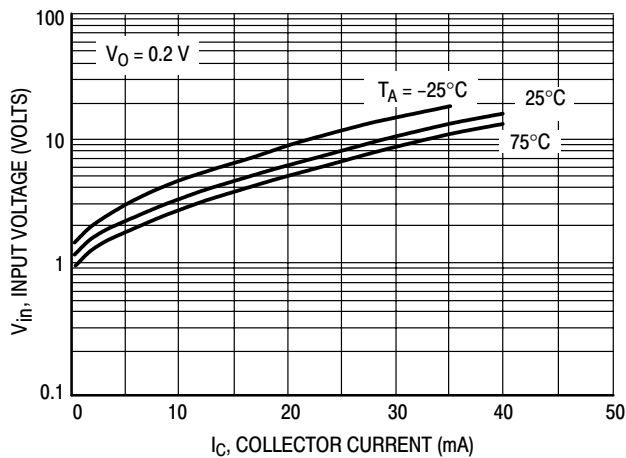


Figure 26. Input Voltage versus Output Current

NSBC114EPDXV6T1, NSBC114EPDXV6T5

TYPICAL ELECTRICAL CHARACTERISTICS – NSBC144EPDXV6T1 PNP TRANSISTOR

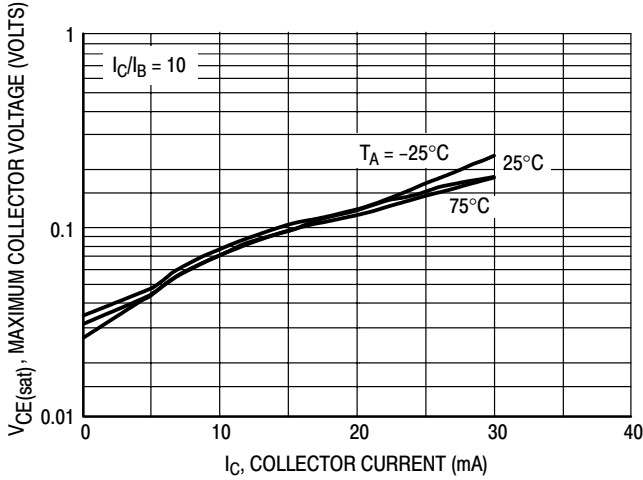


Figure 27. $V_{CE(sat)}$ versus I_C

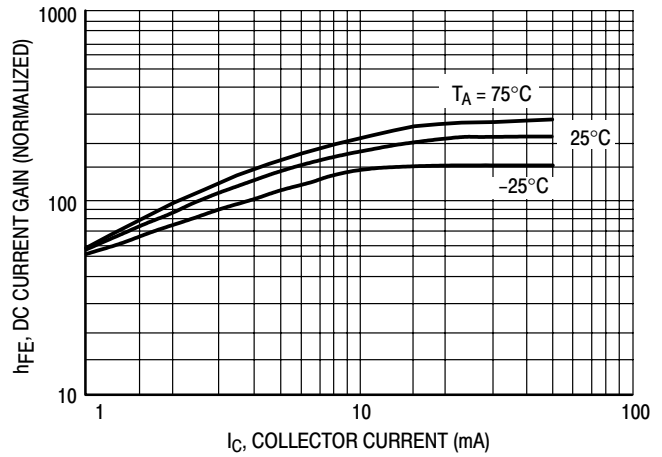


Figure 28. DC Current Gain

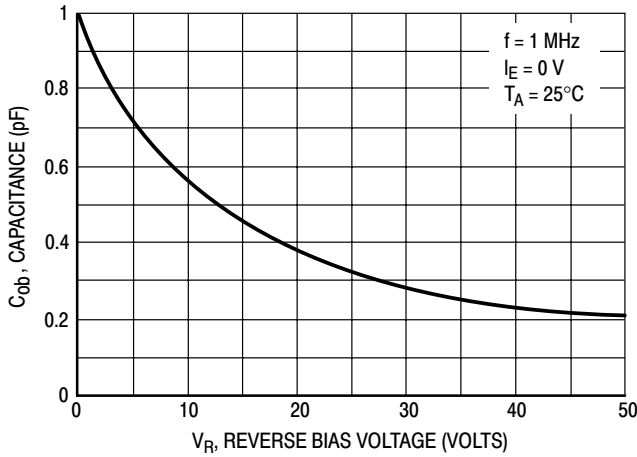


Figure 29. Output Capacitance

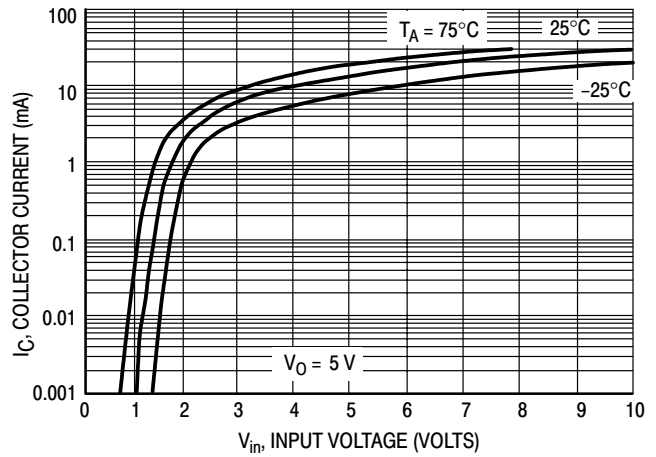


Figure 30. Output Current versus Input Voltage

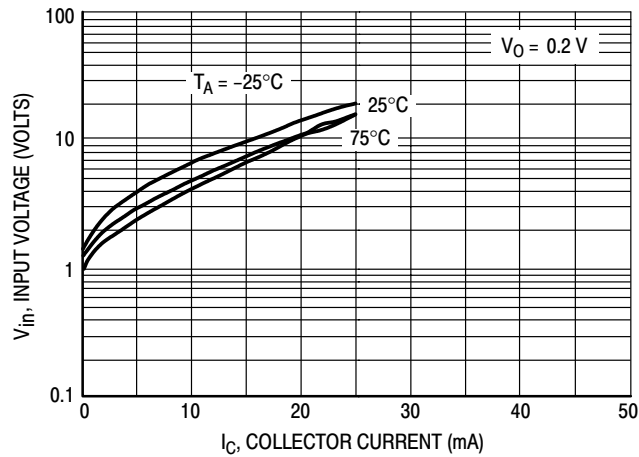


Figure 31. Input Voltage versus Output Current

NSBC114EPDXV6T1, NSBC114EPDXV6T5

TYPICAL ELECTRICAL CHARACTERISTICS – NSBC114YPDXV6T1 NPN TRANSISTOR

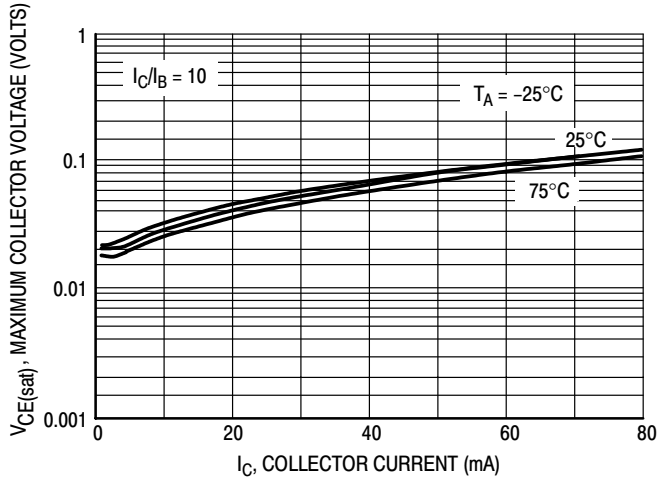


Figure 32. $V_{CE(sat)}$ versus I_C

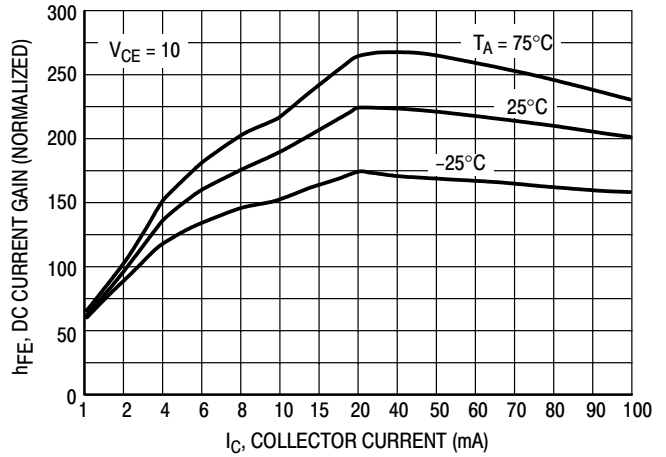


Figure 33. DC Current Gain

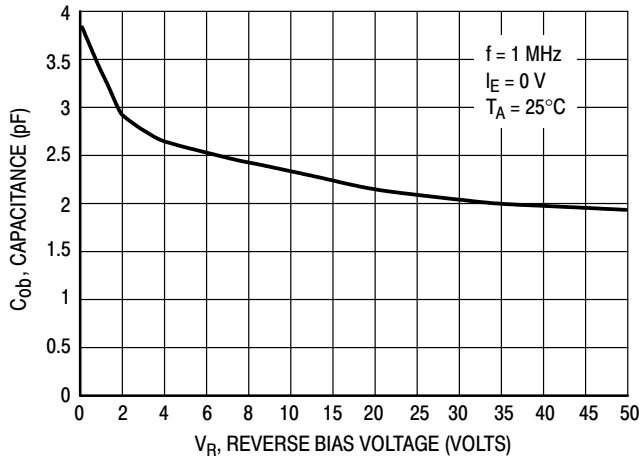


Figure 34. Output Capacitance

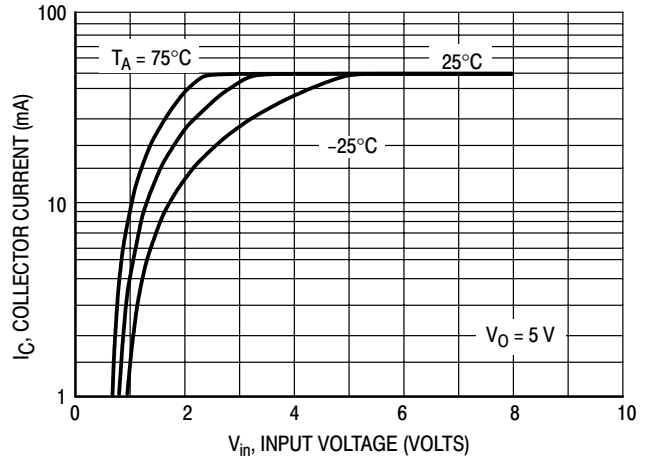


Figure 35. Output Current versus Input Voltage

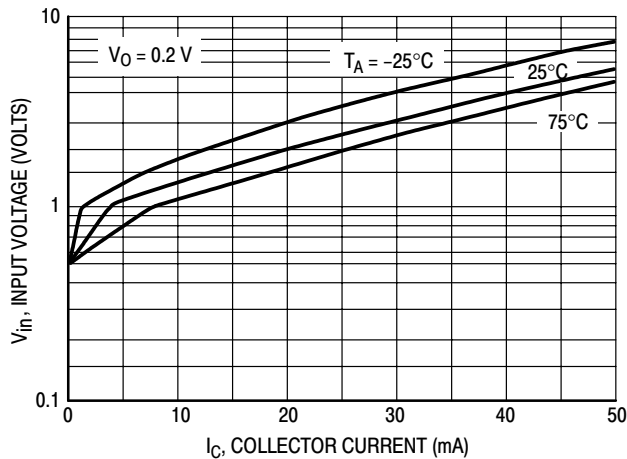


Figure 36. Input Voltage versus Output Current

NSBC114EPDXV6T1, NSBC114EPDXV6T5

TYPICAL ELECTRICAL CHARACTERISTICS – NSBC114YPDXV6T1 PNP TRANSISTOR

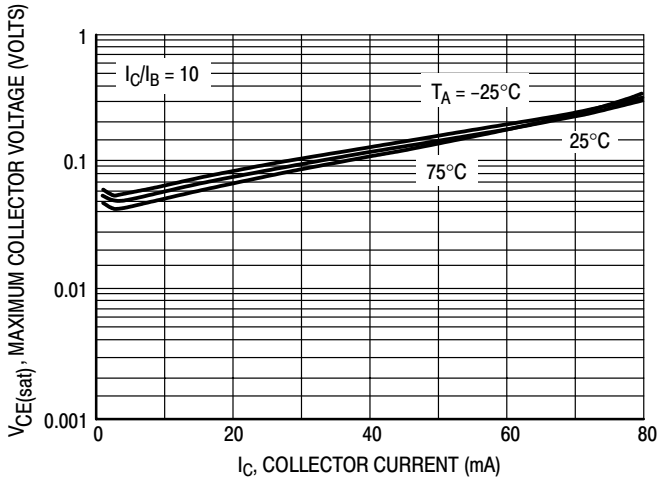


Figure 37. $V_{CE(sat)}$ versus I_C

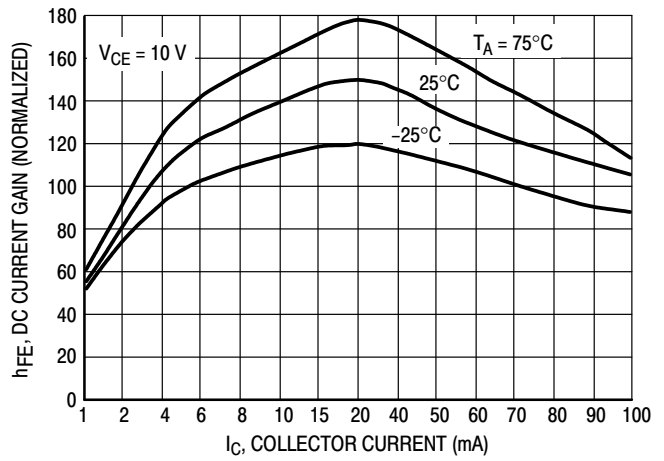


Figure 38. DC Current Gain

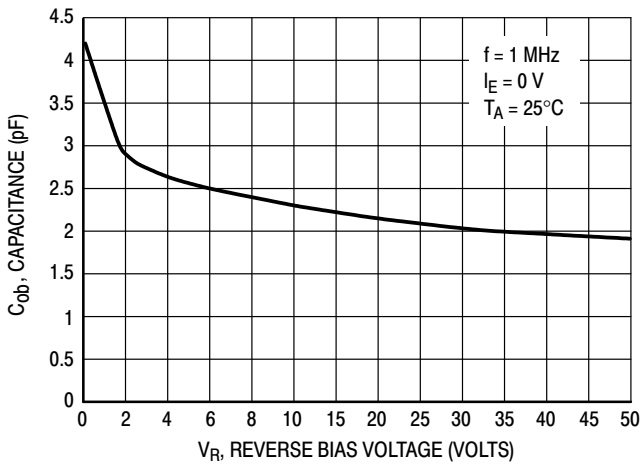


Figure 39. Output Capacitance

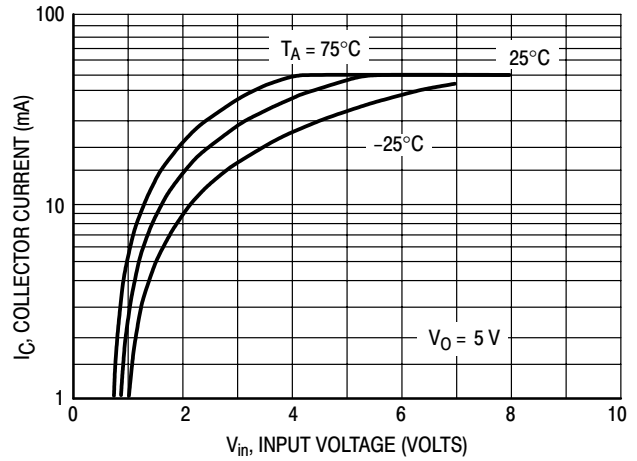


Figure 40. Output Current versus Input Voltage

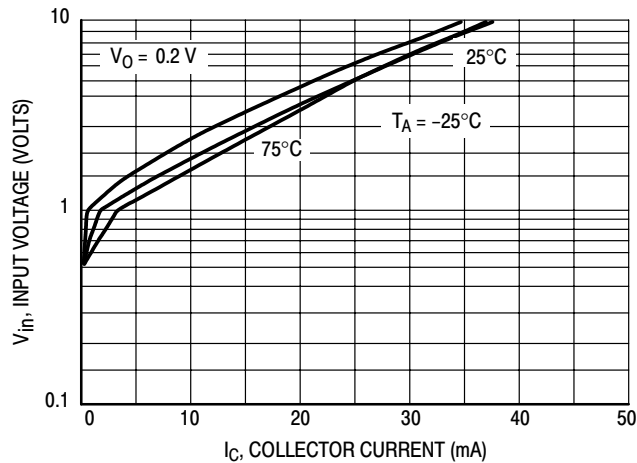


Figure 41. Input Voltage versus Output Current

NSBC114EPDXV6T1, NSBC114EPDXV6T5

TYPICAL ELECTRICAL CHARACTERISTICS – NSBC114TPDXV6T1

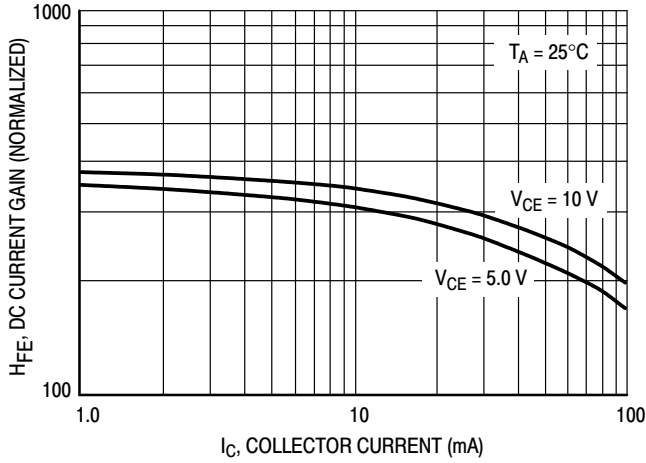


Figure 42. DC Current Gain – PNP

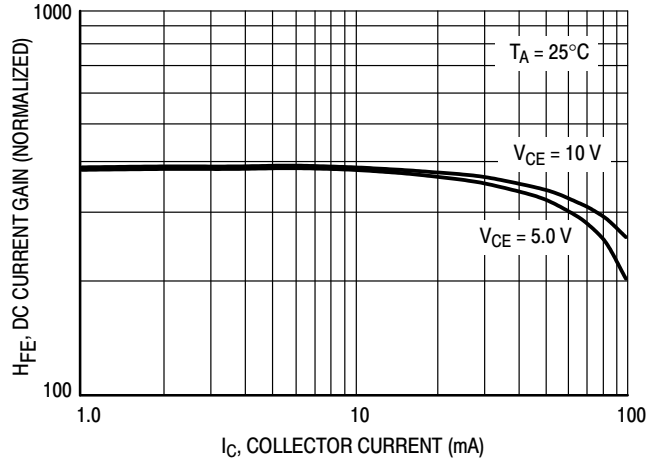


Figure 43. DC Current Gain – NPN

TYPICAL ELECTRICAL CHARACTERISTICS – NSBC143TPDXV6T1

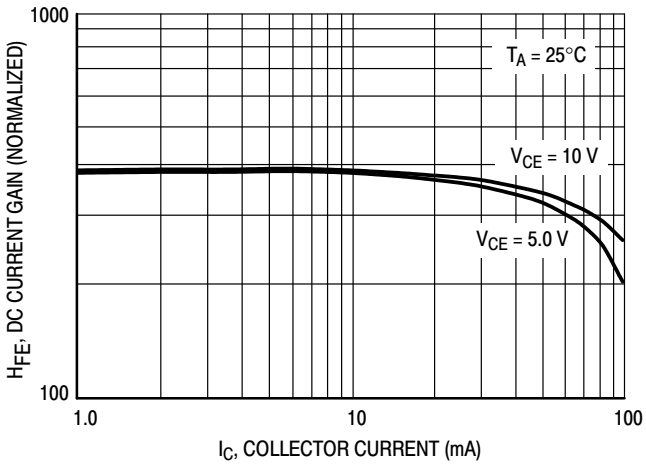


Figure 44. DC Current Gain – PNP

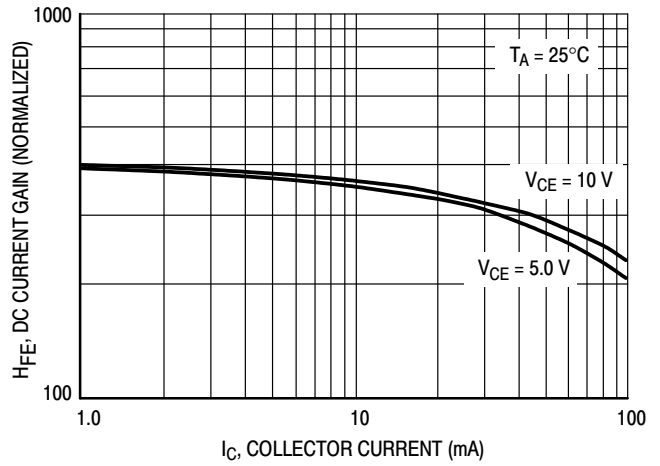
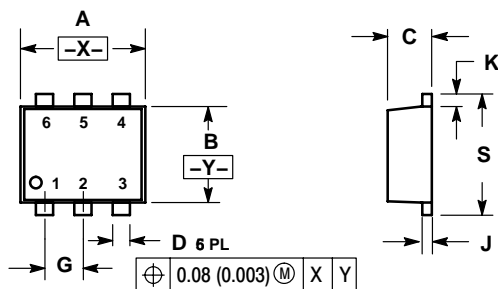


Figure 45. DC Current Gain – NPN

NSBC114EPDXV6T1, NSBC114EPDXV6T5

PACKAGE DIMENSIONS

SOT-563, 6 LEAD
CASE 463A-01
ISSUE O

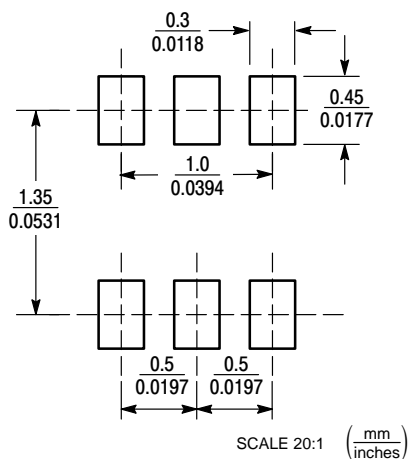


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETERS
 3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 1.50 | 1.70 | 0.059 | 0.067 |
| B | 1.10 | 1.30 | 0.043 | 0.051 |
| C | 0.50 | 0.60 | 0.020 | 0.024 |
| D | 0.17 | 0.27 | 0.007 | 0.011 |
| G | 0.50 BSC | | 0.020 BSC | |
| J | 0.08 | 0.18 | 0.003 | 0.007 |
| K | 0.10 | 0.30 | 0.004 | 0.012 |
| S | 1.50 | 1.70 | 0.059 | 0.067 |

- | | | | |
|---|---|---|--|
| <p>STYLE 1: PIN 1. EMITTER 1 2. BASE 1 3. COLLECTOR 2 4. EMITTER 2 5. BASE 2 6. COLLECTOR 1</p> | <p>STYLE 2: PIN 1. EMITTER 1 2. EMITTER 2 3. BASE 2 4. COLLECTOR 2 5. BASE 1 6. COLLECTOR 1</p> | <p>STYLE 3: PIN 1. CATHODE 1 2. CATHODE 1 3. ANODE/ANODE 2 4. CATHODE 2 5. CATHODE 2 6. ANODE/ANODE 1</p> | <p>STYLE 4: PIN 1. COLLECTOR 2. COLLECTOR 3. BASE 4. EMITTER 5. COLLECTOR 6. COLLECTOR</p> |
|---|---|---|--|

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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