

## MM74HC138

### 3-to-8 Line Decoder

#### General Description

The MM74HC138 decoder utilizes advanced silicon-gate CMOS technology and is well suited to memory address decoding or data routing applications. The circuit features high noise immunity and low power consumption usually associated with CMOS circuitry, yet has speeds comparable to low power Schottky TTL logic.

The MM74HC138 has 3 binary select inputs (A, B, and C). If the device is enabled, these inputs determine which one of the eight normally HIGH outputs will go LOW. Two active LOW and one active HIGH enables (G1, G2A and G2B) are provided to ease the cascading of decoders.

The decoder's outputs can drive 10 low power Schottky TTL equivalent loads, and are functionally and pin equivalent to the 74LS138. All inputs are protected from damage due to static discharge by diodes to  $V_{CC}$  and ground.

#### Features

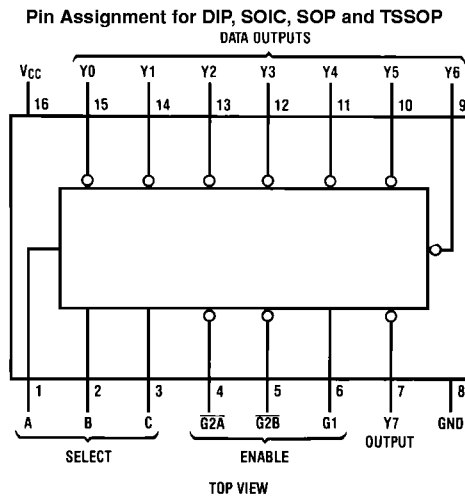
- Typical propagation delay: 20 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 80  $\mu$ A maximum (74HC Series)
- Low input current: 1  $\mu$ A maximum
- Fanout of 10 LS-TTL loads

#### Ordering Code:

Order Number	Package Number	Package Description
MM74HC138M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC138SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC138MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC138N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

#### Connection Diagram



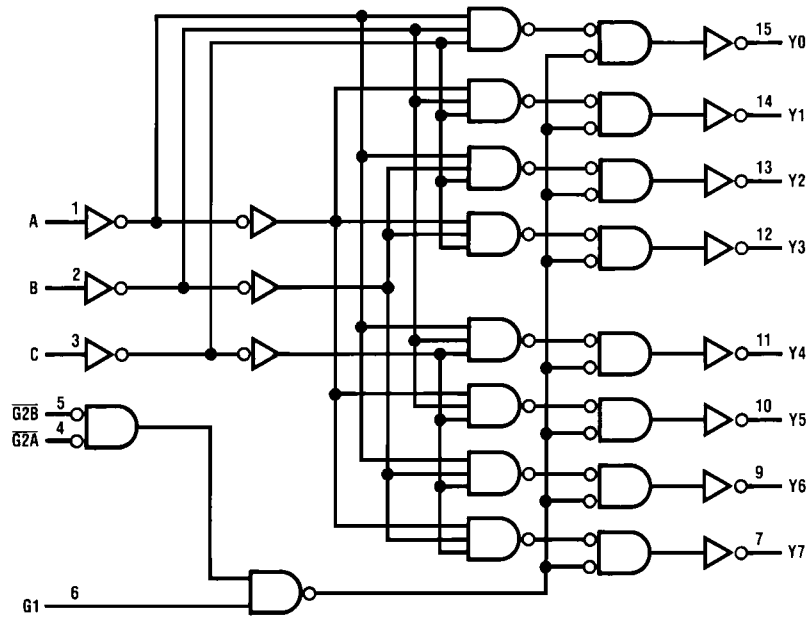
Truth Table

Inputs					Outputs							
Enable		Select										
G1	$\overline{G2}$ (Note 1)	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Level, L = LOW Level, X = don't care

Note 1:  $\overline{G2} = G2A + G2B$

Logic Diagram



Absolute Maximum Ratings <sup>(Note 2)</sup>		Recommended Operating Conditions		
(Note 3)				
Supply Voltage ( $V_{CC}$ )	- 0.5 to + 7.0V	Min	Max	Units
DC Input Voltage ( $V_{IN}$ )	- 1.5 to $V_{CC} + 1.5V$	2	6	V
DC Output Voltage ( $V_{OUT}$ )	- 0.5 to $V_{CC} + 0.5V$	0	$V_{CC}$	V
Clamp Diode Current ( $I_{IK}, I_{OK}$ )	$\pm 20$ mA	$(V_{IN}, V_{OUT})$		
DC Output Current, per pin ( $I_{OUT}$ )	$\pm 25$ mA	Operating Temperature Range ( $T_A$ )		
DC $V_{CC}$ or GND Current, per pin ( $I_{CC}$ )	$\pm 50$ mA	-40	+85	$^{\circ}C$
Storage Temperature Range ( $T_{STG}$ )	- 65 $^{\circ}C$ to + 150 $^{\circ}C$	Input Rise or Fall Times		
Power Dissipation ( $P_D$ )		$(t_r, t_f)$ $V_{CC} = 2.0V$	1000	ns
(Note 4)	600 mW	$V_{CC} = 4.5V$	500	ns
S.O. Package only	500 mW	$V_{CC} = 6.0V$	400	ns
Lead Temperature ( $T_L$ )	260 $^{\circ}C$	<b>Note 2:</b> Absolute Maximum Ratings are those values beyond which damage to the device may occur.		
(Soldering 10 seconds)		<b>Note 3:</b> Unless otherwise specified all voltages are referenced to ground.		
		<b>Note 4:</b> Power Dissipation temperature derating — plastic "N" package: - 12 mW/ $^{\circ}C$ from 65 $^{\circ}C$ to 85 $^{\circ}C$ .		

### DC Electrical Characteristics <sup>(Note 5)</sup>

Symbol	Parameter	Conditions	$V_{CC}$	$T_A = 25^{\circ}C$		$T_A = -40$ to $85^{\circ}C$		Units
				Typ	Guaranteed Limits			
$V_{IH}$	Minimum HIGH Level Input Voltage		2.0V		1.5	1.5	V	
			4.5V		3.15	3.15	V	
			6.0V		4.2	4.2	V	
$V_{IL}$	Maximum LOW Level Input Voltage		2.0V		0.5	0.5	V	
			4.5V		1.35	1.35	V	
			6.0V		1.8	1.8	V	
$V_{OH}$	Minimum HIGH Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 20 \mu A$	2.0V	2.0	1.9	1.9	V	
			4.5V	4.5	4.4	4.4	V	
			6.0V	6.0	5.9	5.9	V	
		$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 4.0$ mA $ I_{OUT}  \leq 5.2$ mA	4.5V	4.2	3.98	3.84	V	
			6.0V	5.7	5.48	5.34	V	
$V_{OL}$	Maximum LOW Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 20 \mu A$	2.0V	0	0.1	0.1	V	
			4.5V	0	0.1	0.1	V	
			6.0V	0	0.1	0.1	V	
		$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 4.0$ mA $ I_{OUT}  \leq 5.2$ mA	4.5V	0.2	0.26	0.33	V	
			6.0V	0.2	0.26	0.33	V	
$I_{IN}$	Maximum Input Current	$V_{IN} = V_{CC}$ or GND	6.0V		$\pm 0.1$	$\pm 1.0$	$\mu A$	
$I_{CC}$	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu A$	6.0V		8.0	80	$\mu A$	

**Note 5:** For a power supply of  $5V \pm 10\%$  the worst case output voltages ( $V_{OH}$ , and  $V_{OL}$ ) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case  $V_{IH}$  and  $V_{IL}$  occur at  $V_{CC} = 5.5V$  and 4.5V respectively. (The  $V_{IH}$  value at 5.5V is 3.85V.) The worst case leakage current ( $I_{IN}$ ,  $I_{CC}$ , and  $I_{OZ}$ ) occur for CMOS at the higher voltage and so the 6.0V values should be used.

## AC Electrical Characteristics

$V_{CC} = 5V$ ,  $T_A = 25^\circ C$ ,  $C_L = 15$  pF,  $t_r = t_f = 6$  ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
$t_{PLH}$	Maximum Propagation Delay, Binary Select to any Output		18	25	ns
$t_{PHL}$	Maximum Propagation Delay, Binary Select to any Output		28	35	ns
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay, G1 to any Output		18	25	ns
$t_{PHL}$	Maximum Propagation Delay $\overline{G2A}$ or $\overline{G2B}$ to Output		23	30	ns
$t_{PLH}$	Maximum Propagation Delay $\overline{G2A}$ or $\overline{G2B}$ to Output		18	25	ns

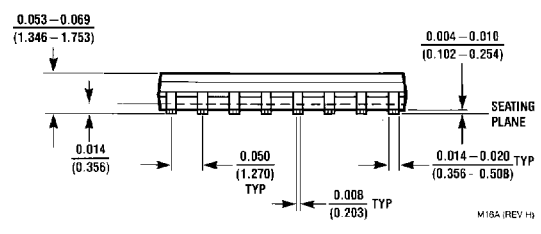
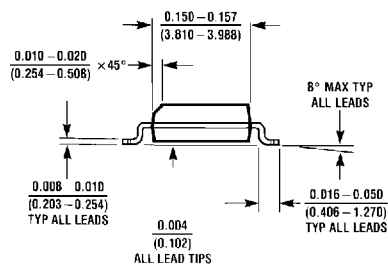
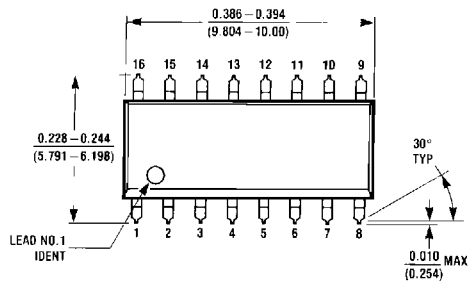
## AC Electrical Characteristics

$C_L = 50$  pF,  $t_r = t_f = 6$  ns (unless otherwise specified)

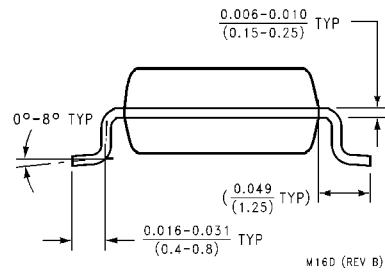
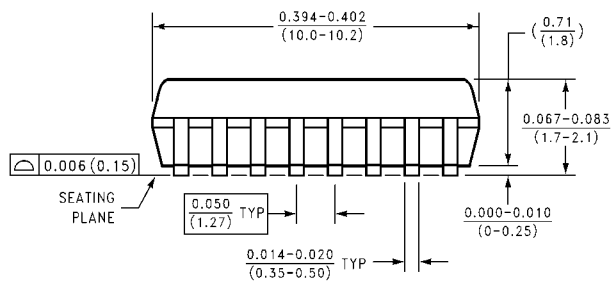
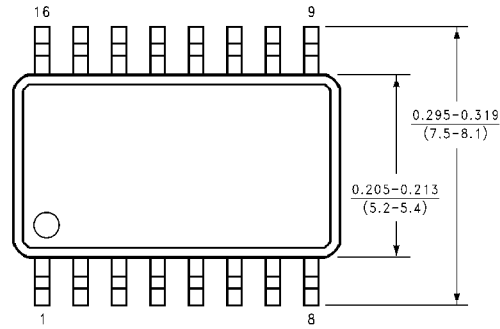
Symbol	Parameter	Conditions	$V_{CC}$	$T_A = 25^\circ C$		$T_A = -40$ to $85^\circ C$	Units
				Typ	Guaranteed Limits		
$t_{PLH}$	Maximum Propagation Delay Binary Select to any Output LOW-to-HIGH		2.0V	75	150	189	ns
			4.5V	15	30	38	ns
			6.0V	13	26	32	ns
$t_{PHL}$	Maximum Propagation Delay Binary Select to any Output HIGH-to-LOW		2.0V	100	200	252	ns
			4.5V	20	40	50	ns
			6.0V	17	34	43	ns
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay G1 to any Output		2.0V	75	150	189	ns
			4.5V	15	30	38	ns
			6.0V	13	26	32	ns
$t_{PHL}$	Maximum Propagation Delay $\overline{G2A}$ or $\overline{G2B}$ to Output		2.0V	82	175	221	ns
			4.5V	28	35	44	ns
			6.0V	22	30	37	ns
$t_{PLH}$	Maximum Propagation Delay $\overline{G2A}$ or $\overline{G2B}$ to Output		2.0V	75	150	189	ns
			4.5V	15	30	38	ns
			6.0V	13	26	32	ns
$t_{TLH}$ , $t_{THL}$	Output Rise and Fall Time		2.0V	30	75	95	ns
			4.5V	8	15	19	ns
			6.0V	7	13	16	ns
$C_{IN}$	Maximum Input Capacitance			3	10	10	pF
$C_{PD}$	Power Dissipation Capacitance	(Note 6)		75			pF

**Note 6:**  $C_{PD}$  determines the no load dynamic power consumption,  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ , and the no load dynamic current consumption,  $I_S = C_{PD} V_{CC} f + I_{CC}$ .

**Physical Dimensions** inches (millimeters) unless otherwise noted

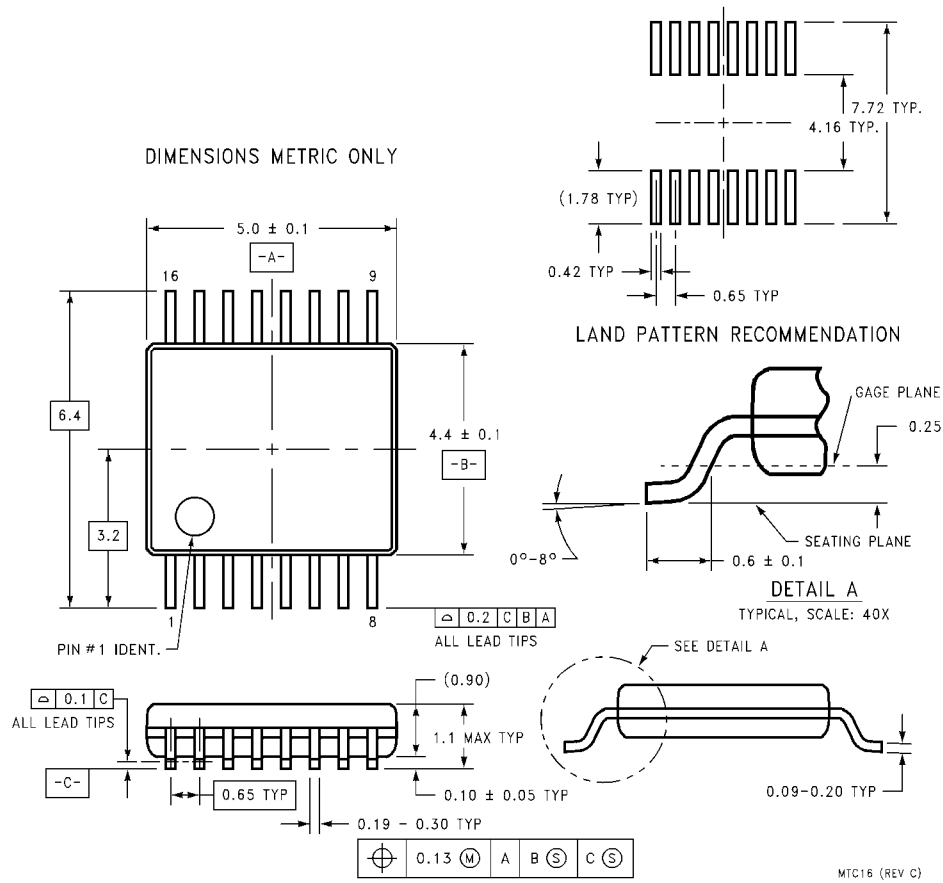


**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow  
Package Number M16A**



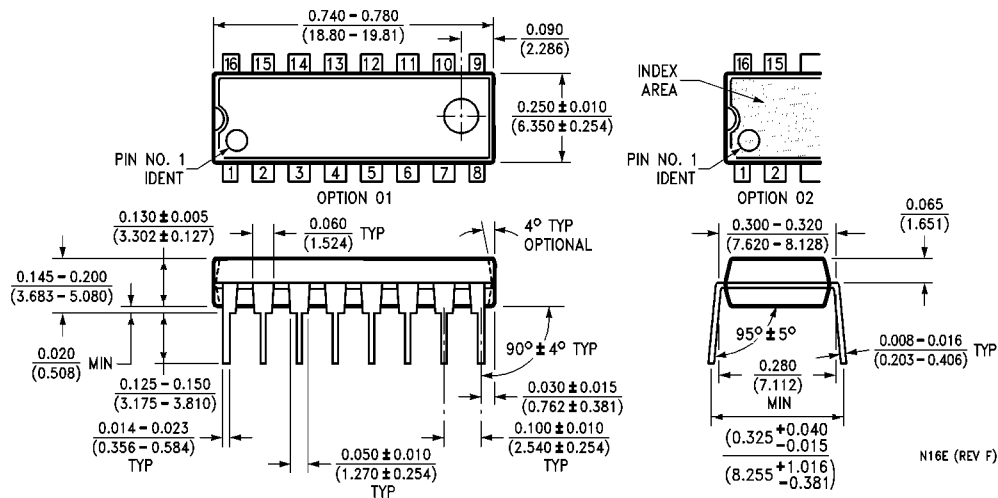
**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
Package Number M16D**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide  
Package Number MTC16**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N16E**

N16E (REV F)

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