MC14070B, MC14077B

CMOS SSI

Quad Exclusive "OR" and "NOR" Gates

The MC14070B quad exclusive OR gate and the MC14077B quad exclusive NOR gate are constructed with MOS P–channel and N–channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low–Power TTL Loads or One Low–Power Schottky TTL Load Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- MC14070B — Replacement for CD4030B and CD4070B Types
- MC14077B — Replacement for CD4077B Type

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic "P and D/DW" Packages: − 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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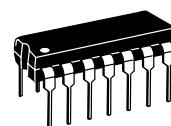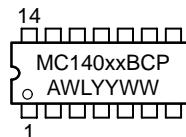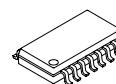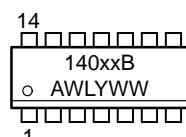
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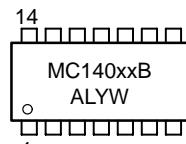
ORDERING INFORMATION

| Device	Package	Shipping
MC140XXBCP	PDIP–14	2000/Box
MC140XXBD	SOIC–14	2750/Box
MC140XXBDR2	SOIC–14	2500/Tape & Reel
MC140XXBF	SOEIAJ–14	See Note 1.
MC140XXBFEL	SOEIAJ–14	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

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PIN ASSIGNMENT

IN 1_A	1 ●		14	V_{DD}
IN 2_A	2		13	IN 2_D
OUT_A	3		12	IN 1_D
OUT_B	4		11	OUT_D
IN 1_B	5		10	OUT_C
IN 2_B	6		9	IN 2_C
V_{SS}	7		8	IN 1_C
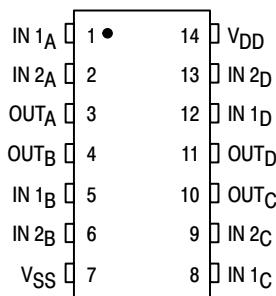
MC14070B
QUAD Exclusive OR
Gate

MC14077B
**QUAD Exclusive NOR**
Gate
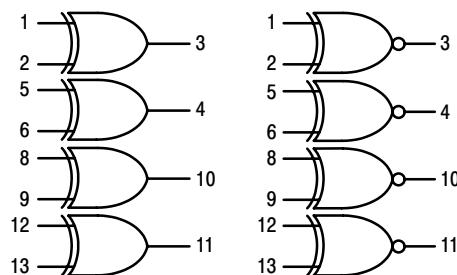
V_{DD} = PIN 14
V_{SS} = PIN 7
(BOTH DEVICES)

*Inverted output on MC14077B only.
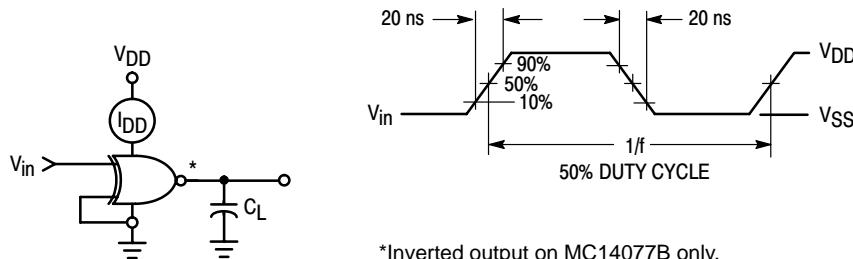
Figure 1. Power Dissipation Test Circuit and Waveform

*Inverted output on MC14077B only.
#Connect unused input to V_{DD} for MC14070B, to V_{SS} for MC14077B.
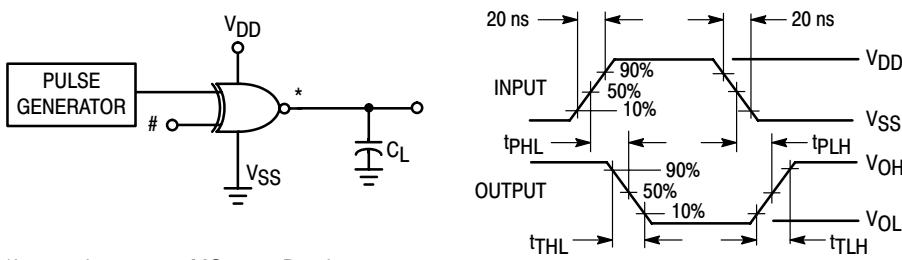
Figure 2. Switching Time Test Circuit and Waveforms

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	– 55°C		25°C			125°C		Unit
				Min	Max	Min	Typ [4.]	Max	Min	Max	
Output Voltage "0" Level $V_{in} = V_{DD}$ or 0		V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
			10	—	0.05	—	0	0.05	—	0.05	
			15	—	0.05	—	0	0.05	—	0.05	
"1" Level $V_{in} = 0$ or V_{DD}		V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
			10	9.95	—	9.95	10	—	9.95	—	
			15	14.95	—	14.95	15	—	14.95	—	
Input Voltage "0" Level (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)		V_{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
			10	—	3.0	—	4.50	3.0	—	3.0	
			15	—	4.0	—	6.75	4.0	—	4.0	
"1" Level (V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)		V_{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
			10	7.0	—	7.0	5.50	—	7.0	—	
			15	11	—	11	8.25	—	11	—	
Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)		I_{OH}	5.0	– 3.0	—	– 2.4	– 4.2	—	– 1.7	—	mAdc
			5.0	– 0.64	—	– 0.51	– 0.88	—	– 0.36	—	
			10	– 1.6	—	– 1.3	– 2.25	—	– 0.9	—	
			15	– 4.2	—	– 3.4	– 8.8	—	– 2.4	—	
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)		I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
			10	1.6	—	1.3	2.25	—	0.9	—	
			15	4.2	—	3.4	8.8	—	2.4	—	
Input Current		I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)		C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)		I_{DD}	5.0	—	0.25	—	0.0005	0.25	—	7.5	µAdc
			10	—	0.5	—	0.0010	0.5	—	15	
			15	—	1.0	—	0.0015	1.0	—	30	
Total Supply Current [5.] [6.] (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)		I_T	5.0	I_T = (0.3 µA/kHz) f + I_{DD}							µAdc
			10	I_T = (0.6 µA/kHz) f + I_{DD}							
			15	I_T = (0.9 µA/kHz) f + I_{DD}							
Output Rise and Fall Times [5.] (C_L = 50 pF) t_{TLH}, t_{THL} = (1.35 ns/pF) C_L + 33 ns t_{TLH}, t_{THL} = (0.60 ns/pF) C_L + 20 ns t_{TLH}, t_{THL} = (0.40 ns/pF) C_L + 20 ns		t_{TLH}, t_{THL}	5.0	—	—	—	100	200	—	—	ns
			10	—	—	—	50	100	—	—	
			15	—	—	—	40	80	—	—	
Propagation Delay Times [5.] (C_L = 50 pF) t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 130 ns t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 57 ns t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 37 ns		t_{PLH}, t_{PHL}	5.0	—	—	—	175	350	—	—	ns
			10	—	—	—	75	150	—	—	
			15	—	—	—	55	110	—	—	

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
5. The formulas given are for the typical characteristics only at 25°C.
6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: I_T is in µH (per package), C_L in pF, V = ($V_{DD} - V_{SS}$) in volts, f in kHz is input frequency, and k = 0.002.