

74F534 Octal D-Type Flip-Flop with 3-STATE Outputs

General Description

The 'F534 is a high speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable (\overline{OE}) are common to all flip-flops. The 'F534 is the same as the 'F374 except that the outputs are inverted.

Features

- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- 3-STATE outputs for bus-oriented applications
- Guaranteed 4000V minimum ESD protection

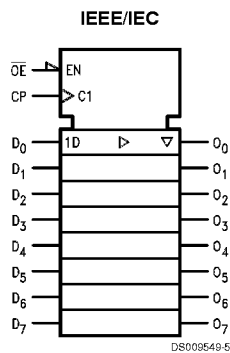
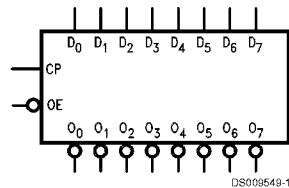
Ordering Code:

Commercial	Military	Package Number	Package Description
74F534PC		N20A	20-Lead (0.300" Wide) Molded Dual-In-Line
	54F534DM (Note 2)	J20A	20-Lead Ceramic Dual-In-Line
74F534SC (Note 1)		M20B	20-Lead (0.300" Wide) Molded Small Outline, JEDEC
74F534SJ (Note 1)		M20D	20-Lead (0.300" Wide) Molded Small Outline, EIAJ
	54F534FM (Note 2)	W20A	20-Lead Cerpack
	54F534LM (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

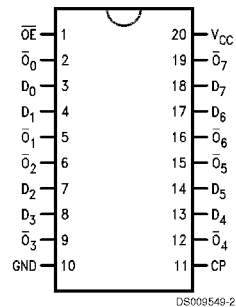
Note 1: Devices also available in 13" reel. Use suffix = SCX, and SJX

Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB

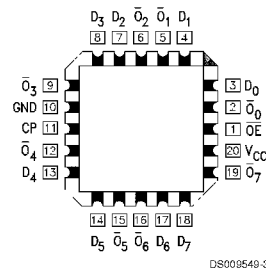
Logic Symbols



Connection Diagrams



Pin Assignment for LCC



Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
D ₀ -D ₇	Data Inputs	1.0/1.0	20 μ A/-0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μ A/-0.6 mA
\overline{OE}	3-STATE Output Enable Input (Active LOW)	1.0/1.0	20 μ A/-0.6 mA
\overline{O}_0 - \overline{O}_7	Complementary 3-STATE Outputs	150/40(33.3)	-3 mA/24 mA (20 mA)

Functional Description

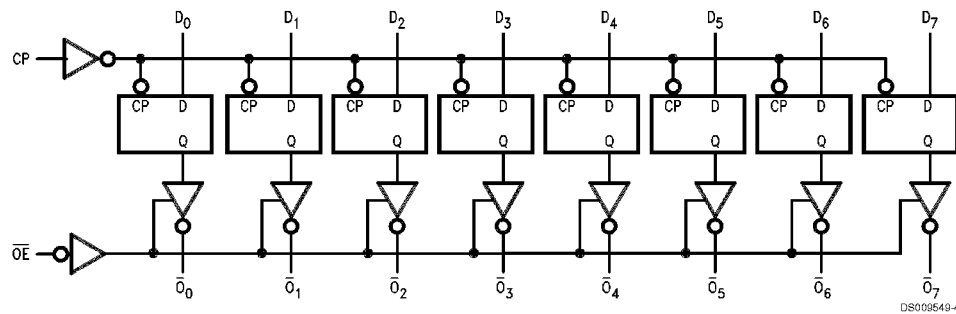
The 'F534 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-STATE complementary outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH clock (CP) transition. With the Output Enable (\overline{OE}) LOW, the contents of the eight flip-flops are available at the outputs. When the \overline{OE} is HIGH, the outputs go to the high impedance state. Operation of the \overline{OE} input does not affect the state of the flip-flops.

Function Table

CP	Inputs		Output
	OE	D	\overline{O}
\nearrow	L	H	L
\nearrow	L	L	H
L	L	X	\overline{O}_0
X	H	X	Z

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 \nearrow = LOW-to-HIGH Clock Transition
 Z = High Impedance
 \overline{O}_0 = Value stored from previous clock cycle

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 3)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
Plastic	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 4)	-0.5V to +7.0V
Input Current (Note 4)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}
3-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)

ESD Last Passing Voltage (Min)

4000V

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

Note 3: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 4: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		54F/74F			Units	V _{CC}	Conditions
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage		0.8			V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage		-1.2			V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54F 10% V _{CC}	2.5		V	Min	I _{OH} = -1 mA	
		54F 10% V _{CC}	2.4				I _{OH} = -3 mA	
		74F 10% V _{CC}	2.5				I _{OH} = -1 mA	
		74F 10% V _{CC}	2.4				I _{OH} = -3 mA	
		74F 5% V _{CC}	2.7				I _{OH} = -1 mA	
		74F 5% V _{CC}	2.7				I _{OH} = -3 mA	
V _{OL}	Output LOW Voltage	54F 10% V _{CC}	0.5		V	Min	I _{OL} = 20 mA	
		74F 10% V _{CC}	0.5				I _{OL} = 24 mA	
I _{IH}	Input HIGH Current	54F	20.0		μA	Max	V _{IN} = 2.7V	
		74F	5.0					
I _{BVI}	Input HIGH Breakdown Test	54F	100		μA	Max	V _{IN} = 7.0V	
		74F	7.0					
I _{CEX}	Output HIGH Leakage Current	54F	250		μA	Max	V _{OUT} = V _{CC}	
		74F	50					
V _{ID}	Input Leakage Test	74F	4.75		V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded	
I _{OD}	Output Leakage Circuit Current	74F	3.75		μA	0.0	V _{IOD} = 1.50 μA All Other Pins Grounded	
I _{IL}	Input LOW Current		-0.6		mA	Max	V _{IN} = 0.5V	
I _{OZH}	Output Leakage Current		50		μA	Max	V _{OUT} = 2.7V	
I _{OZL}	Output Leakage Current		-50		μA	Max	V _{OUT} = 0.5V	
I _{OS}	Output Short-Circuit Current		-60	-150	mA	Max	V _{OUT} = 0V	
I _{ZZ}	Bus Drainage Test		500		μA	0.0V	V _{OUT} = 5.25V	
I _{CCZ}	Power Supply Current		55	86	mA	Max	V _O = HIGH Z	

AC Electrical Characteristics

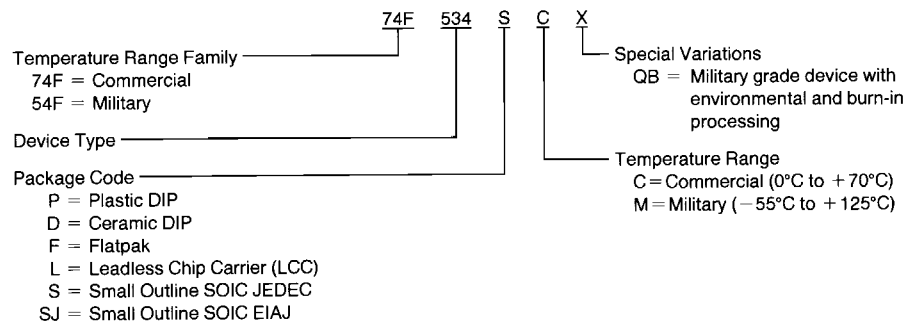
Symbol	Parameter	74F			54F		74F		Units
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$		
		Min	Typ	Max	Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency	100			60		70		MHz
t_{PLH}	Propagation Delay	4.0	6.5	8.5	4.0	10.5	4.0	10.0	ns
t_{PHL}	CP to \overline{O}_n	4.0	6.5	8.5	4.0	11.0	4.0	10.0	
t_{PZH}	Output Enable Time	2.0	9.0	11.5	2.0	14.0	2.0	12.5	ns
t_{PZL}	Output Disable Time	2.0	5.8	7.5	2.0	10.0	2.0	8.5	
t_{PHZ}	Output Disable Time	1.5	5.3	7.0	1.5	8.0	1.5	8.0	
t_{PLZ}	Output Disable Time	1.5	4.3	5.5	1.5	7.5	1.5	6.5	

AC Operating Requirements

Symbol	Parameter	74F		54F		74F		Units
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$		
		Min	Max	Min	Max	Min	Max	
$t_s(\text{H})$	Setup Time, HIGH or LOW	2.0		2.0		2.0		ns
$t_s(\text{L})$	D_n to CP	2.0		2.5		2.0		
$t_h(\text{H})$	Hold Time, HIGH or LOW	2.0		2.0		2.0		ns
$t_h(\text{L})$	D_n to CP	2.0		2.5		2.0		
$t_w(\text{H})$	CP Pulse Width	7.0		7.0		7.0		ns
$t_w(\text{L})$	HIGH or LOW	6.0		6.0		6.0		

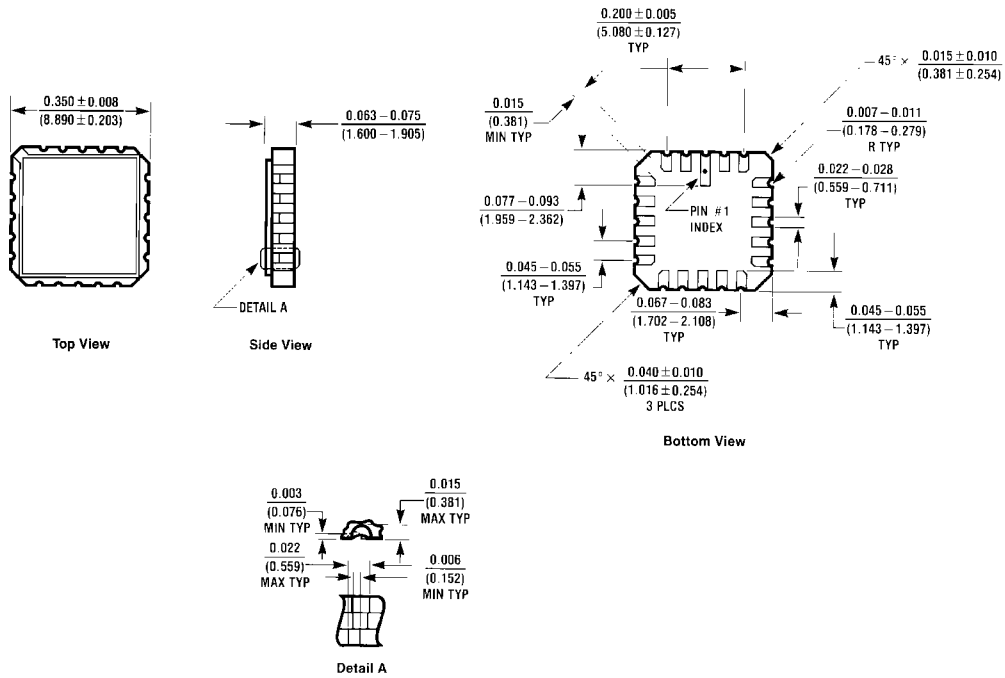
Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



DS001549-6

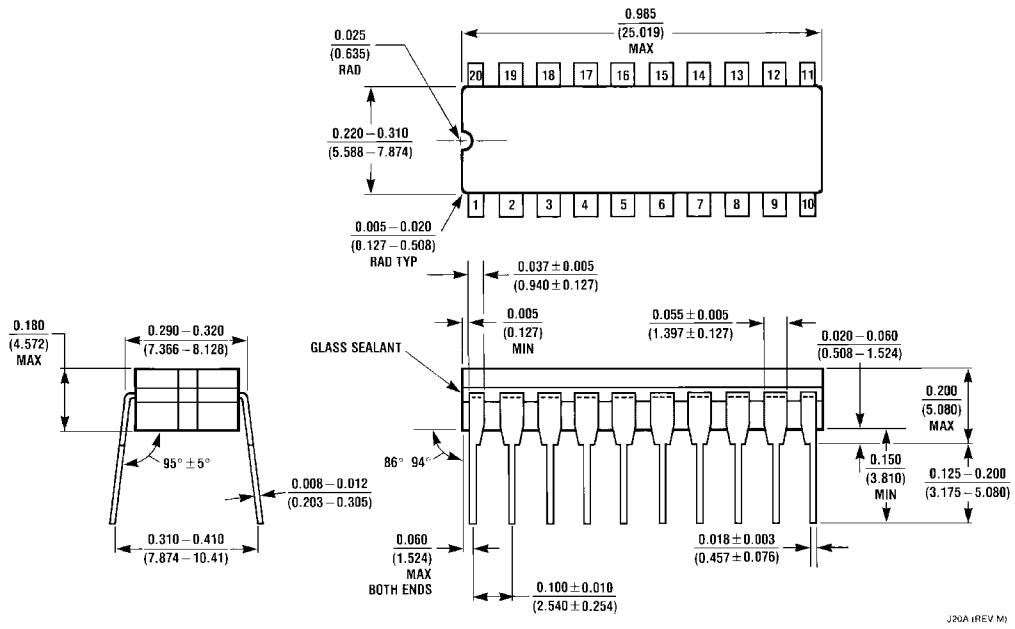
Physical Dimensions inches (millimeters) unless otherwise noted



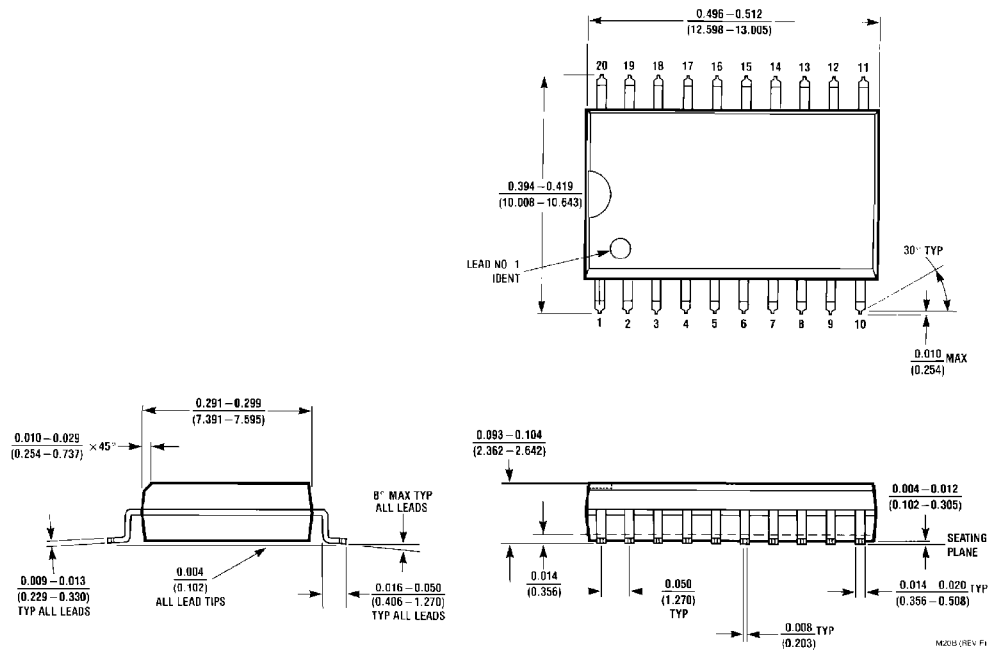
**20-Lead Ceramic Leadless Chip Carrier (L)
Package Number E20A**

EDA (REV. 1)

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

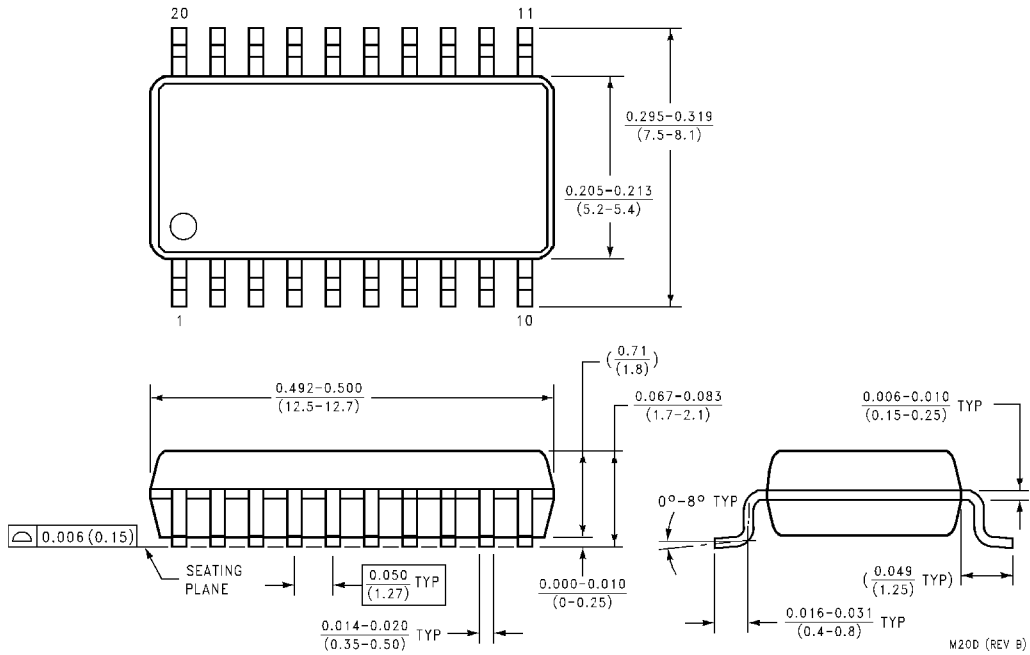


**20-Lead Ceramic Dual-In-Line Package (D)
 Package Number J20A**

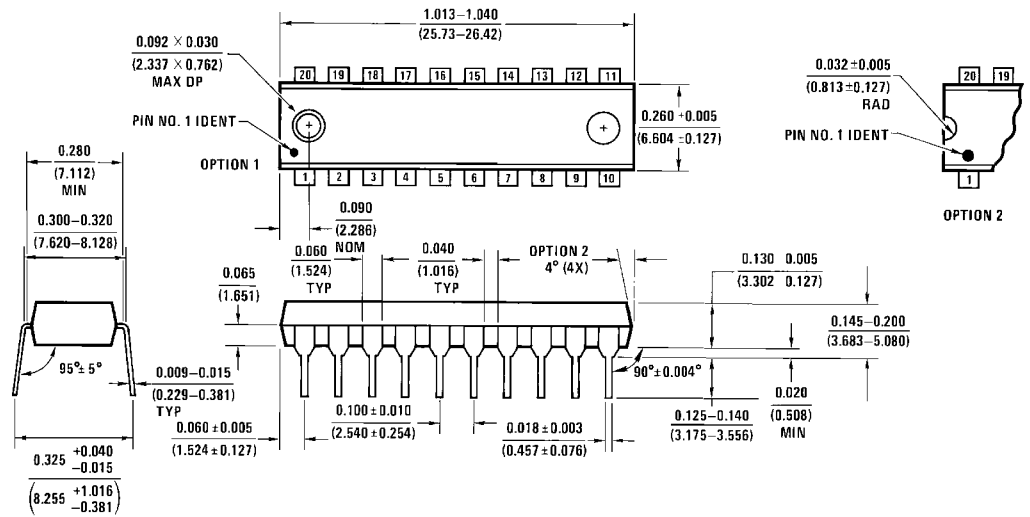


**20-Lead (0.300" Wide) Molded Small Outline Package, JEDEC
 Package Number M20B**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

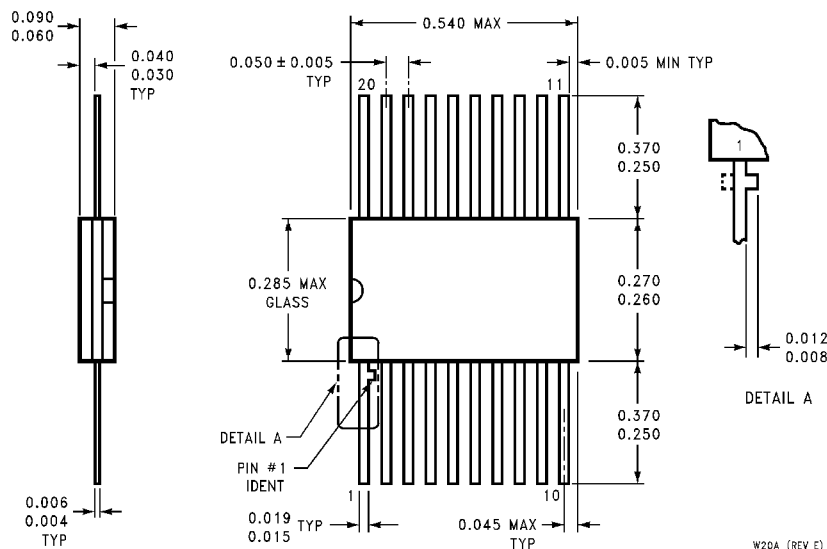


**20-Lead (0.300" Wide) Molded Small Outline Package, EIAJ (SJ)
 Package Number M20D**



**20-Lead (0.300" Wide) Molded Dual-In-Line Package (P)
 Package Number N20A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**20-Lead Ceramic Flatpak (F)
Package Number W20A**

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