CS2844, CS3844, CS2845, CS3845

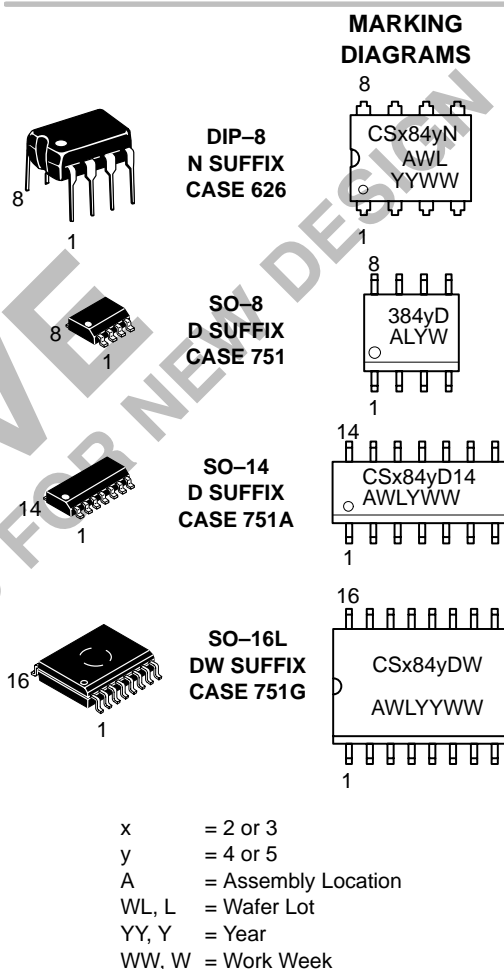# Current Mode PWM Control Circuit with 50% Max Duty Cycle

The CS3844/45 provides all the necessary features to implement off–line fixed frequency current–mode control with a minimum number of external components.

The CS3844 family incorporates a new precision temperature–controlled oscillator to minimize variations in frequency. An internal toggle flip–flop, which blanks the output every other clock cycle, limits the duty–cycle range to less than 50%. An undervoltage lockout ensures that V_{REF} is stabilized before the output stage is enabled. In the CS2844/CS3844 turn on occurs at 16 V and turn off at 10 V. In the CS2845/CS3845 turn on is at 8.4 V and turn off at 7.6 V.

Other features include low start–up current, pulse–by–pulse current limiting, and a high–current totem pole output for driving capacitive loads, such as gate of a power MOSFET. The output is low in the off state, consistent with N–channel devices.

Features

- Optimized for Off–Line Control
- Temp. Compensated Oscillator
- 50% Max Duty–Cycle Clamp
- V_{REF} Stabilized Before Output Stage Is Enabled
- Low Start–Up Current
- Pulse–By–Pulse Current Limiting
- Improved Undervoltage Lockout
- Double Pulse Suppression
- 1.0% Trimmed Bandgap Reference
- High Current Totem Pole Output

ON Semiconductor™

http://onsemi.com

MARKING DIAGRAMS

DIP–8
N SUFFIX
CASE 626

CSx84yN
AWL
YYWW

SO–8
D SUFFIX
CASE 751

384yD
ALYW

SO–14
D SUFFIX
CASE 751A

CSx84yD14
AWLYWW

SO–16L
DW SUFFIX
CASE 751G

CSx84yDW
AWLYYWW

x	= 2 or 3
y	= 4 or 5
A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

Publication Order Number:
CS2844/D

CS2844, CS3844, CS2845, CS3845

PIN CONNECTIONS

DIP–8 & SO–8

```
        1        8
COMP ⊏        ⊐ V_REF
V_FB ⊏        ⊐ V_CC
Sense ⊏       ⊐ V_OUT
OSC ⊏         ⊐ GND
```

SO–14

```
         1          14
COMP ⊏  ○         ⊐ V_REF
 NC ⊏              ⊐ NC
V_FB ⊏            ⊐ V_CC
 NC ⊏             ⊐ V_CC Pwr
Sense ⊏          ⊐ V_OUT
 NC ⊏             ⊐ GND
OSC ⊏            ⊐ Pwr GND
```

SO–16L

```
        1          16
 NC ⊏             ⊐ NC
 NC ⊏             ⊐ V_REF
COMP ⊏           ⊐ V_CC
V_FB ⊏           ⊐ V_CC Pwr
Sense ⊏          ⊐ V_OUT
OSC ⊏            ⊐ GND
 NC ⊏             ⊐ Pwr GND
 NC ⊏             ⊐ NC
```
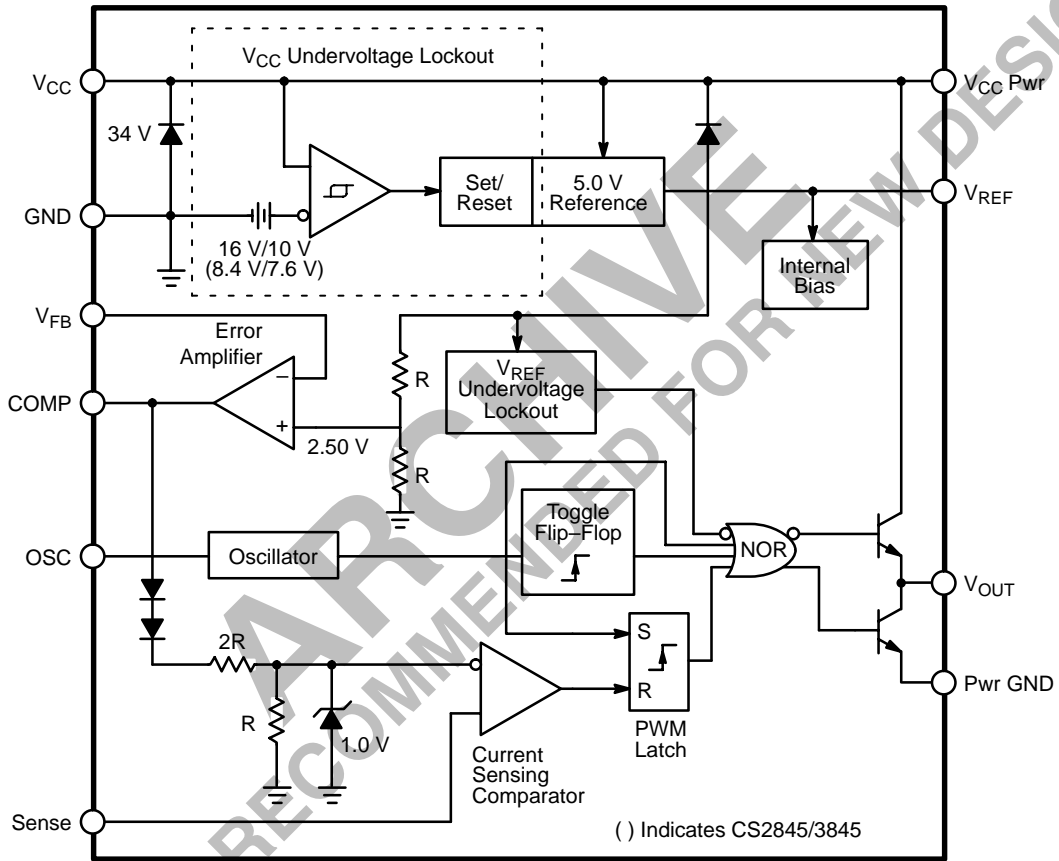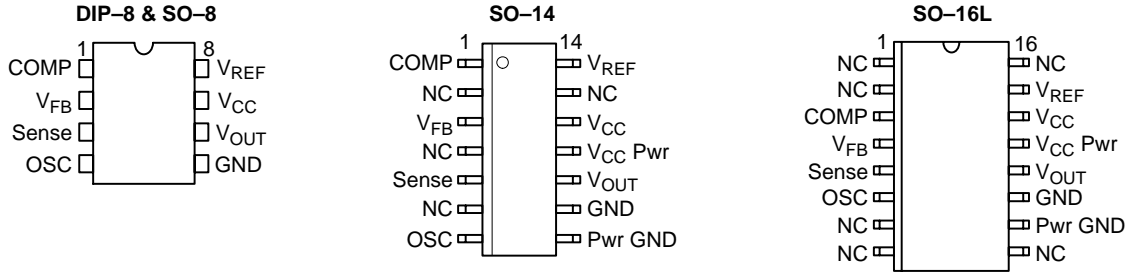

Figure 1. Block Diagram

MAXIMUM RATINGS*

Rating		Value	Unit
Supply Voltage (I_{CC} < 30 mA)		Self Limiting	–
Supply Voltage (Low Impedance Source)		30	V
Output Current		±1.0	A
Output Energy (Capacitive Load)		5.0	μJ
Analog Inputs (V_{FB}, Sense)		–0.3 to + 5.5	V
Error Amp Output Sink Current		10	mA

Package Thermal Resistance, PDIP–8
    Junction–to–Case, $R_{\theta JC}$
    Junction–to–Ambient, $R_{\theta JA}$
		52
		100
			°CW
			°CW

Package Thermal Resistance, SO–8
    Junction–to–Case, $R_{\theta JC}$
    Junction–to–Ambient, $R_{\theta JA}$
		45
		165
			°CW
			°CW

Package Thermal Resistance, SO–14
    Junction–to–Case, $R_{\theta JC}$
    Junction–to–Ambient, $R_{\theta JA}$
		30
		125
			°CW
			°CW

Package Thermal Resistance, SO–16L
    Junction–to–Case, $R_{\theta JC}$
    Junction–to–Ambient, $R_{\theta JA}$
		23
		105
			°CW
			°CW

Lead Temperature Soldering:	Wave Solder (through hole styles only) (Note 1) Reflow (SMD styles only) (Note 2)	260 peak 230 peak	°C °C

1. 10 second maximum.

2. 60 second maximum above 183°C.

*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS (–25° ≤ T_A ≤ 85° for CS2844/2845, 0° ≤ T_A ≤ 70° for CS3844/CS3845. V_{CC} = 15 V*; R_T = 10 kΩ, C_T = 3.3 nF for sawtooth mode; unless otherwise stated.)

Characteristic	Test Conditions	CS2844/CS2845			CS3844/CS3845			Unit
		Min	Typ	Max	Min	Typ	Max	
Reference Section								
Output Voltage	T_J = 25°C, I_{REF} = 1.0 mA	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	12 ≤ V_{CC} ≤ 25 V	–	6.0	20	–	6.0	20	mV
Load Regulation	1.0 ≤ I_{REF} ≤ 20 mA	–	6.0	25	–	6.0	25	mV
Temperature Stability	Note 3.	–	0.2	0.4	–	0.2	0.4	mV/°C
Total Output Variation	Line, Load, Temperature. Note 3.	4.90	–	5.10	4.82	–	5.18	V
Output Noise Voltage	10 Hz ≤ f ≤ 10 kHz, T_J = 25°C. Note 3.	–	50	–	–	50	–	μV
Long Term Stability	T_A = 125°C, 1000 Hrs. Note 3.	–	5.0	25	–	5.0	25	mV
Output Short Circuit	T_A = 25°C	–30	–100	–180	–30	–100	–180	mA
Oscillator Section								
Initial Accuracy	Sawtooth Mode, T_J = 25°C	47	52	57	47	52	57	kHz
Voltage Stability	12 ≤ V_{CC} ≤ 25 V	–	0.2	1.0	–	0.2	1.0	%
Temperature Stability	Sawtooth Mode T_{MIN} ≤ T_A ≤ T_{MAX}. Note 3.	–	5.0	–	–	5.0	–	%
Amplitude	V_{OSC} (peak to peak)	–	1.7	–	–	1.7	–	V

3. These parameters, although guaranteed, are not 100% tested in production.

*Adjust V_{CC} above the start threshold before setting at 15 V.

ELECTRICAL CHARACTERISTICS (continued) ($-25° \leq T_A \leq 85°$ for CS2844/2845, $0° \leq T_A \leq 70°$ for CS3844/CS3845. $V_{CC} = 15$ V*; $R_T = 10$ kΩ, $C_T = 3.3$ nF for sawtooth mode; unless otherwise stated.)

Characteristic	Test Conditions	CS2842A/CS2843A Min	Typ	Max	CS3842A/CS3843A Min	Typ	Max	Unit
Error Amp Section								
Input Voltage	$V_{COMP} = 2.5$ V	2.45	2.50	2.55	2.42	2.50	2.58	V
Input Bias Current	$V_{FB} = 0$	–	–0.3	–1.0	–	–0.3	–2.0	μA
A_{VOL}	$2.0 \leq V_{OUT} \leq 4.0$ V	65	90	–	65	90	–	dB
Unity Gain Bandwidth	Note 4.	0.7	1.0	–	0.7	1.0	–	MHz
PSRR	$12 \leq V_{CC} \leq 25$ V	60	70	–	60	70	–	dB
Output Sink Current	$V_{FB} = 2.7$ V, $V_{COMP} = 1.1$ V	2.0	6.0	–	2.0	6.0	–	mA
Output Source Current	$V_{FB} = 2.3$ V, $V_{COMP} = 5.0$ V	–0.5	–0.8	–	–0.5	–0.8	–	mA
V_{OUT} High	$V_{FB} = 2.3$ V, $R_L = 15$ kΩ to GND	5.0	6.0	–	5.0	6.0	–	V
V_{OUT} Low	$V_{FB} = 2.7$ V, $R_L = 15$ kΩ to V_{REF}	–	0.7	1.1	–	0.7	1.1	V
Current Sense Section								
Gain	Notes 5 & 6.	2.85	3.00	3.15	2.85	3.00	3.15	V/V
Maximum Input Signal	$V_{COMP} = 5.0$ V. Note 5.	0.9	1.0	1.1	0.9	1.0	1.1	V
PSRR	$12 \leq V_{CC} \leq 25$ V. Note 5.	–	70	–	–	70	–	dB
Input Bias Current	$V_{SENSE} = 0$	–	–2.0	–10	–	–2.0	–10	μA
Delay to Output	$T_J = 25°C$. Note 4.	–	150	300	–	150	300	ns
Output Section								
Output Low Level	$I_{SINK} = 20$ mA $I_{SINK} = 200$ mA	– –	0.1 1.5	0.4 2.2	– –	0.1 1.5	0.4 2.2	V V
Output High Level	$I_{SOURCE} = 20$ mA $I_{SOURCE} = 200$ mA	13 12	13.5 13.5	– –	13 12	13.5 13.5	– –	V V
Rise Time	$T_J = 25°C$, $C_L = 1.0$ nF. Note 4.	–	50	150	–	50	150	ns
Fall Time	$T_J = 25°C$, $C_L = 1.0$ nF. Note 4.	–	50	150	–	50	150	ns
Total Standby Current								
Startup Current	–	–	0.5	1.0	–	0.5	1.0	mA
Operating Supply Current	$V_{FB} = V_{SENSE} = 0$ V, $R_T = 10$ kΩ, $C_T = 3.3$ nF	–	11	17	–	11	17	mA
V_{CC} Zener Voltage	$I_{CC} = 25$ mA	–	34	–	–	34	–	V
PWM Section								
Maximum Duty Cycle	–	46	48	50	46	48	50	%
Minimum Duty Cycle	–	–	–	0	–	–	0	%

4. These parameters, although guaranteed, are not 100% tested in production.

5. Parameters measured at trip point of latch with $V_{FB} = 0$.

6. Gain defined as: $A = \Delta V_{COMP}/\Delta V_{SENSE}$; $0 \leq V_{SENSE} \leq 0.8$ V.

*Adjust V_{CC} above the start threshold before setting at 15 V.

ELECTRICAL CHARACTERISTICS (continued) ($-25° \leq T_A \leq 85°$ for CS2844/2845, $0° \leq T_A \leq 70°$ for CS3844/CS3845.
V_{CC} = 15 V*; R_T = 10 kΩ, C_T = 3.3 nF for sawtooth mode; unless otherwise stated.)

Characteristic	Test Conditions	CS2844			CS3844			CS2845/CS3845			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Undervoltage Lockout Section											
Start Threshold	–	15	16	17	14.5	16	17.5	7.8	8.4	9.0	V
Min. Operating Voltage	After Turn On	9.0	10	11	8.5	10	11.5	7.0	7.6	8.2	V

*Adjust V_{CC} above the start threshold before setting at 15 V.

PACKAGE PIN DESCRIPTION

Package Pin Number					
DIP–8 & SO–8	SO–14	Symbol	Symbol	Description	
1	1	3	COMP	Error amp output, used to compensate error amplifier.	
2	3	4	V_{FB}	Error amp inverting input.	
3	5	5	Sense	Noninverting input to Current Sense Comparator.	
4	7	6	OSC	Oscillator timing network with capacitor to ground, resistor to V_{REF}.	
5	9	11	GND	Ground.	
–	8	10	Pwr GND	Output driver ground.	
6	10	12	V_{OUT}	Output drive pin.	
–	11	13	V_{CC} Pwr	Output driver positive supply.	
7	12	14	V_{CC}	Positive power supply.	
8	14	15	V_{REF}	Output of 5.0 V internal reference.	
–	2, 4, 6, 13	1, 2, 7, 8, 9, 16	NC	No connection.	
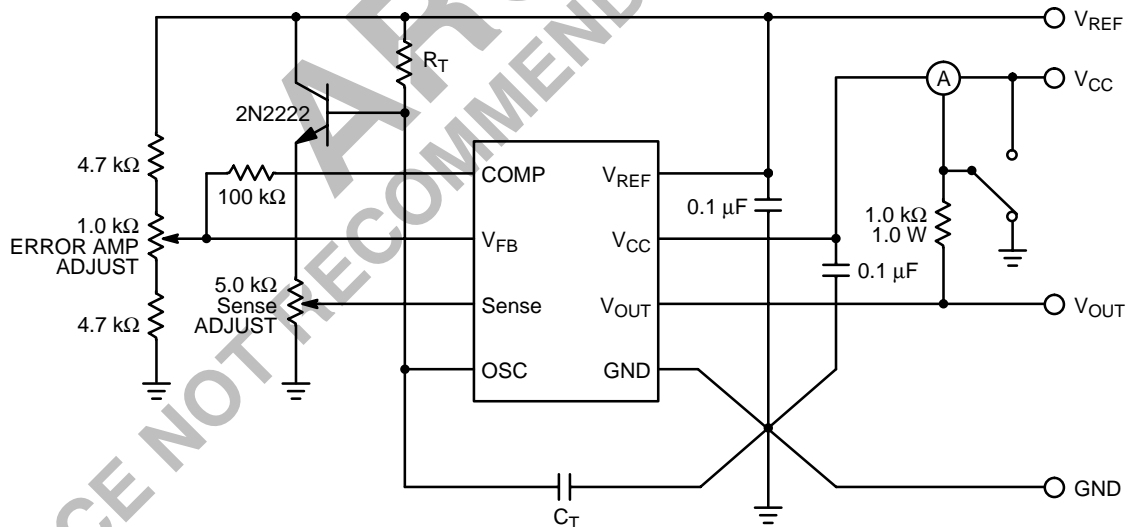
Figure 2. Test Circuit Open Loop Laboratory Test Fixture

CIRCUIT DESCRIPTION

	CSX844	CSX845
V_{ON}	16 V	8.4 V
V_{OFF}	10 V	7.6 V
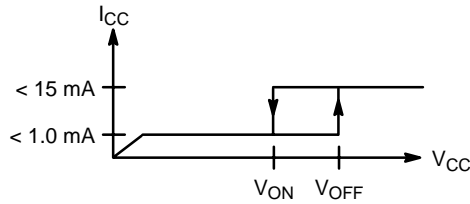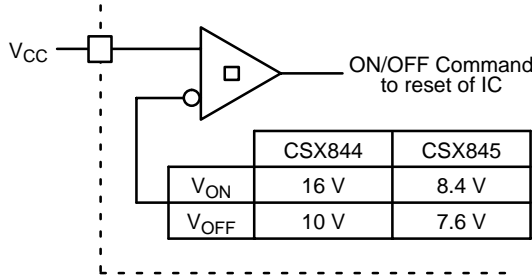
Figure 3. Startup Voltage for CSX844 and CSX845

Undervoltage Lockout

During Undervoltage Lockout (Figure 3), the output driver is biased to sink minor amounts of current. The output should be shunted to ground with a resistor to prevent activating the power switch with extraneous leakage currents.

PWM Waveform

To generate the PWM waveform, the control voltage from the error amplifier is compared to a current sense signal which represents the peak output inductor current (Figure 4). An increase in V_{CC} causes the inductor current slope to increase, thus reducing the duty cycle. This is an inherent feed–forward characteristic of current mode control, since the control voltage does not have to change during changes of input supply voltage.
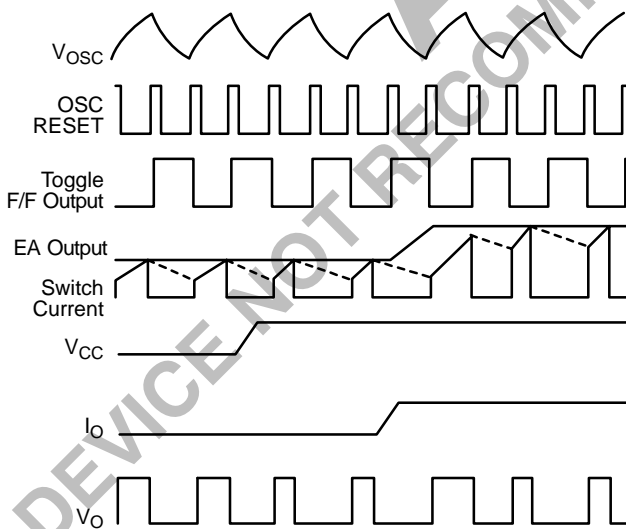
Figure 4. Timing Diagram

$$t_{on} = t_c$$
$$t_{off} = t_c + 2t_d$$
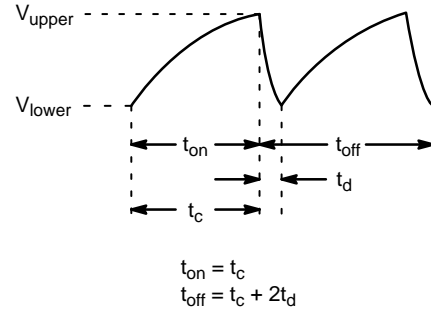
Figure 5. Duty Cycle Parameters

When the power supply sees a sudden large output current increase, the control voltage will increase allowing the duty cycle to momentarily increase. Since the duty cycle tends to exceed the maximum allowed to prevent transformer saturation in some power supplies, the internal oscillator waveform provides the maximum duty cycle clamp as programmed by the selection of OSC components.

Setting the Oscillator

The times t_c and t_d can be determined as follows:

$$t_c = R_T C_T \ln\left(\frac{V_{REF} - V_{lower}}{V_{REF} - V_{upper}}\right)$$

$$t_d = R_T C_T \ln\left(\frac{V_{REF} - I_d R_T - V_{lower}}{V_{REF} - I_d R_T - V_{upper}}\right)$$

Substituting in typical values for the parameters in the above formulas:

V_{REF} = 5.0 V, V_{upper} = 2.7 V, V_{lower} = 1.0 V, I_d = 8.3 mA then:

$$t_c \approx 0.5534 R_T C_T$$

$$t_d = R_T C_T \ln\left(\frac{2.3 - 0.0083 R_T}{4.0 - 0.0083 R_T}\right)$$

For better accuracy R_T should be $\geq$ 10 kΩ.

Grounding

High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to Gnd in a single point ground.

The transistor and 5.0 kΩ potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to Sense.

CS2844, CS3844, CS2845, CS3845

ORDERING INFORMATION

Device	Temperature Range	Package	Shipping
CS2844LN8	−25°C to 85°C	DIP–8	50 Units/Rail
CS2844LD14		SO–14	55 Units/Rail
CS2844LDR14		SO–14	2500 Tape & Reel
CS2844LDW16		SO–16L	48 Units/Rail
CS2844LDWR16		SO–16L	2500 Tape & Reel
CS2845LN8		DIP–8	50 Units/Rail
CS2845LDW16		SO–16L	48 Units/Rail
CS2845LDWR16		SO–16L	2500 Tape & Reel
CS3844GN8	0°C to 70°C	DIP–8	50 Units/Rail
CS3844GD8		SO–8	98 Units/Rail
CS3844GDR8		SO–8	2500 Tape & Reel
CS3844GD14		SO–14	55 Units/Rail
CS3844GDR14		SO–14	2500 Tape & Reel
CS3844GDW16		SO–16	48 Units/Rail
CS3844GDWR16		SO–16	2500 Tape & Reel
CS3845GN8		DIP–8	50 Units/Rail
CS3845GD8		SO–8	98 Units/Rail
CS3845GDR8		SO–8	2500 Tape & Reel
CS3845GD14		SO–14	55 Units/Rail
CS3845GDR14		SO–14	2500 Tape & Reel
CS3845GDW16		SO–16L	48 Units/Rail
CS3845GDWR16		SO–16L	2500 Tape & Reel

PACKAGE DIMENSIONS

DIP–8
N SUFFIX
CASE 626–05
ISSUE L

NOTE 2
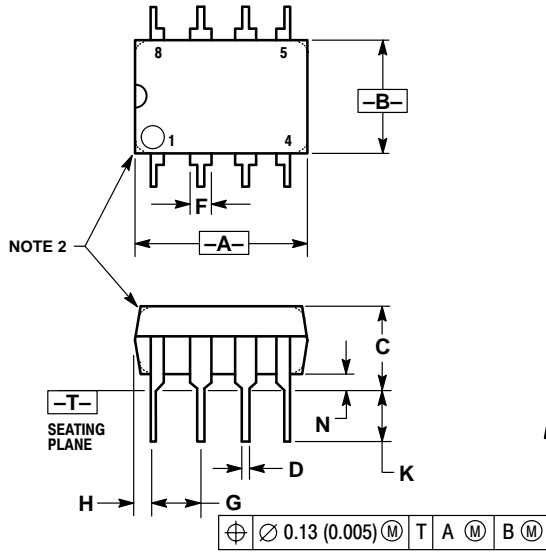
NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	---	10°	---	10°
N	0.76	1.01	0.030	0.040

SEATING PLANE

⊕ | ⌀ 0.13 (0.005) Ⓜ | T | A Ⓜ | B Ⓜ

SO–8
D SUFFIX
CASE 751–07
ISSUE W
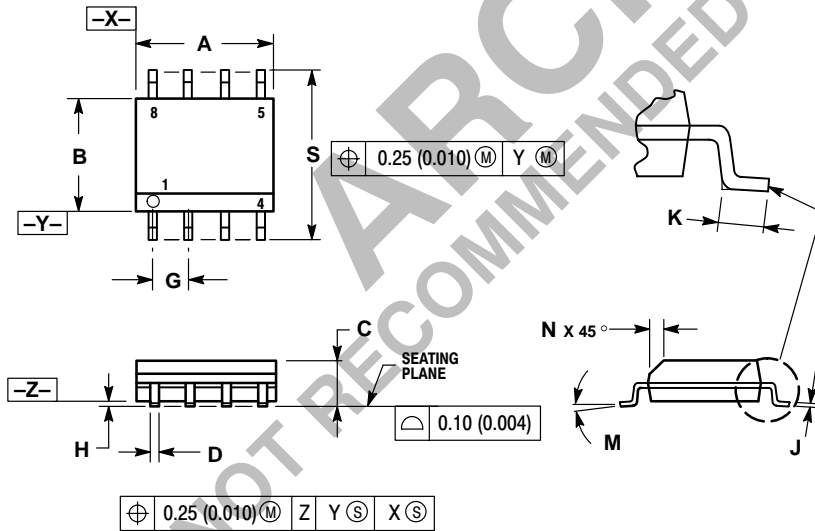
0.25 (0.010) Ⓜ | Y Ⓜ

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

SEATING PLANE

⌓ 0.10 (0.004)

N X 45°

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

⊕ | 0.25 (0.010) Ⓜ | Z | Y Ⓢ | X Ⓢ

CS2844, CS3844, CS2845, CS3845

PACKAGE DIMENSIONS

SO–14
D SUFFIX
CASE 751A–03
ISSUE F
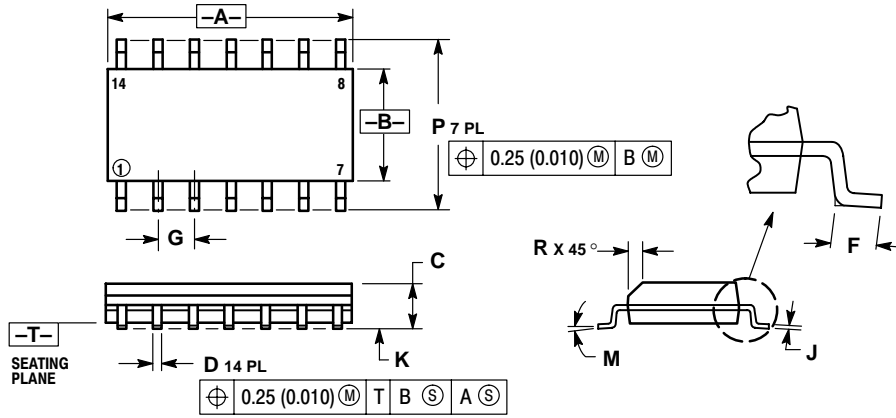
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

SO–16L
DW SUFFIX
CASE 751G–03
ISSUE B
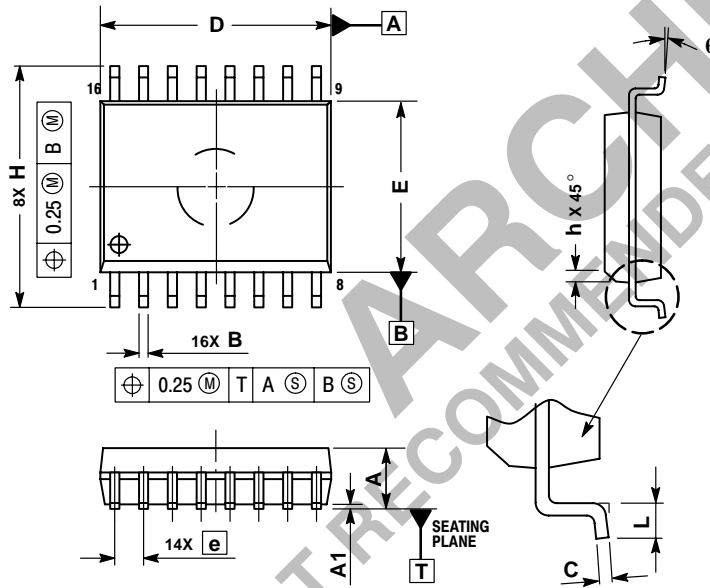
NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INLCUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0 °	7 °

Notes

Notes

CS2844, CS3844, CS2845, CS3845

PUBLICATION ORDERING INFORMATION