MIC2584

Dual-Channel Hot Swap Controller/Sequencer

Features

- 1.0V to 13.2V Supply Voltage Operation
- Surge Voltage Protection Up to 20V
- Current Regulation Limits Inrush Current Regardless of Load Capacitance
- Programmable Inrush Current Limiting
- Electronic Circuit Breaker
- Dual Level Overcurrent Fault Sensing Eliminates False Tripping
- Fast Response to Short Circuit Conditions (<1 µs)
- Undervoltage Output Monitoring
- Undervoltage Lockout Protection
- FAULT Status Output
- Power On Reset Output

Applications

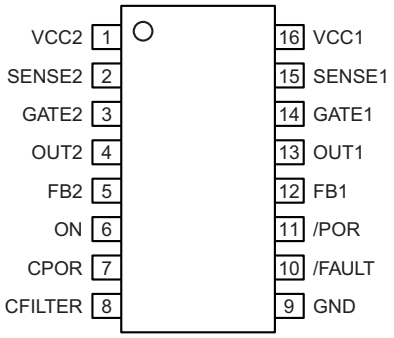
- RAID Systems
- Network Servers
- Base Stations
- Network Switches
- Hot Board Insertion

General Description

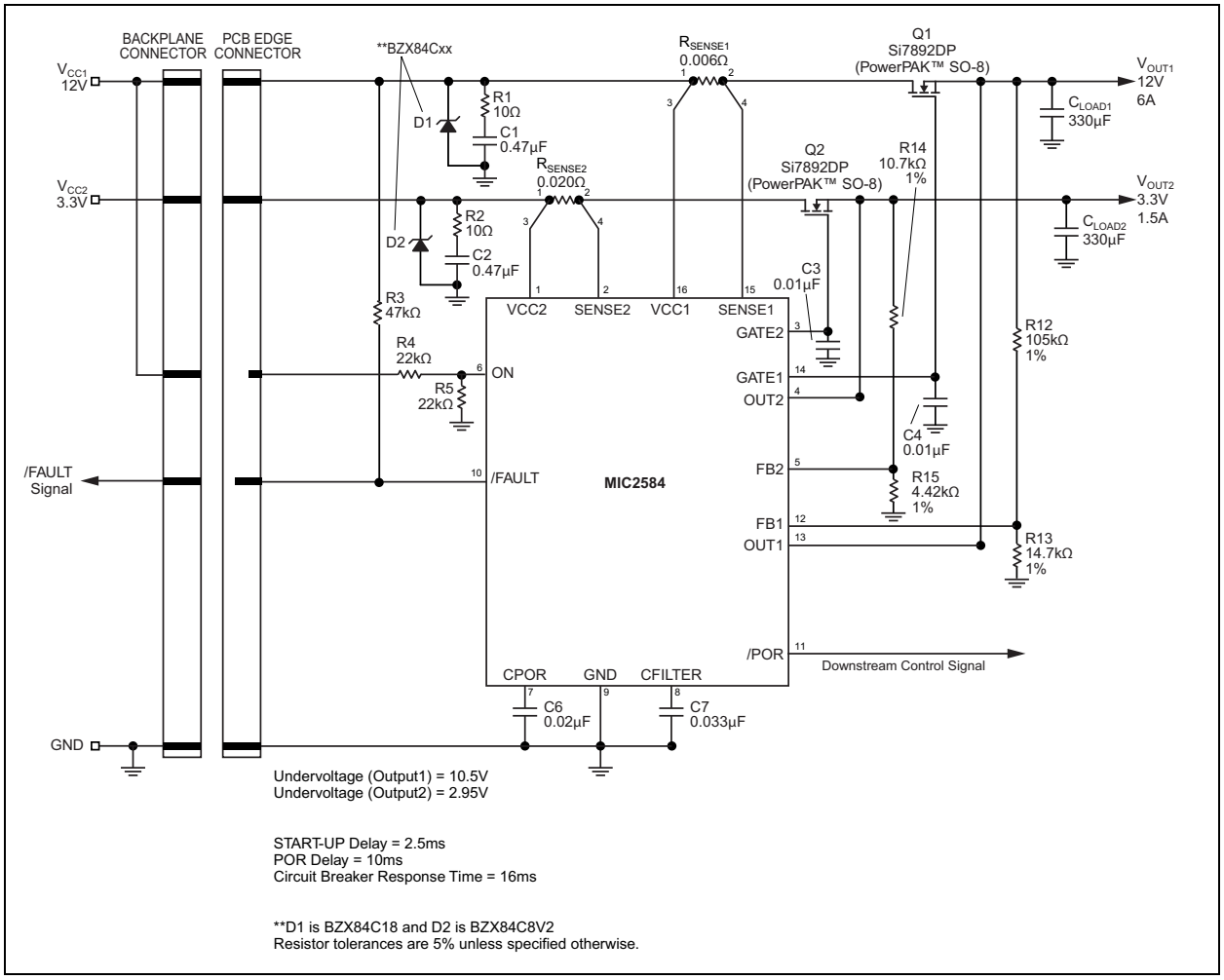
The MIC2584 is a dual-channel positive voltage hot swap controller designed to facilitate the safe insertion of boards into live system backplanes. The MIC2584 is available in a 16-lead TSSOP package. Using a few external discrete components and by controlling the gate drives of external N-Channel MOSFET devices, the MIC2584 provides inrush current limiting and output voltage slew rate control in harsh, critical power supply environments. In combination, the device's many features provide a simplified, robust solution for many network applications meeting protection requirements of multiple voltage logic systems.

Package Type

MIC2584
16-Pin TSSOP (TS)
(Top View)



Typical Application Circuit

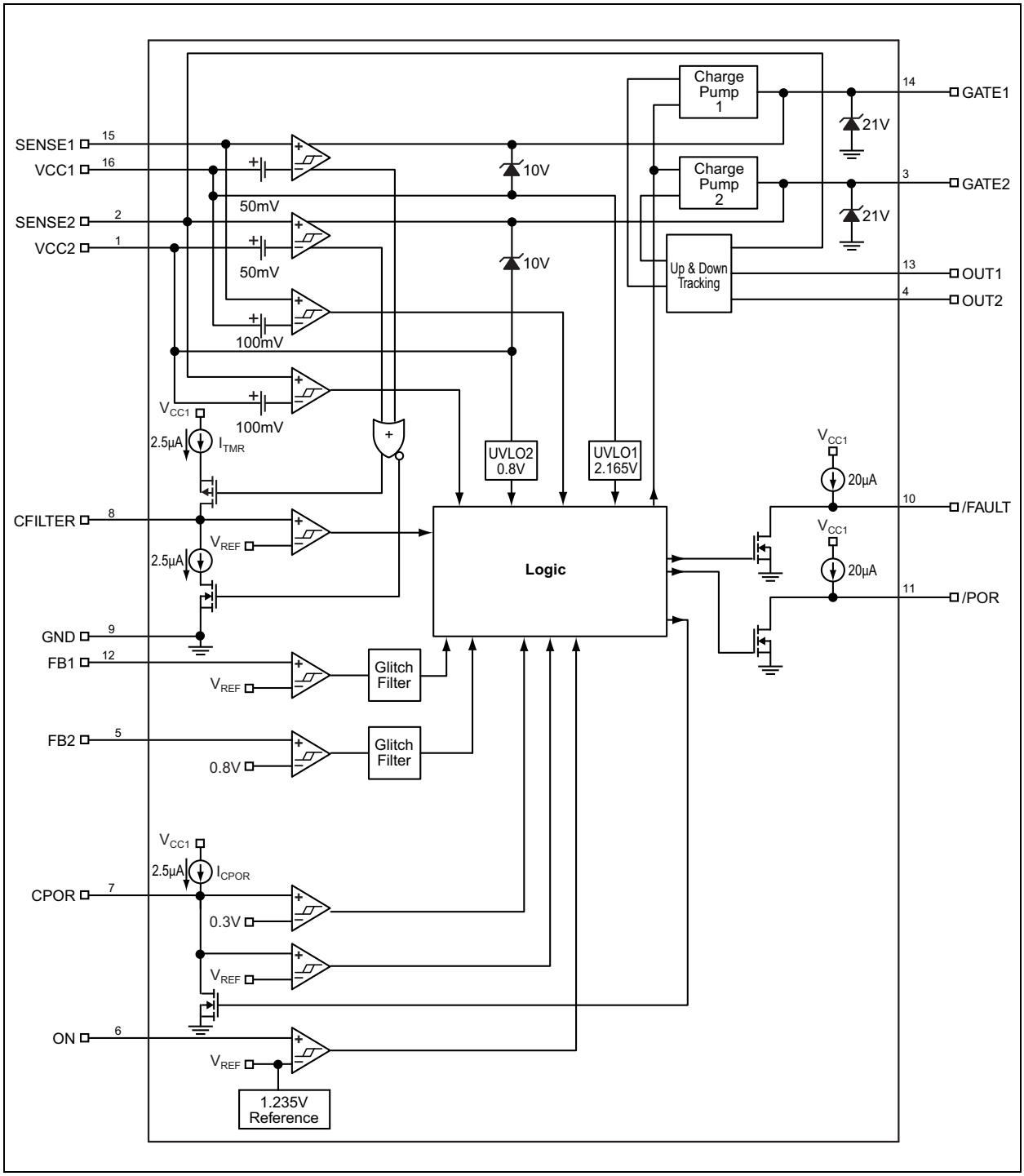


Undervoltage (Output1) = 10.5V
Undervoltage (Output2) = 2.95V

START-UP Delay = 2.5ms
POR Delay = 10ms
Circuit Breaker Response Time = 16ms

**D1 is BZX84C18 and D2 is BZX84C8V2
Resistor tolerances are 5% unless specified otherwise.

Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{CC1}/V_{CC2}) ..... –0.3V to +20V
SENSE1/SENSE2 Pins ..... –0.3V to $V_{CC1/2}$
ON, OUT1, OUT2, /POR, /FAULT Pins ..... –0.3V to +15V
GATE1/GATE2 Pin ..... –0.3V to +25V
All Other Input Pins ..... –0.3V to +15V
ESD Rating (Note 1)
Human Body Model 1500V
Machine Model 100V

Operating Ratings ‡

Supply Voltage (V_{CC1}) ..... +2.3V to +13.2V
Supply Voltage (V_{CC2}) ..... +1.0V to +13.2V

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability. Specifications are for packaged product only.

‡ Notice: The device is not guaranteed to function outside its operating ratings.

Note 1: Devices are ESD sensitive. Handling precautions are recommended.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: 2.3V ≤ V_{CC1} ≤ 13.2V, 1.0V ≤ V_{CC2} ≤ 13.2V, T_A = +25°C unless otherwise noted. **Bold** values indicate –40°C ≤ T_A ≤ +85°C. (Note 1)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Supply Voltage	V_{CC1}	2.3	—	13.2	V	—
Supply Current	I_{CC1}	—	1.7	**3**	mA	—
Supply Voltage	V_{CC2}	1.0	—	13.2	V	$V_{CC2} \le V_{CC1}$
Supply Current	I_{CC2}	—	0.05	**0.15**	mA	—
V_{CC1} Undervoltage Lockout Threshold	V_{UV1}	**2.050**	2.165	**2.275**	V	—
V_{CC1} Undervoltage Lockout Hysteresis	V_{UV1HYS}	—	200	—	mV	—
V_{CC2} Undervoltage Lockout Threshold	V_{UV2}	**0.7**	0.8	**0.9**	V	—
V_{CC2} Undervoltage Lockout Hysteresis	V_{UV2HYS}	—	30	—	mV	—
Slow Trip Overcurrent Threshold	$V_{TRIPSLOW}$	**42.5**	50	**57.5**	mV	$V_{CCx} - V_{SENSEx}$, $V_{CC1} = V_{CC2}$ = 5V
Slow Trip Overcurrent Hysteresis	$V_{TRIPHYS}$	—	2.5	—	mV	—
Fast Trip Overcurrent Threshold	$V_{TRIPFAST}$	**90**	100	**110**	mV	$V_{CC1} = V_{CC2}$ = 5V, J option
		—	150	—	mV	$V_{CC1} = V_{CC2}$ = 5V, K option
		—	200	—	mV	$V_{CC1} = V_{CC2}$ = 5V, L option
External Gate Drive (GATE1 and GATE2)	V_{GATE}	**6**	8	**10**	V	$V_{GATEx} - V_{CCx}$ (V_{CC1} or V_{CC2} > 5V)
		3.5	4.5	**8**	V	$V_{GATEx} - V_{CCx}$ (V_{CC1} or V_{CC2} < 5V)

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: 2.3V ≤ V_{CC1} ≤ 13.2V, 1.0V ≤ V_{CC2} ≤ 13.2V, T_A = +25°C unless otherwise noted. **Bold** values indicate –40°C ≤ T_A ≤ +85°C. (Note 1)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
GATE Pin Pull-Up Current	I_{GATE}	–25	–14	–8	µA	Start cycle
GATE Pin Sink Current	$I_{GATEOFF}$	—	50	—	mA	/FAULT asserted
		30	45	**70**	µA	Turn off (ON deasserted)
Overcurrent Timer Pin Charge Current	I_{TMR}	**–3.5**	–2.5	**–1.5**	µA	$V_{CCx} – V_{SENSEx}$ = 50 mV
		1.5	2.5	**3.5**	µA	$V_{CCx} – V_{SENSEx}$ = 25 mV
Overcurrent Timer Pin Threshold	V_{TMR}	**1.190**	1.235	**1.290**	V	—
Power-on Reset Current	I_{CPOR}	**–3.5**	–2.5	**–1.5**	µA	V_{CC1} = 5V, C_{POR} = 0.5V Charge Current
		—	2.5	—		V_{CC1} = 5V, C_{POR} = 0.5V Sink Current
Power-on Reset Delay Threshold	V_{POR}	**1.190**	1.235	**1.290**	V	Start-up cycle
Power-On Reset Delay Threshold Hysteresis	V_{PORHYS}	—	25	—	mV	—
Start-Up Threshold	V_{START}	**0.25**	0.30	**0.35**	V	Start-up cycle
FB1 Threshold	V_{FB1}	1.190	1.235	**1.290**	V	—
FB1 Threshold Hysteresis	V_{FB1HYS}	—	25	—	mV	—
FB2 Threshold	V_{FB2}	**0.75**	0.80	**0.85**	V	—
FB2 Threshold Hysteresis	V_{FB2HYS}	—	25	—	mV	—
ON Pin Input Threshold	V_{ON}	**1.190**	1.235	**1.290**	V	—
ON Pin Hysteresis	V_{ONHYS}	—	25	—	mV	—
ON Pin Input Current	I_{ON}	—	0.1	**0.5**	µA	V_{ON} = V_{CCx}
/FAULT, /POR Output Low Voltage	V_{OL}	—	—	**0.4**	V	I_{OUT} = 1.6 mA, V_{CC1} = 5V
/FAULT, /POR Active Output Pull-Up Current	I_{PULLUP}	**7**	12	**22**	µA	ON asserted, V_{FB1} > 1.25V, V_{FB2} > 0.8V, /POR = V_{CC1} – 1V
GATE1 and GATE2 ON/OFF Voltage Window	$V_{GATEWIN}$	—	100	**250**	mV	See Timing Diagrams, (Figure 1-2)
AC Parameters						
Fast Overcurrent Sense to GATE Low Trip Time	t_{OCFAST}	—	1	—	µs	$V_{CCx} – V_{SENSEx}$ = 100 mV, C_{GATE} = 10 nF, See Timing Diagrams, (Figure 1-3)
Slow Overcurrent Sense to GATE Low Trip Time	t_{OCSLOW}	—	20	—	µs	$V_{CCx} – V_{SENSEx}$ = 50 mV, C_{FILTER} = 0

Note 1: Specification for packaged product only.

TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Maximum Junction Temperature	T_J	—	—	125	°C	Internally Limited
Operating Temperature Range	T_A	–40	—	+85	°C	—
Package Thermal Resistances						
Thermal Resistance 16-Lead TSSOP	θ_{JA}	—	99.1	—	°C/W	—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}).

Test Circuit

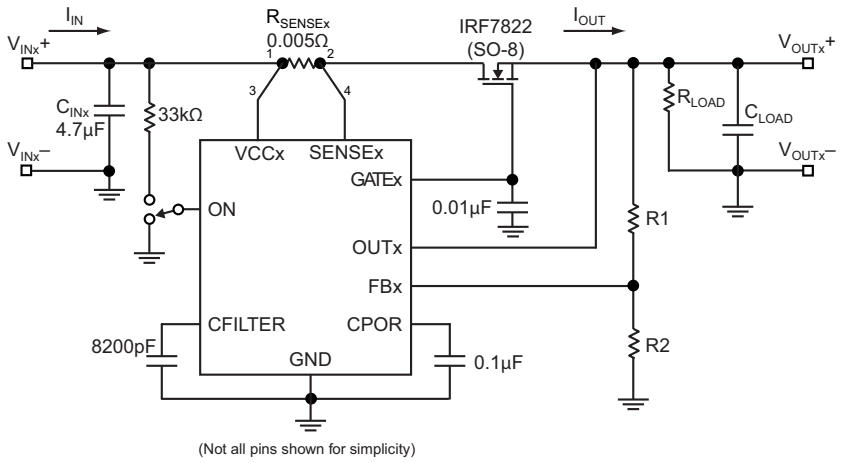


FIGURE 1-1: *MIC2584 Test Circuit.*

Timing Diagrams

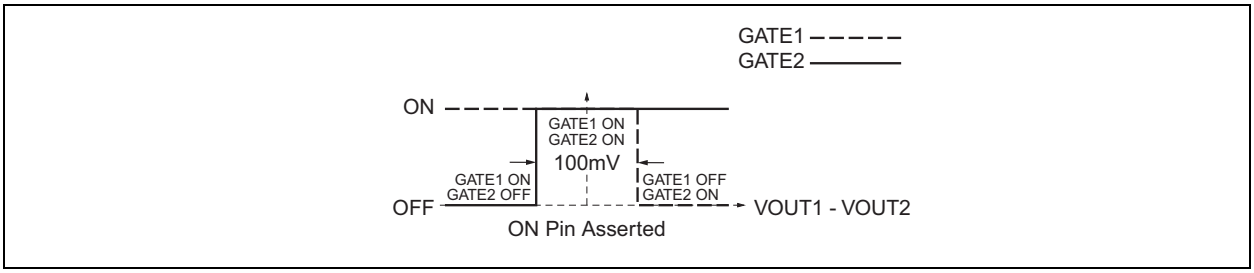


FIGURE 1-2: *Gate Voltage Window.*

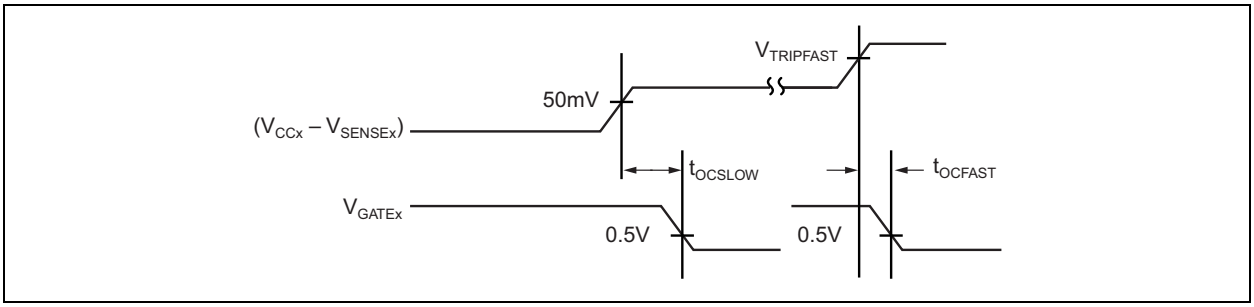


FIGURE 1-3: *Current Limit Response.*

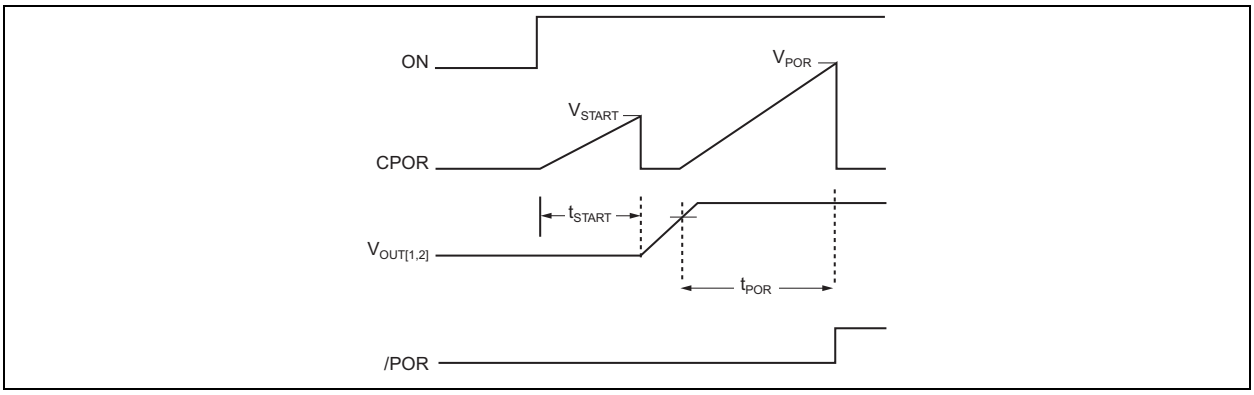


FIGURE 1-4: *Start-Up Cycle Timing.*

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

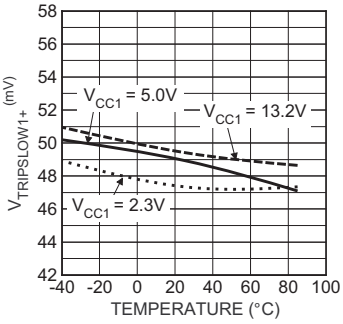


FIGURE 2-1: *$V_{TRIPSLOW1+}$ vs. Temperature.*

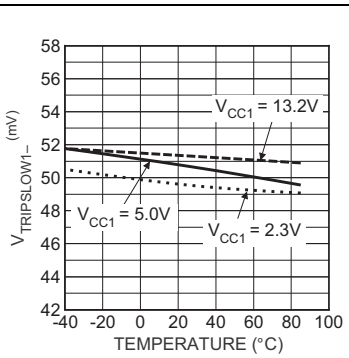


FIGURE 2-2: *$V_{TRIPSLOW1-}$ vs. Temperature.*

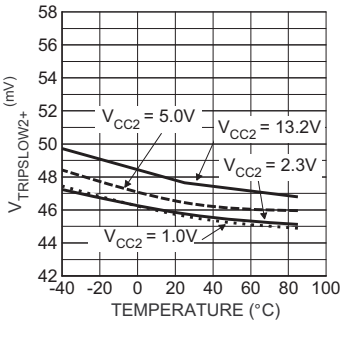


FIGURE 2-3: *$V_{TRIPSLOW2+}$ vs. Temperature.*

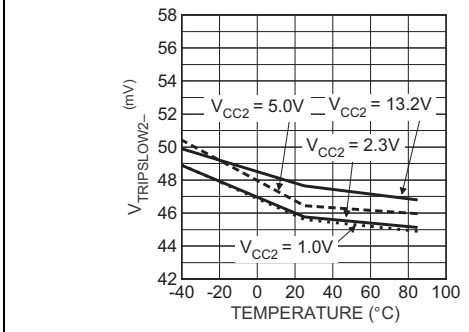


FIGURE 2-4: *$V_{TRIPSLOW2-}$ vs. Temperature.*

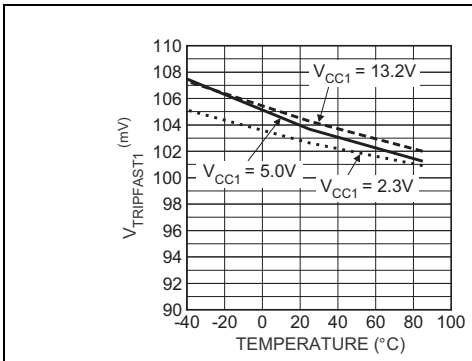


FIGURE 2-5: *$V_{TRIPFAST1}$ vs. Temperature.*

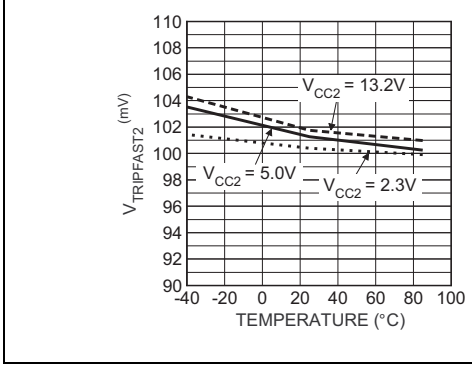


FIGURE 2-6: *$V_{TRIPFAST2}$ vs. Temperature.*

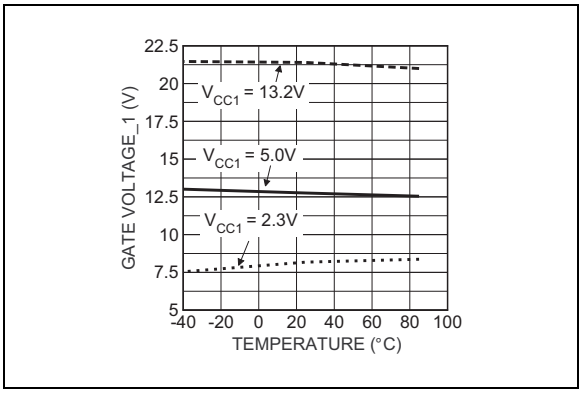


FIGURE 2-7: *V_{GATE1} vs. Temperature.*

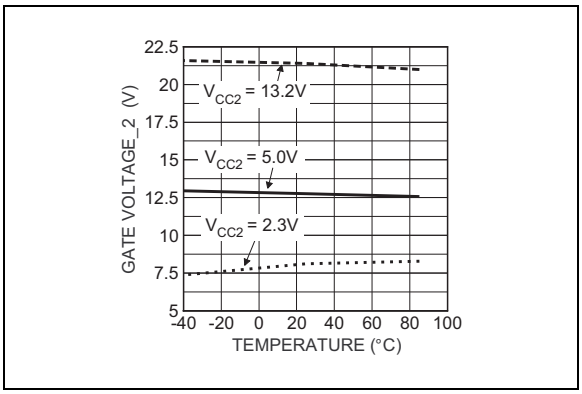


FIGURE 2-8: *V_{GATE2} vs. Temperature.*

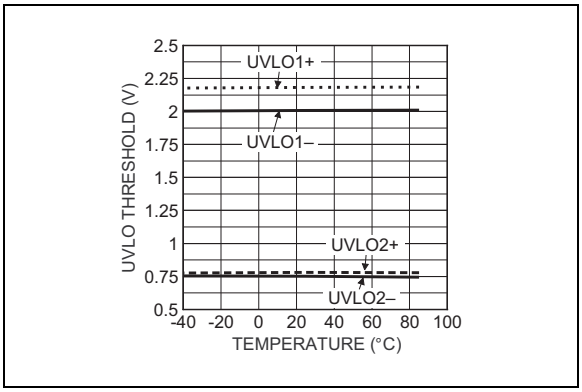


FIGURE 2-9: *UVLO1 and UVLO2 vs. Temperature.*

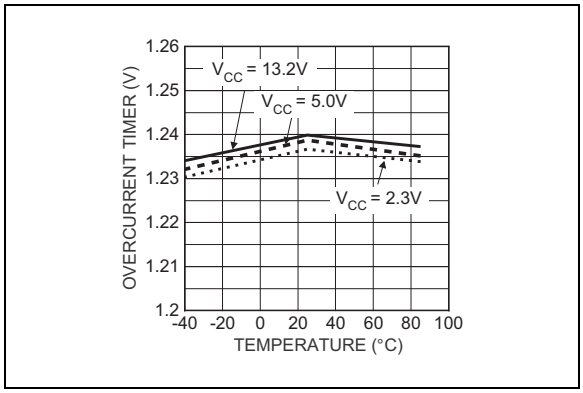


FIGURE 2-10: *Overcurrent Timer Threshold vs. Temperature.*

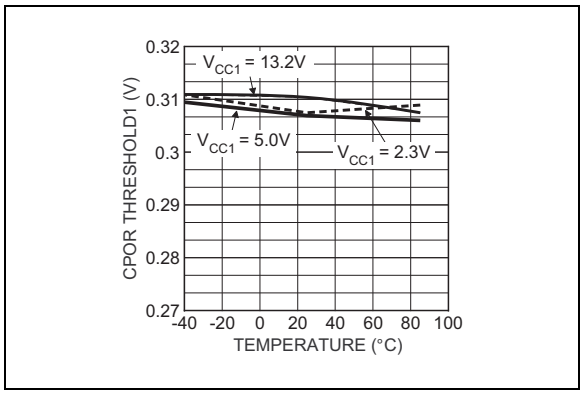


FIGURE 2-11: *CPOR Threshold1 (Start-Up) vs. Temperature.*

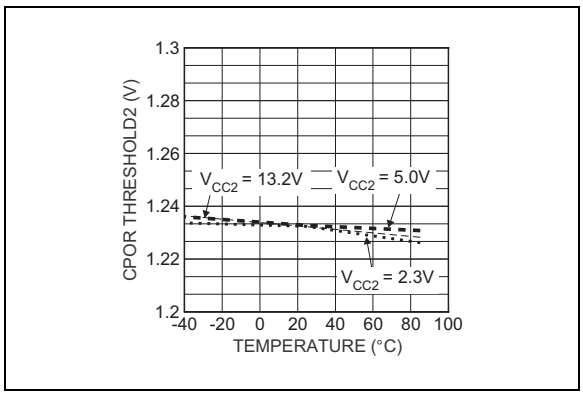


FIGURE 2-12: *CPOR Threshold2 vs. Temperature.*

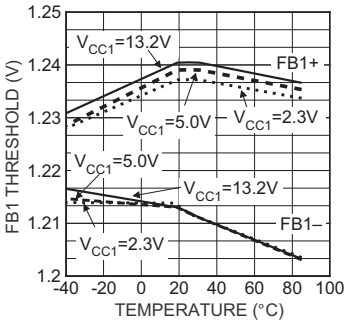


FIGURE 2-13: *FB1 Threshold vs. Temperature.*

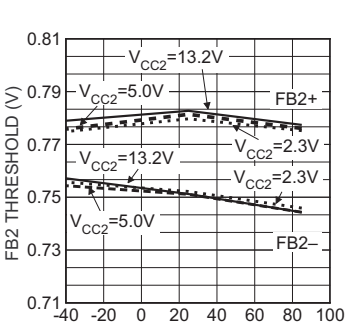


FIGURE 2-14: *FB2 Threshold vs. Temperature.*

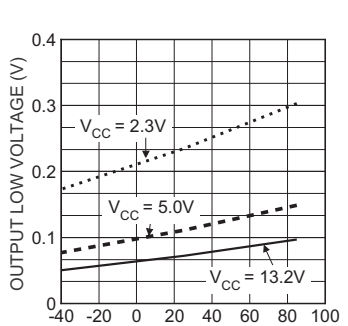


FIGURE 2-15: *Output Low Voltage vs. Temperature.*

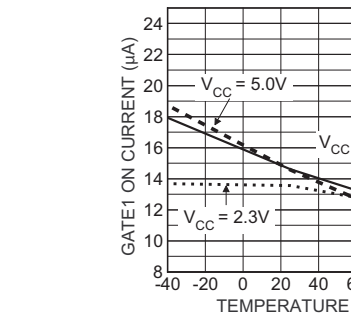


FIGURE 2-16: *GATE1 On Current vs. Temperature.*

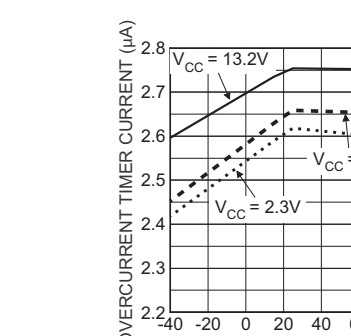


FIGURE 2-17: *Overcurrent Timer Discharge Current vs. Temperature.*

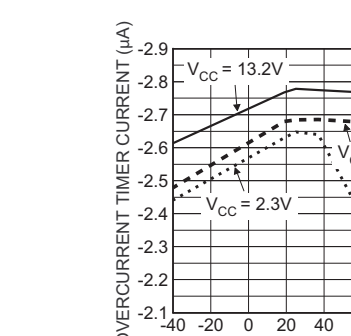


FIGURE 2-18: *Overcurrent Timer Charge Current vs. Temperature.*

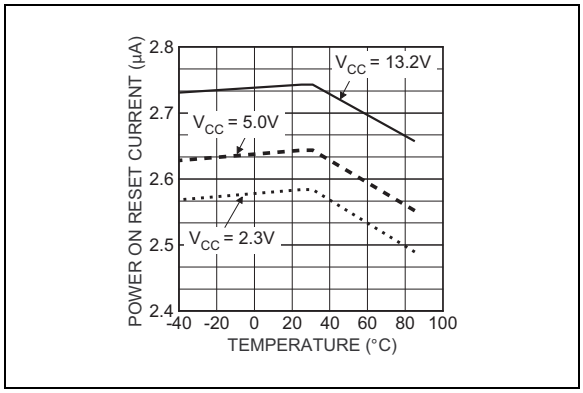


FIGURE 2-19: *Power On Reset Current vs. Temperature.*

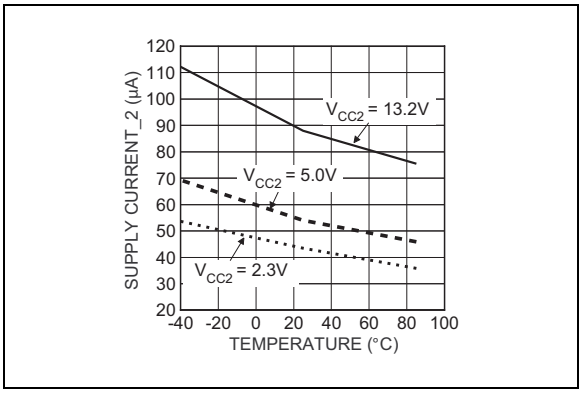


FIGURE 2-22: *Supply Current_2 vs. Temperature.*

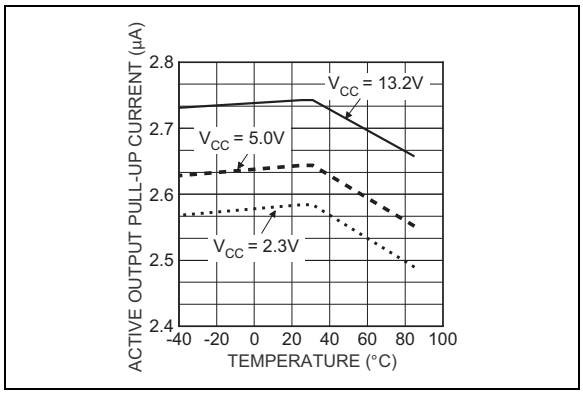


FIGURE 2-20: *Active Output Pull-Up Current vs. Temperature.*

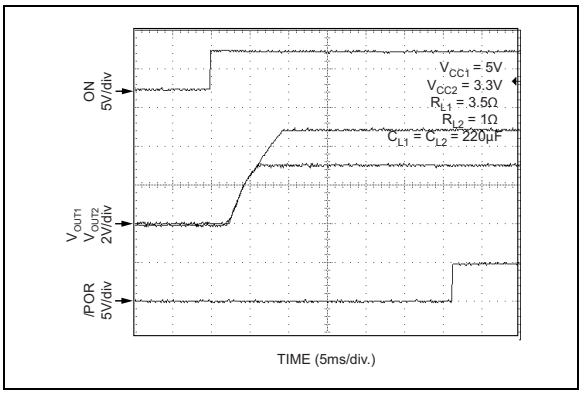


FIGURE 2-23: *Turn-On (No Delay).*

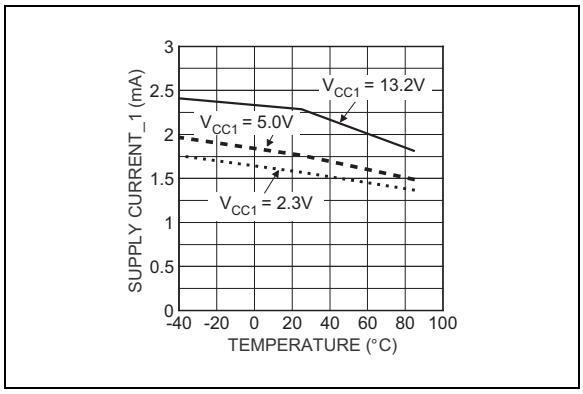


FIGURE 2-21: *Supply Current_1 vs. Temperature.*

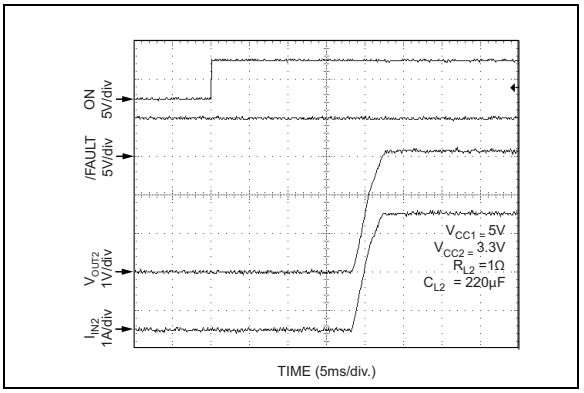


FIGURE 2-24: *Turn-On (Channel 2).*

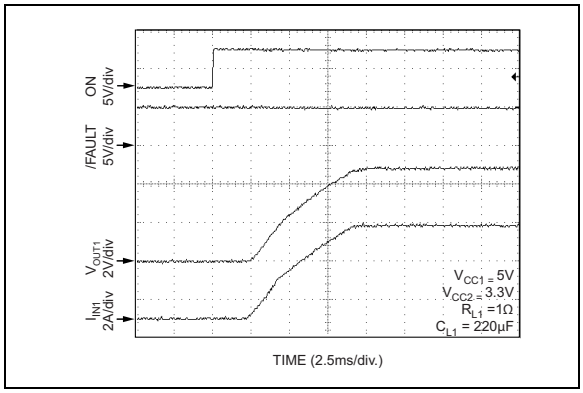


FIGURE 2-25: *Turn-On (Channel 1).*

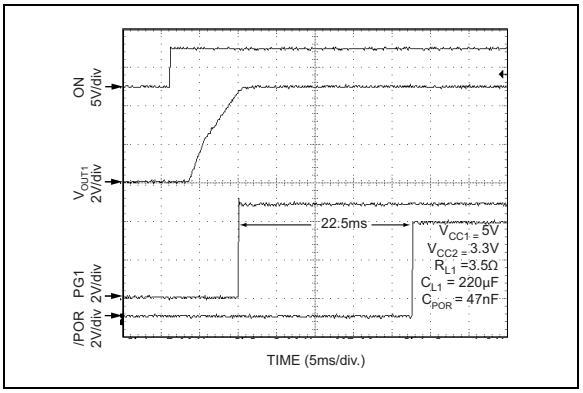


FIGURE 2-28: *Power-on Reset Response.*

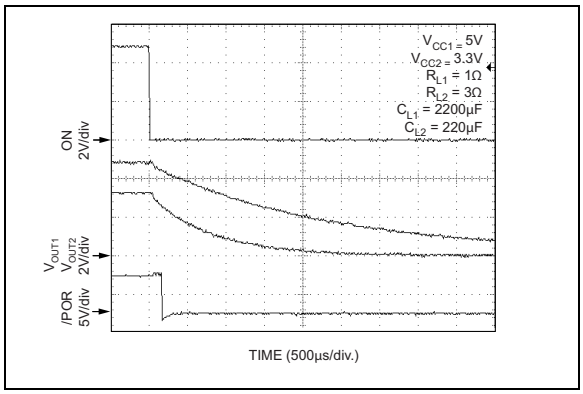


FIGURE 2-26: *Turn-Off.*

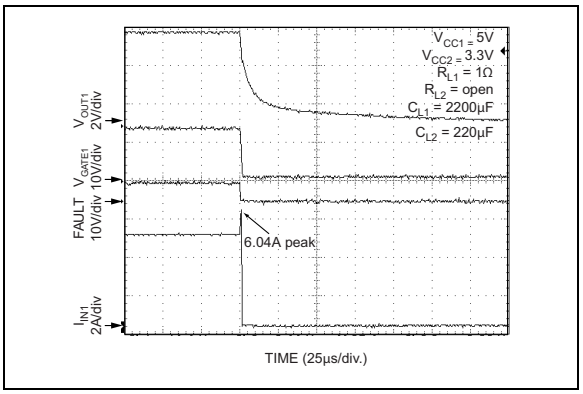


FIGURE 2-29: *Short-Circuit Response.*

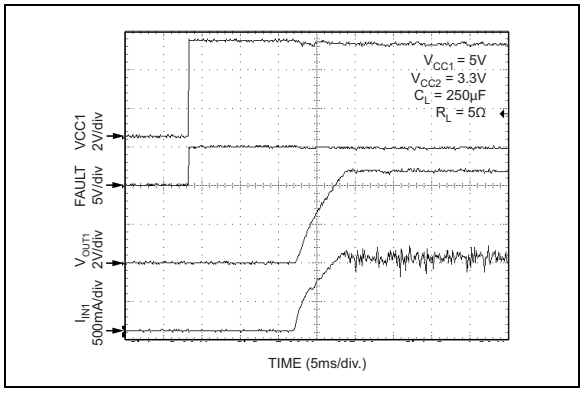


FIGURE 2-27: *Turn-On Response (Hot Insert).*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	VCC2	Positive Supply (Input), Channel 2: The GATE2 pin is held low by an internal undervoltage lockout circuit until V_{CC1} and V_{CC2} exceed their respective undervoltage lockout threshold of 2.165V and 0.8V. This input must be in the range of 1.0V to 13.2V and be less than or equal to V_{CC1}. This input is protected up to 20V.
2, 15	SENSE2, SENSE1	Circuit Breaker Sense (Inputs): A resistor between this pin and VCC1 and VCC2 sets the current limit threshold for each channel. Whenever the voltage across either sense resistor exceeds the slow trip current limit threshold ($V_{TRIPSLOW}$), the GATE voltage is adjusted to ensure a constant load current. If $V_{TRIPSLOW}$ (50 mV) is exceeded for longer than time period t_{OCSLOW}, then the circuit breaker is tripped and both GATE outputs are immediately pulled low. If the voltage across either sense resistor exceeds the fast trip circuit breaker threshold, $V_{TRIPFAST}$, at any point due to fast, high amplitude power supply faults, then both GATE outputs are immediately brought low without delay. To disable the circuit breaker for either channel, the SENSE and VCC pins can be tied together. The default $V_{TRIPFAST}$ for either device is 100 mV. Other fast trip thresholds are available: 150 mV, 200 mV, or OFF ($V_{TRIPFAST}$ disabled). Please contact factory for availability of other options.
3, 14	GATE2, GATE1	Gate Drive (Outputs): Connect each output to the gates of external N-Channel MOSFETs. When ON is asserted, a 14 µA current source is activated and begins to charge the gate of the N-Channel MOSFET connected to this pin. An internal clamp ensures that no more than 10V is applied between the GATE and Source when VCC1 or VCC2 is above 5V. When the circuit breaker trips or when an input undervoltage lockout condition is detected, the GATE1 and GATE2 pins are immediately brought low.
4, 13	OUT2, OUT1	Output Voltage Monitor (Inputs): For output tracking, connect these pins to their respective output to sense the output voltage.
5, 12	FB2, FB1	Power Good Threshold Input (Undervoltage Detect): FB1 and FB2 are internally compared to 1.235V and 0.80V references with 25 mV of hysteresis, respectively. External resistive divider networks may be used to set the voltage at these pins. If either FB input momentarily goes below its threshold, then /POR is activated for one timing cycle, t_{POR}, indicating an output undervoltage condition. The /POR signal deasserts one timing cycle after the FB pin exceeds its power good threshold by 25 mV. A 5 µs filter on these pins prevents glitches from inadvertently activating the /POR signal.
6	ON	Enable (Input): Active-High. The ON pin, an input to a Schmitt-triggered comparator used to enable/disable the controller, is compared to a 1.235V reference with 25 mV of hysteresis. When a logic high is applied to the ON pin (V_{ON} > 1.235V), a start-up sequence begins when the GATE1 and GATE2 pins begin ramping up towards their final operating voltage. When the ON pin receives a logic low signal (V_{ON} < 1.21V), the GATE pins are grounded and /FAULT remains high if both inputs are above their respective UVLO thresholds. The ON pin must be low for at least 20 µs in order to initiate a start-up sequence. Additionally, toggling the ON pin LOW to HIGH resets the circuit breaker.

TABLE 3-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number	Pin Name	Description
7	CPOR	Power-on Reset Timer (Input): A capacitor connected between this pin and ground sets the start-up delay (t_{START}) and the power-on reset interval (t_{POR}). Once the lagging supply rises above its UVLO threshold and ON asserts, the capacitor connected to CPOR begins to charge. When the voltage at CPOR crosses 0.3V, the start-up threshold (V_{START}), a start cycle is initiated as the GATE outputs begin to ramp while capacitor CPOR is immediately discharged to ground. When the voltage at the lagging FB pin rises above its threshold (V_{FB}), capacitor CPOR begins to charge again. When the voltage at CPOR rises above the power-on reset delay threshold (V_{POR}) of 1.235V, the timer resets by pulling CPOR to ground and /POR is deasserted. If CPOR = 0, then t_{START} defaults to 20 µs.
8	CFILTER	Current Limit Response Timer (Input): A capacitor connected to this pin defines the period of time, t_{OCSLOW}, in which an overcurrent event must last to signal a fault condition and trip the circuit breaker. When an overcurrent condition occurs, a 2.5 µA current source begins to charge this capacitor. If the voltage at this pin reaches 1.235V, the circuit breaker is tripped, both GATE pins immediately shut off, and /FAULT is asserted. If C_{FILTER} = 0, then t_{OCSLOW} defaults to 20 µs.
9	GND	Ground: Tie to analog ground.
10	/FAULT	Circuit Breaker Fault Status (Output): Active-Low, weak pull-up to VCC1 or open-drain. Asserted when the circuit breaker is tripped due to an overcurrent, undervoltage lockout event.
11	/POR	Power-on Reset (Output): Active-Low, weak pull-up to VCC1 or open drain. This pin remains asserted during start-up until a time period (t_{POR}) after the lagging FB pin threshold (V_{FB1} or V_{FB2}) is exceeded. The timing capacitor CPOR determines t_{POR}. When the output voltage monitored at either FB pin falls below V_{FB}, /POR is asserted for a minimum of one timing cycle (t_{POR}).
16	VCC1	Positive Supply (Input), Channel 1: This input is the main supply to the internal circuitry and must be in the range of 2.3V to 13.2V. The GATE1 pin is held low by an internal undervoltage lockout circuit until V_{CC1} and V_{CC2} exceed their respective undervoltage lockout threshold of 2.165V and 0.8V. This input is protected up to 20V.

4.0 FUNCTIONAL DESCRIPTION

4.1 Hot Swap Insertion

When circuit boards are inserted into live system backplanes and supply voltages, high inrush currents can result due to the charging of bulk capacitance that resides across the supply pins of the circuit board. This inrush current, although transient in nature, may be high enough to cause permanent damage to on-board components or may cause the system's supply voltages to go out of regulation during the transient period, which may result in system failures. The MIC2584 acts as a controller for external N-channel MOSFET devices in which the gate drive is controlled to provide inrush current limiting and output voltage slew rate control during hot swap insertions.

4.2 Power Supply

V_{CC1} is the main supply input to the MIC2584 controller with a voltage range of 2.3V to 13.2V. The V_{CC2} supply input ranges from 1.0V to 13.2V and must be less than or equal to V_{CC1} for operation. Both inputs can withstand transient spikes up to 20V. In order to ensure stability of the supplies, a minimum 1 µF capacitor from each V_{CC} to ground is recommended. Alternatively, a low pass filter, shown in the Typical Application Circuit, can be used to eliminate high frequency oscillations as well as help suppress transient spikes.

Also, due to the existence of undetermined parasitic inductance in the absence of bulk capacitance, placing a Zener diode at each V_{CC} of the controller to ground in order to provide external supply transient protection is strongly recommended. See the Typical Application Circuit.

4.3 Start-Up Cycle

4.3.1 SUPPLY CONTACT DELAY

During a hot insert of a PC board into a backplane or when the main supply (V_{CC1}) is powered up from a cold start, as the voltage at the ON pin rises above its threshold (1.235V typical), the MIC2584 first checks that both supply voltages are above their respective UVLO thresholds. If so, then the device is enabled and an internal 2.5 µA current source begins charging the capacitor CPOR to 0.3V to initiate a start-up sequence. Once the start-up delay (t_{START}) elapses, the CPOR pin is pulled immediately to ground and a separate 14 µA current source begins charging each GATE output to drive the external MOSFET that switches V_{IN} to V_{OUT}. The programmed contact start-up delay is calculated using Equation 4-1:

EQUATION 4-1:

$$t_{START} = C_{POR} \times \frac{V_{START}}{I_{CPOR}} \cong 0.12 \times C_{POR}(\mu F)$$

Where:

Start-up delay timer threshold (V_{START}) =	0.3V
Power-on Reset timer current (I_{CPOR}) =	2.5 µA

See Table 4-2 for some typical supply contact start-up delays using several standard value capacitors. As each GATE voltage continues ramping toward its final value (V_{CC} + V_{GS}) at a defined slew rate (See the Load Capacitance Dominated Start-Up and GATE Capacitance Dominated Start-Up sections), a second CPOR timing cycle begins if: /FAULT is high and CFILTER is low (i.e., not an overvoltage, undervoltage lockout, or overcurrent state).

This second timing cycle (t_{POR}) begins when the lagging voltage exceeds its FB pin threshold (V_{FB}). See Figure 1-4 in the Timing Diagrams section. When the power supply is already present (i.e., not a "hot swapping" condition) and the MIC2584 device is enabled by applying a logic high signal at the ON pin, the GATE outputs begin ramping immediately as the first CPOR timing cycle is bypassed. Active current regulation is employed to limit the inrush current transient response during start-up by regulating the load current at the programmed current limit value (See the Current Limiting and Dual-Level Circuit Breaker section). Equation 4-2 is used to determine the nominal current limit value:

EQUATION 4-2:

$$I_{LIM} = \frac{V_{TRIPSLOW}}{R_{SENSE}} = \frac{50mV}{R_{SENSE}}$$

Where:

$V_{TRIPSLOW}$ =	The current limit slow trip threshold.
R_{SENSE} =	The selected value that sets the desired current limit.

There are two basic start-up modes for the MIC2584: Start-up dominated by load capacitance and start-up dominated by total gate capacitance. The magnitude of the inrush current delivered to the load will determine the dominant mode. If the inrush current is greater than the programmed current limit (I_{LIM}), then load capacitance is dominant. Otherwise, gate capacitance is dominant. The expected inrush current may be calculated using Equation 4-3:

EQUATION 4-3:

$$INRUSH = I_{GATE} \times \frac{C_{LOAD}}{C_{GATE}} \cong 14\mu A \times \frac{C_{LOAD}}{C_{GATE}}$$

Where:

I_{GATE} =	GATE pin pull-up current
C_{LOAD} =	The total GATE capacitance
C_{GATE} =	Total GATE capacitance (The C_{ISS} of the external MOSFET and any external capacitor connected from the MIC2584 GATE pin to ground.)

4.3.2 LOAD CAPACITANCE DOMINATED START-UP

In this case, the load capacitance (C_{LOAD}) is large enough to cause the inrush current to exceed the programmed current limit but is less than the fast-trip threshold (or the fast-trip threshold is disabled, 'M' option). During start-up under this condition, the load current is regulated at the programmed current limit value (I_{LIM}) and held constant until the output voltage rises to its final value. The output slew rate and equivalent GATE voltage slew rate is computed by Equation 4-4:

EQUATION 4-4:

$$dV_{OUT}/dt = \frac{I_{LIM}}{C_{LOAD}}$$

Where:

I_{LIM} =	The programmed current limit value.

Consequently, the value of C_{FILTER} must be selected to ensure that the overcurrent response time, t_{OCSLOW}, exceeds the time needed for the output to reach its final value. For example, given a MOSFET with an input capacitance C_{ISS} = C_{GATE} = 2000 pF, C_{LOAD} is 1000 µF, and I_{LIM} is set to 5A with a 12V input, then the load capacitance dominates as determined by the calculated INRUSH > I_{LIM}. Therefore, the output voltage slew rate determined from Equation 4-5 is:

EQUATION 4-5:

$$dV_{OUT}/dt = \frac{5A}{100\mu F} = 5 \times \frac{V}{ms}$$

The resulting t_{OCSLOW} needed to achieve a 12V output is approximately 2.5 ms. See the Power-on Reset, Overcurrent Timer, and Sequenced Output Delays section to calculate t_{OCSLOW}.

4.3.3 GATE CAPACITANCE DOMINATED START-UP

In this case, the value of the load capacitance relative to the GATE capacitance is small enough such that during start-up the output current never exceeds the current limit threshold as determined by Equation 4-3. The minimum value of C_{GATE} that will ensure that the current limit is never exceeded is given by Equation 4-6:

EQUATION 4-6:

$$C_{GATE(MIN)} = \frac{I_{GATE}}{I_{LIMIT}} \times C_{LOAD}$$

Where:

C_{GATE} =	The summation of the MOSFET input capacitance (C_{ISS}) specification and the value of the capacitor connected to the GATE pin of the MIC2584 (and MOSFET) to ground.

Once C_{GATE} is determined, use Equation 4-7 to determine the output slew rate dV_{OUT}/dt for gate capacitance dominated start-up:

EQUATION 4-7:

$$dV_{OUT}/dt = \frac{I_{GATE}}{C_{GATE}}$$

Table 4-1 depicts the output slew rate for various values of C_{GATE}.

TABLE 4-1: OUTPUT SLEW RATE SELECTION FOR GATE CAPACITANCE DOMINATED START-UP

I_{GATE} = 14 µA	
C_{GATE}	dV_{OUT}/dt
0.001 µF	14V/ms
0.01 µF	1.4V/ms
0.1 µF	0.14V/ms
1 µF	0.014V/ms

4.4 Current Limiting and Dual-Level Circuit Breaker

Many applications will require that the inrush and steady state supply current be limited at a specific value in order to protect critical components within the system. Connecting a sense resistor between the VCC and SENSE pins of each channel sets the nominal current limit value for each channel of the MIC2584 and the current limit is calculated using Equation 4-2.

The MIC2584 also features a dual-level circuit breaker triggered via 50 mV and 100 mV current limit thresholds sensed across the VCC and SENSE pins. The first level of the circuit breaker functions as follows. For the MIC2584, once the voltage sensed across these two pins exceeds 50 mV on either channel, the overcurrent timer, its duration set by capacitor C_{FILTER}, starts to ramp the voltage at CFILTER using a 2.5 µA constant current source. If the voltage at CFILTER reaches the overcurrent timer threshold (V_{TMR}) of 1.235V, then CFILTER immediately returns to ground as the circuit breaker trips and both GATE outputs are immediately shut down. For the second level, if the voltage sensed across VCC and SENSE of either channel exceeds 100 mV (–J option) at any time, the circuit breaker trips and both GATE outputs shut down immediately, bypassing the overcurrent timer period. To disable current limit and circuit breaker operation, tie each channel's SENSE and VCC pins together and the CFILTER pin to ground.

4.5 Output Undervoltage Detection

The MIC2584 employ output undervoltage detection by monitoring the output voltage through a resistive divider connected at the FB pins. During turn on, while the voltage at either FB pin is below its threshold (V_{FB}), the /POR pin is asserted low. Once both FB pin voltages cross their respective threshold (V_{FB}), a 2.5 µA current source charges capacitor C_{POR}. Once the CPOR pin voltage reaches 1.235V, the time period t_{POR} elapses as pin CPOR is pulled to ground and the /POR pin goes HIGH. If the voltage at either FB drops below V_{FB} for more than 10 µs, the /POR pin resets for at least one timing cycle defined by t_{POR} (See Application Information for an example).

4.6 Power-on Reset, Overcurrent Timer, and Sequenced Output Delays

The Power-on Reset delay, t_{POR}, is the time period for the /POR pin to go HIGH once the lagging voltage exceeds the power good threshold (V_{FB}) monitored at the FB pin. A capacitor connected to CPOR sets the interval and is determined by using Equation 4-8 with V_{POR} substituted for V_{START}. The resulting equation becomes:

EQUATION 4-8:

$$t_{POR} = C_{POR} \times \frac{V_{POR}}{I_{CPOR}} \cong 0.5 \times C_{POR}(\mu F)$$

Where:

V_{POR} (Power-on Reset threshold) = 1.235V

I_{CPOR} (Timer current) = 2.5 µA

For the MIC2584, a capacitor connected to CFILTER is used to set the timer that activates the circuit breaker during overcurrent conditions. When the voltage across either sense resistor exceeds the slow trip current limit threshold of 50 mV, the overcurrent timer begins to charge for a period, t_{OCSLOW}, determined by C_{FILTER}. If t_{OCSLOW} elapses, then the circuit breaker is activated and both GATE outputs are immediately pulled to ground. The following equation is used to determine the overcurrent timer period, t_{OCSLOW}.

EQUATION 4-9:

$$t_{OCSLOW} = C_{FILTER} \times \frac{V_{TMR}}{I_{TMR}} \cong 0.5 \times C_{FILTER}(\mu F)$$

Where:

The overcurrent timer threshold (V_{TMR}) = 1.235V

The overcurrent timer current (I_{TMR}) = 2.5 µA

If no capacitor for CFILTER is used, then t_{OCSLOW} defaults to 20 µs.

Table 4-2 and Table 4-3 provide a quick reference for several timer calculations using selected standard value capacitors.

4.7 Undervoltage Lockout

Internal circuitry keeps both GATE output charge pumps off until V_{CC1} and V_{CC2} exceed 2.165V and 0.8V, respectively.

TABLE 4-2: SELECTED POWER-ON RESET AND START-UP DELAYS

C_{POR}	t_{START}	t_{POR}
0.01 µF	1.2 ms	5 ms
0.033 µF	4 ms	16.5 ms
0.05 µF	6 ms	25 ms
0.1 µ µF	12 ms	50 ms
0.33 µF	40 ms	165 ms
0.47 µF	56 ms	235 ms
1 µF	120 ms	500 ms

TABLE 4-3: SELECTED OVERCURRENT TIMER DELAYS

C_{FILTER}	t_{OSCLOW}
220 pF	110 µs
680 pF	340 µs
1000 pF	500 µs
3300 pF	1.6 ms
0.01 µF	5 ms
0.047 µF	23.5 ms
0.1 µF	50 ms
0.33 µF	165 ms

5.0 APPLICATION INFORMATION

5.1 Output Tracking and Sequencing

The MIC2584 can be used in systems that support more than two supplies. Figure 5-1 illustrates the generic use of two separate controllers configured to support four independent supply rails with an associated output timing response. The /POR output of the first controller is used to enable the second controller. As configured, a fault condition on either V_{OUT1} or V_{OUT2} will result in all channels being shut down. For systems with multiple power sequencing requirements, the controllers' output tracking and sequencing features can be implemented in order to meet the system's timing demands.

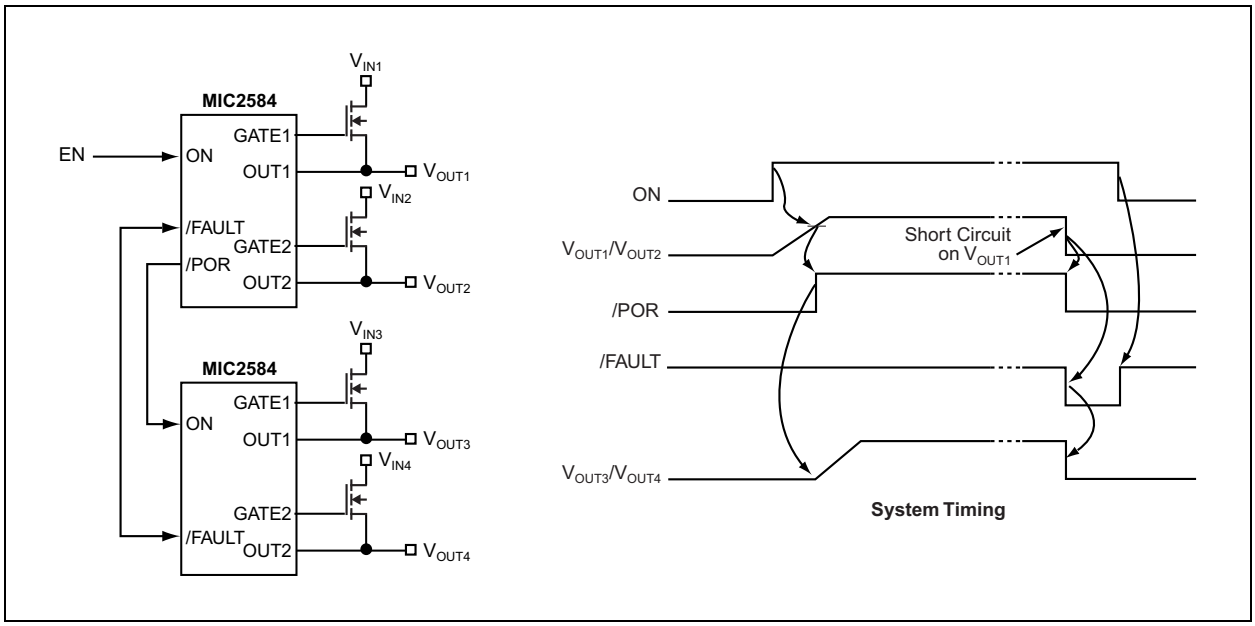


FIGURE 5-1: *Supporting More Than Two Supplies.*

5.2 Output Undervoltage Detection

For output undervoltage detection, the first consideration is to establish the output voltage level that indicates "power is good." For this example, the output value for which a 12V supply will signal "good" is 10.5V. Next, consider the tolerances of the input supply and FB threshold (V_{FB}). For this example, given a 12V ±5% supply for Channel 1, the resulting output voltage may be as low as 11.4V and as high as 12.6V. Additionally, the FB1 threshold has ±50 mV tolerance and may be as low as 1.19V and as high as 1.29V. Thus, to determine the values of the resistive divider network (R12 and R13) at the FB1 pin, shown in Typical Application Circuit, use the following iterative design procedure.

Choose R13 so as to limit the current through the divider to approximately 100 µA or less.

EQUATION 5-1:

$$R13 \cong \frac{V_{FB1(MAX)}}{100\mu A} \cong \frac{1.29V}{100\mu A} \cong 12.9k\Omega$$

Where:

R13 = 14.7 kΩ ±1%

Next, determine R12 using the output "good" voltage of 10.5V and Equation 5-2:

EQUATION 5-2:

$$V_{OUT1(GOOD)} = V_{FB1(MAX)}\left[\frac{(R12 + R13)}{R13}\right]$$

Using some basic algebra and simplifying Equation 5-2 to isolate R12, yields:

EQUATION 5-3:

$$R12 = R13\left[\left(\frac{V_{OUT1(GOOD)}}{V_{FB1(MAX)}}\right)\right]-1$$

Where:

$V_{FB1(MAX)}$ = 1.29V
$V_{OUT1(GOOD)}$ = 10.5V
R13 = 14.7kΩ

Substituting these values into Equation 5-3 now yields R12 = 104.95 kΩ. A standard 105 kΩ ±1% is selected. Now, consider the 11.4V minimum output voltage, the lower tolerance for R13 and higher tolerance for R12, 14.55 kΩ and 106.05 kΩ, respectively. With only 11.4V available, the voltage sensed at the FB1 pin exceeds $V_{FB1(MAX)}$, thus the /POR signal will transition from LOW to HIGH indicating “power is good” given the worse case tolerances of this example. A similar approach should be used for Channel 2

5.3 PCB Connection Sense

There are several configuration options for the MIC2584’s ON pin to detect if the PCB has been fully seated in the backplane before initiating a start-up cycle. In Typical Application Circuit, the MIC2584 is mounted on the PCB with a resistive divider network connected to the ON pin. R4 is connected to a short pin on the PCB edge connector. Until the connectors mate, the ON pin is held low which keeps the GATE output charge pump off. Once the connectors mate, the resistor network is pulled up to the input supply, 12V in this example, and the ON pin voltage exceeds its threshold (V_{ON}) of 1.235V and the MIC2584 initiates a start-up cycle. In Figure 5-2, the connection sense consisting of a discrete logic-level MOSFET and a few resistors allows for interrupt control from the processor or other signal controller to shut off the output of the MIC2584. R4 pulls the GATE of Q2 to V_{IN} and the ON pin is held low until the connectors are fully mated. Once the connectors fully mate, a logic LOW at the /ON_OFF signal turns Q2 off and allows the ON pin to pull up above its threshold and initiate a start-up cycle. Applying a logic HIGH at the /ON_OFF signal will turn Q2 on and short the ON pin of the MIC2584 to ground, which turns off the GATE output charge pump.

5.4 Higher UVLO Setting

Once a PCB is inserted into a backplane (power supply), the internal UVLO circuit of the MIC2584 holds the GATE output charge pump off until V_{CC1} exceeds 2.165V and V_{CC2} exceeds 0.8V. If V_{CC1} falls below 1.935V or V_{CC2} falls below 0.77V, the UVLO circuit pulls the GATE output to ground and clears the overvoltage and/or current limit faults. For a higher UVLO threshold, the circuit in Figure 5-3 can be used to delay the output MOSFET from switching on until the desired input voltage is achieved. The circuit allows the charge pumps to remain off until V_{IN1} exceeds (1 + R1/R2) x 1.235V, provided that V_{CC2} has exceeded its threshold. Both GATE drive outputs will be shut down when V_{IN1} falls below (1 + R1/R2) x 1.21V.

In Figure 5-3, the rising UVLO threshold is set at approximately 9.0V and the falling UVLO threshold is established as 8.9V. The circuit consists of an external resistor divider at the ON pin that keeps both GATE output charge pumps off until the voltage at the ON pin exceeds its threshold (V_{ON}) and after the start- up timer elapses.

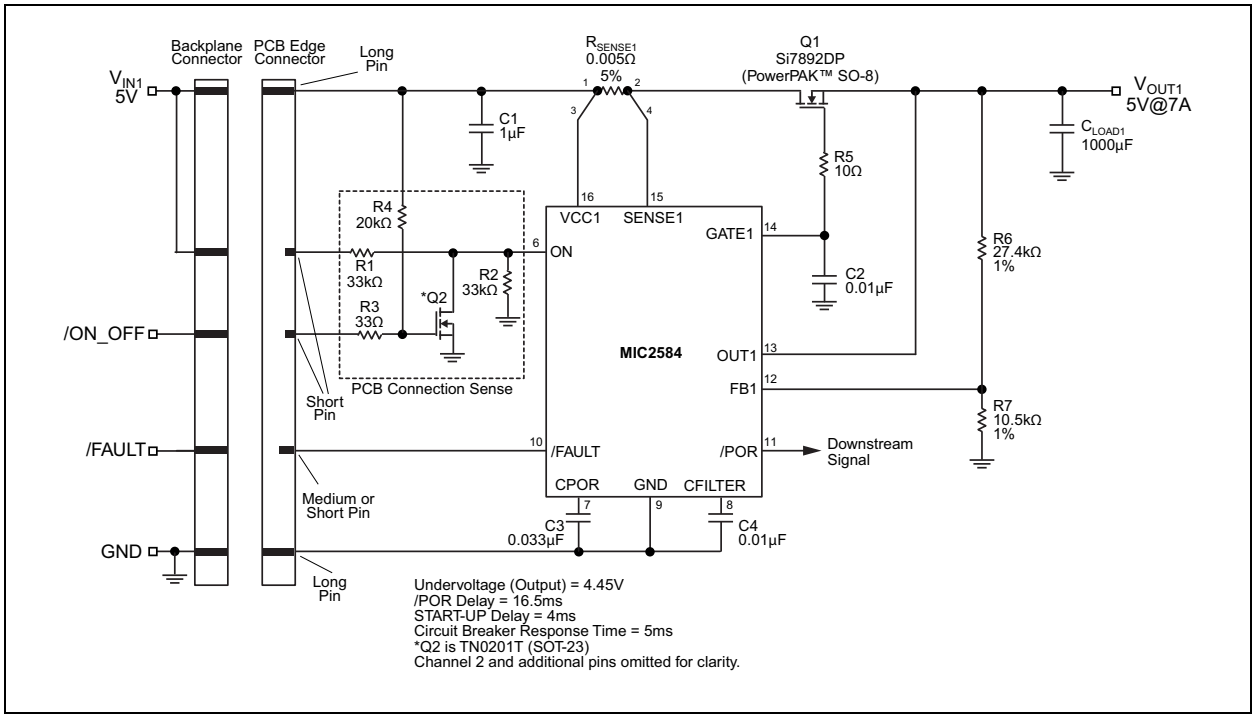


FIGURE 5-2: *PCB Connection Sense with ON/OFF Control.*

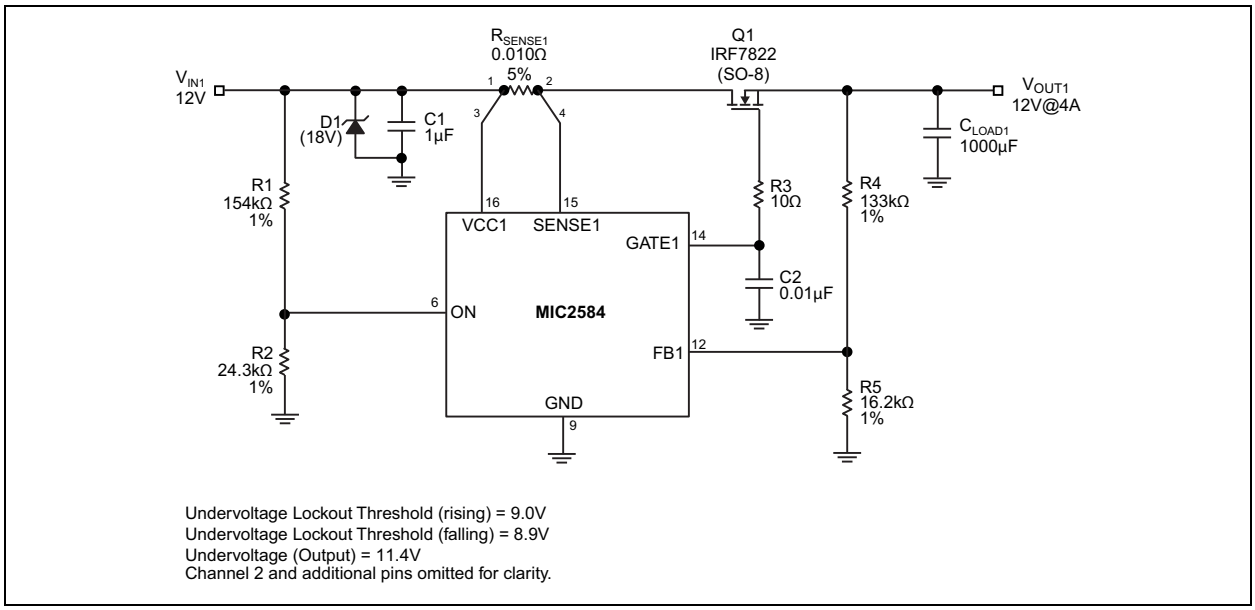


FIGURE 5-3: *Higher UVLO Setting.*

5.5 Sense Resistor Selection

The MIC2584 uses a low value sense resistor to measure the current flowing through the MOSFET switch (and therefore the load). This sense resistor is nominally set at 50 mV/$I_{LOAD(CONT)}$. To accommodate worst case tolerances for both the sense resistor (allow ±3% over time and temperature for a resistor with ±1% initial tolerance) and still supply the maximum required steady-state load current, a slightly more detailed calculation must be used.

The current limit threshold voltage (i.e., the “trip point”) for the MIC2584 may be as low as 42.5 mV, which would equate to a sense resistor value of 42.5 mV/$I_{LOAD(CONT)}$. Carrying the numbers through for the case where the value of the sense resistor is 3% high yields:

EQUATION 5-4:

$$R_{SENSE(MAX)} = \frac{42.5mV}{(1.03)(I_{LOAD(CONT)})} = \frac{41.3mV}{I_{LOAD(CONT)}}$$

Once the value of R_{SENSE} has been chosen in this manner, it is good practice to check the maximum $I_{LOAD(CONT)}$ which the circuit may let through in the case of tolerance build-up in the opposite direction. Here, the worst case maximum current is found using a 57.5 mV trip voltage and a sense resistor that is 3% low in value. The resulting equation is:

EQUATION 5-5:

$$I_{LOAD(CONTMAX)} = \frac{57.5mV}{0.97(R_{SENSE(NOM)})} = \frac{59.3mV}{R_{SENSE(NOM)}}$$

As an example, if an output must carry a continuous 6A without nuisance trips occurring, Equation 5-4 yields:

EQUATION 5-6:

$$R_{SENSE(MAX)} = \frac{41.3mV}{6A} = 6.88m\Omega$$

The next lowest standard value is 6 mΩ, and the other set of tolerance extremes for the output in question.

EQUATION 5-7:

$$I_{LOAD(CONTMAX)} = \frac{59.3mV}{6.0m\Omega} = 9.88A$$

Knowing this final data, we can determine the necessary wattage of the sense resistor using $P = I^2R$, where I will be $I_{LOAD(CONTMAX)}$, and R will be $(0.97)(R_{SENSE(NOM)})$. These numbers yield the following:

EQUATION 5-8:

$$P_{MAX} = (9.88A)^2 \times (5.82m\Omega) = 0.568W$$

In this example, a 1W sense resistor is sufficient.

5.6 MOSFET Selection

Selecting the proper external MOSFET for use with the MIC2584 involves three straightforward tasks:

- Choose a MOSFET that meets minimum voltage requirements.
- Select a device to handle the maximum continuous current (steady-state thermal issues).
- Verify the selected part's ability to withstand any peak currents (transient thermal issues).

5.7 MOSFET Voltage Requirements

The first voltage requirement for the MOSFET is easily stated: the drain-source breakdown voltage of the MOSFET must be greater than $V_{IN(MAX)}$. For instance, a 12V input may reason ably be expected to see high frequency transients as high as 18V. Therefore, the drain-source breakdown voltage of the MOSFET must be at least 19V. For ample safety margin and standard availability, the closest minimum value will be 20V.

The second breakdown voltage criterion that must be met is a bit subtler than simple drain source breakdown voltage, but is not hard to meet. In MIC2584 applications, the gate of the external MOSFET is driven up to approximately 20V by the internal output MOSFET (again, assuming 12V operation). At the same time, if the output of the external MOSFET (its source) is suddenly subjected to a short, the gate source voltage will go to (20V - 0V) = 20V. This means that the external MOSFET must be chosen to have a gate-source breakdown voltage of 20V or more, which is an available standard maximum value. However, if operation is above 12V, the 20V gate source maximum will likely be exceeded. As a result, an external Zener diode clamp should be used to prevent breakdown of the external MOSFET when operating at voltages above 10V. A Zener diode with 10V rating is recommended as shown in Figure 5-4. At the present time, most power MOSFETs with a 20V gate-source voltage rating have a 30V drain source break down rating or higher. As a general tip, choose surface mount devices with a drain source rating of 30V as a starting point.

Finally, the external gate drive of the MIC2584 requires a low voltage logic level MOSFET when operating at voltages lower than 3V. There are 2.5V logic level MOSFETs available.

5.8 MOSFET Steady State Thermal Issues

The selection of a MOSFET to meet the maximum continuous current is a fairly straightforward exercise. First, the following steps have to be taken:

- The value of $I_{LOAD(CONTMAX)}$ for the output in question (see Sense Resistor Selection).
- The manufacturer's data sheet for the candidate MOSFET.
- The maximum ambient temperature in which the device will be required to operate.
- Any information that can be acquired about the heat sinking available to the device (e.g., through the ground plane/power plane).

The data sheet will almost always give a value of on resistance given for the MOSFET at a gate source voltage of 4.5V, and another value at a gate source voltage of 10V. As a first approximation, add the two values together and divide by two to get the on resistance of the part with 8V of enhancement. Call this value R_{ON}. Because a heavily enhanced MOSFET acts as an ohmic (resistive) device, almost all that's required to determine steady state power dissipation is to calculate I^2R. The one addendum to this is that MOSFETs have a slight increase in R_{ON} with increasing die temperature. A good approximation for this value is 0.5% increase in R_{ON} per °C rise in junction temperature above the point at which R_{ON} was initially specified by the manufacturer. For instance, if the selected MOSFET has a calculated R_{ON} of 10 mΩ at T_J = 25°C, and the actual junction temperature ends up at 110°C, a good first cut at the operating value for R_{ON} would be:

EQUATION 5-9:

$$R_{ON} \cong 10m\Omega[1 + (110 - 25)(0.005)] \cong 14.3m\Omega$$

The final step is to make sure that the heat sinking available to the MOSFET is capable of dissipating at least as much power (rated in °C/W) as that with which the MOSFET's performance was specified by the manufacturer. Here are a few practical tips:

- The heat from a surface mount device such as an SO-8 MOSFET flows almost entirely out of the drain leads. If the drain leads can be soldered down to one square inch or more, the copper will act as the heat sink for the part. This copper must be on the same layer of the board as the MOSFET drain.
- Even a few LFM (linear feet per minute) of air will cool a MOSFET down substantially. If possible, position the MOSFET(s) near the inlet of a power supply's fan, or the outlet of a processor's cooling fan.
- The best test of a surface mount MOSFET for an application (assuming the above tips show it to be a likely fit) is an empirical one. Check the MOSFET's temperature in the actual layout of the expected final circuit, at full operating current. The use of a thermocouple on the drain leads, or infrared pyrometer on the package, will then give a reasonable idea of the device's junction temperature.

5.9 MOSFET Transient Thermal Issues

Having chosen a MOSFET that will withstand the imposed voltage stresses, and the worst case continuous I^2R power dissipation which it will see, it remains only to verify the MOSFET's ability to handle short term overload power dissipation without overheating. A MOSFET can handle a much higher pulsed power without damage than its continuous dissipation ratings would imply. The reason for this is that, like everything else, thermal devices (silicon die, lead frames, etc.) have thermal inertia.

In terms related directly to the specification and use of power MOSFETs, this is known as "transient thermal impedance," or $Z_{\theta(JA)}$. Almost all power MOSFET data sheets give a Transient Thermal Impedance Curve. For example, take the following case: V_{IN} = 12V, t_{OCSLOW} has been set to 100 ms $I_{LOAD(CONT.MAX)}$ is 1.2A, the slow-trip threshold is 50 mV nominal, and the fast trip threshold is 100 mV. If the output is accidentally connected to a 6Ω load, the output current from the MOSFET will be regulated to 1.2A for 100 ms (t_{OCSLOW}) before the part trips. During that time, the dissipation in the MOSFET is given by:

EQUATION 5-10:

$$P = E \times IE_{MOSFET} = [12V - (1.2A)(6\Omega)] = 4.8V$$

$$P_{MOSFET} = (4.8V \times 1.2A) = 5.76W for 100ms$$

At first glance, it would appear that a really hefty MOSFET is required to withstand this sort of fault condition. This is where the transient thermal impedance curves become very useful. Figure 5-5 shows the curve for the Vishay (Siliconix) Si4410DY, a commonly used SO-8 power MOSFET.

Taking the simplest case first, we'll assume that once a fault event such as the one in question occurs, it will be a long time, 10 minutes or more, before the fault is isolated and the channel is reset. In such a case, we

can approximate this as a “single pulse” event, that is to say, there’s no significant duty cycle. Then, reading up from the X-axis at the point where “Square Wave Pulse Duration” is equal to 0.1sec (= 100 ms), we see that the $Z_{\theta(JA)}$ of this MOSFET to a highly infrequent event of this duration is only 8% of its continuous $R_{\theta(JA)}$.

This particular part is specified as having an $R_{\theta(JA)}$ of 50°C/W for intervals of 10 seconds or less. Assume T_A = 55°C maximum, 1 square inch of copper at the drain leads, no airflow.

Recalling from the previous approximation hint, the part has an R_{ON} of (0.0335/2) = 17 mΩ at 25°C.

Assume it has been carrying just about 1.2A for some time.

When performing this calculation, be sure to use the highest anticipated ambient temperature ($T_{A(MAX)}$) in which the MOSFET will be operating as the starting temperature, and find the operating junction temperature increase (ΔT_J) from that point. Then, as shown next, the final junction temperature is found by adding $T_{A(MAX)}$ and ΔT_J. Because this is no a closed form equation, getting a close approximation may take one or two iterations, but it’s not a hard calculation to perform, and tends to converge quickly.

Then the starting (steady state) T_J is:

EQUATION 5-11:

$$T_J \cong T_{A(MAX)} + \Delta T_J \cong T_{A(MAX)} + [R_{ON} + (T_{A(MAX)} - T_A)(0.005/(°C))(R_{ON})] \times I^2 \times R_{\theta(JA)}$$

$$T_J \cong 55°C + [17m\Omega + (55°C - 25°C)(0.005)(17m\Omega)] \times (1.2A)^2 \times (50°C/W)$$

$$T_J \cong (55°C + (0.02815W)(50°C/W) \cong 54.6°C$$

Iterate the calculation once to see if this value is within a few percent of the expected final value.For this iteration, we will start with T_J equal to the already calculated value of 54.6°C.

EQUATION 5-12:

$$T_J \cong T_A + [17m\Omega + (56.4°C - 25°C)(0.005)(17m\Omega)] \times (1.2A)^2 \times (50°C/W)$$

$$T_J \cong (55°C + (0.02832W)(50°C/W) \cong 56.42°C$$

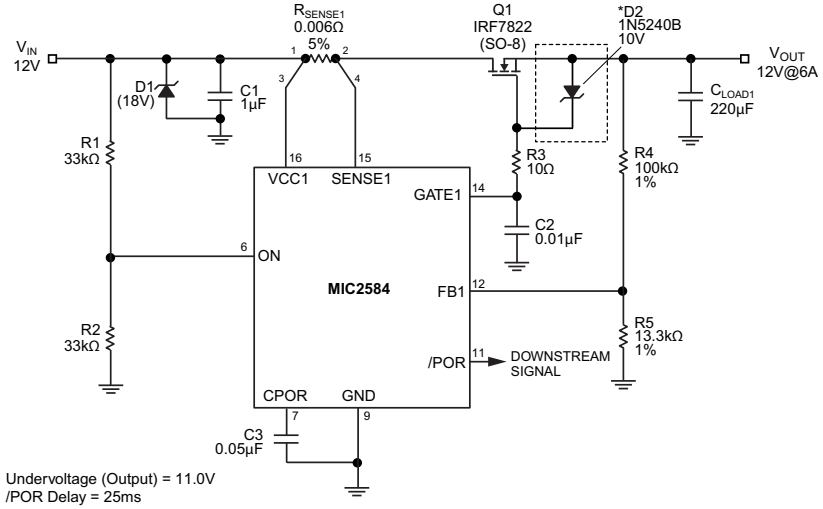


FIGURE 5-4: *Zener Clamped MOSFET Gate.*

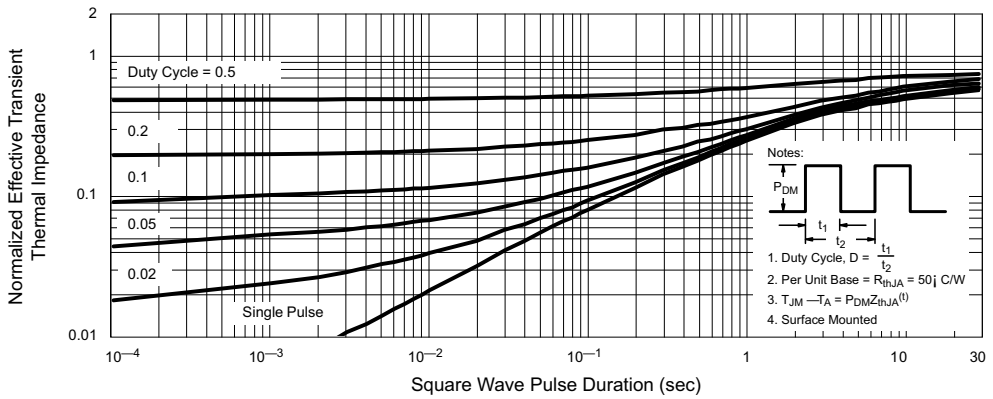
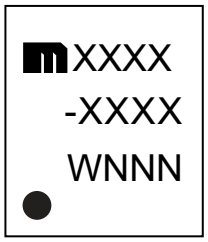


FIGURE 5-5: *Transient Thermal Impedance.*

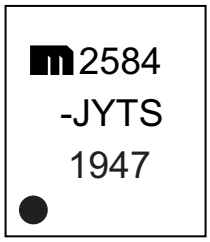
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

16-Lead TSSOP*



Example

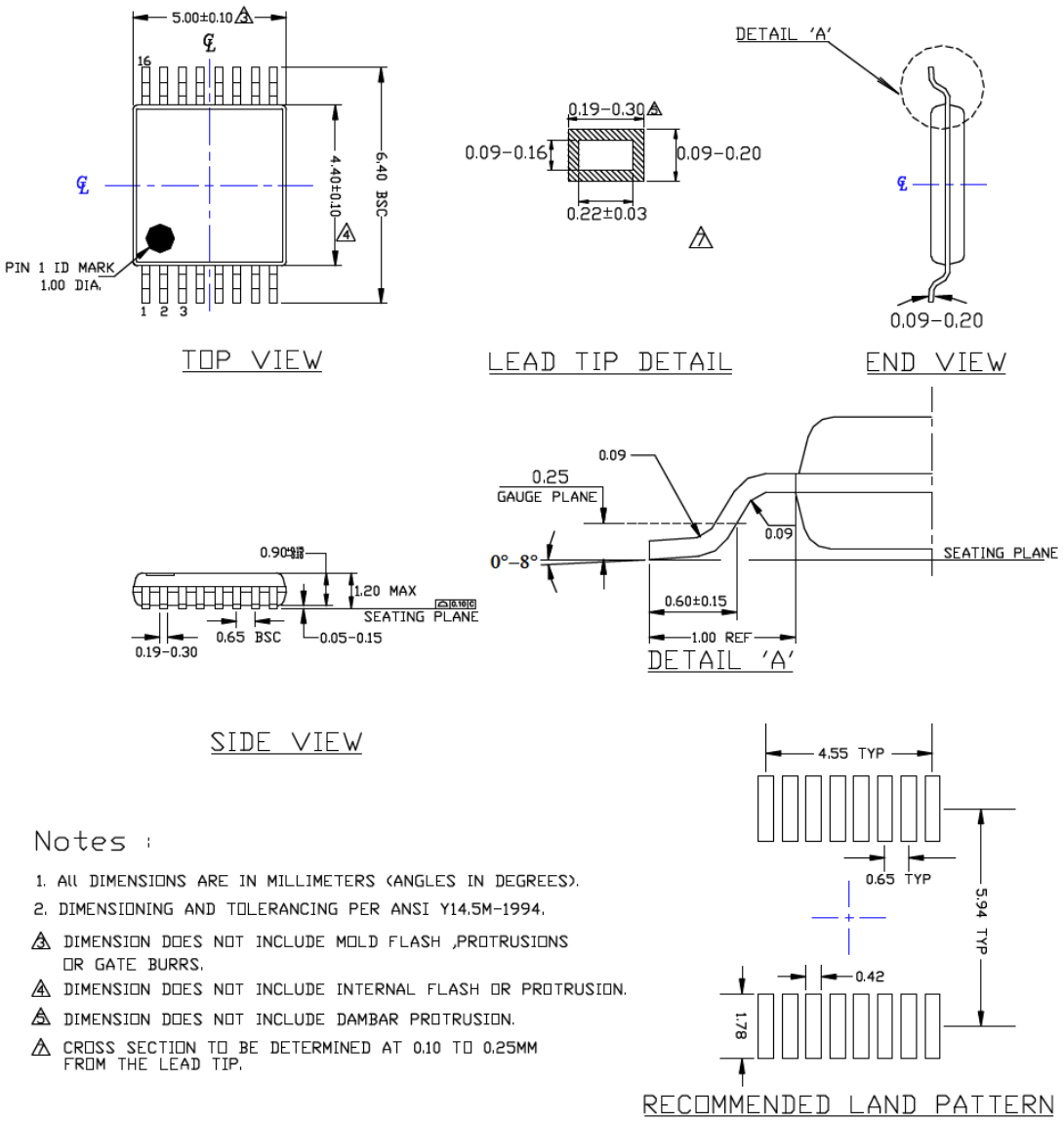


Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

16-Lead TSSOP Package Outline and Recommended Land Pattern

TITLE
16 LEAD TSSOP PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	TSSOP-16LD-PL-1	UNIT	MM



Notes :

1. All DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH ,PROTRUSIONS OR GATE BURRS.
4. DIMENSION DOES NOT INCLUDE INTERNAL FLASH OR PROTRUSION.
5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
6. CROSS SECTION TO BE DETERMINED AT 0.10 TO 0.25MM FROM THE LEAD TIP.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (March 2023)

- Converted Micrel document MIC2584 to Microchip data sheet DS20006617A.
- Minor text changes throughout.
- All reference to the EOL MIC2585 removed.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	–X	X	XX	–XX
Device	Feature	Junction Temperature Range	Package	Media Type

Device:	MIC2584:	Dual-Channel Hot-Swap Controller/ Sequencer
Feature:	Fast Trip Threshold J = K = L = M =	 100 mV 150 mV* 200 mV* Off*
Junction Temperature Range:	Y =	–40°C to +85°C, RoHs Compliant
Package:	TS =	16-Lead TSSOP
Media Type:	Blank = TR =	94/Tube 2,500/Reel

*Contact Sales for availability.

Examples:

a) MIC2584-JYTS:	Dual-Channel Hot-Swap Controller/ Sequencer, 100 mV Fast Circuit Breaker Threshold, Output Latched Off, –40°C to +85°C Temperature Range, RoHS Compliant, 16-Lead TSSOP Package, 94/Tube
b) MIC2584-JYTS-TR:	Dual-Channel Hot-Swap Controller/ Sequencer, 100 mV Fast Circuit Breaker Threshold, Output Latched Off, –40°C to +85°C Temperature Range, RoHS Compliant, 16-Lead TSSOP Package, 2500/Reel
a) MIC2584-KYTS:	Dual-Channel Hot-Swap Controller/ Sequencer, 150 mV Fast Circuit Breaker Threshold, Output Latched Off, –40°C to +85°C Temperature Range, RoHS Compliant, 16-Lead TSSOP Package, 94/Tube
b) MIC2584-KYTS-TR:	Dual-Channel Hot-Swap Controller/ Sequencer, 150 mV Fast Circuit Breaker Threshold, Output Latched Off, –40°C to +85°C Temperature Range, RoHS Compliant, 16-Lead TSSOP Package, 2500/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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