FAIRCHILD SEMICONDUCTOR®

July 2013

FSA2269 / FSA2269TS — Low-Voltage Dual-SPDT (0.4 Ω) Analog Switch with Negative Swing Audio Capability

Features

- 0.4 Ω Typical On Resistance (R_{ON}) for +3.0 V Supply
- 0.25 Ω Maximum R_{ON} Flatness for +3.0 V Supply
- -3 db Bandwidth: > 50 MHz
- Low-I_{CCT} Current Over an Expanded Control Input Range
- Packaged in 10-Lead MicroPak™, UMLP, and WLCSP
- Power-Off Protection on Common Ports
- Broad V_{CC} Operating Range: 1.65 to 4.5 V
- Noise Immunity Termination Resistors in FSA2269TS

Applications

- Cell Phone, PDA, Digital Camera, and Notebook
- LCD Monitor, TV, and Set-Top Box

Description

The FSA2269 is a high-performance, dual Single-Pole Double-Throw (SPDT) analog switch with negative swing audio capability. The FSA2269 features ultra-low R_{ON} of 0.4 Ω (typical) at 3.0 V V_{CC}. The FSA2269 operates over a wide V_{CC} range of 1.65 V to 4.5 V, is fabricated with sub-micron CMOS technology to achieve fast switching speeds, and is designed for break-before-make operation. The select input is TTL-level compatible.

The FSA2269 features very low quiescent current even when the control voltage is lower than the V_{CC} supply. This feature suits mobile handset applications by allowing direct interface with baseband processor general-purpose I/Os with minimal battery consumption.

The FSA2269TS includes termination resistors that improve noise immunity during overshoot excursions, off-isolation coupling, or “pop-minimization.”

Ordering Information

Part Number	Top Mark	Package Description
FSA2269L10X	HL	10-Lead, MicroPak, JEDEC MO-255, 1.6 x 2.1 mm
FSA2269UMX	HP	10-Lead, Quad Ultrathin Molded Leadless Package (UMLP), 1.4 x 1.8 mm, 0.4 mm Pitch
FSA2269TSL10X	HU	10-Lead, MicroPak, JEDEC MO-255, 1.6 x 2.1 mm
FSA2269TSUMX	HT	10-Lead, Quad Ultrathin Molded Leadless Package(UMLP), 1.4 x 1.8 mm, 0.4 mm Pitch
FSA2269UCX	N9	12-Ball, Wafer-Level Chip Scale Package (WLCSP),1.2 x 1.6 mm, 0.4 mm Pitch

Analog Symbols

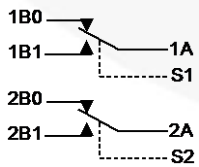

Figure 1. FSA2269

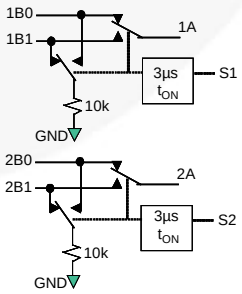

Figure 2. FSA2269TS (with Slow Turn On)

Pin Configuration

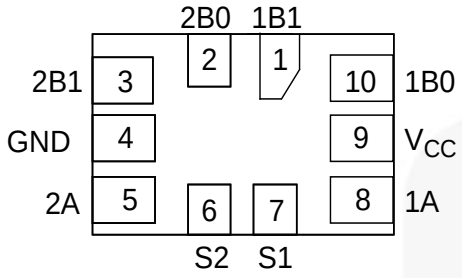

Figure 3. 10-Pin UMLP (Top Through View)

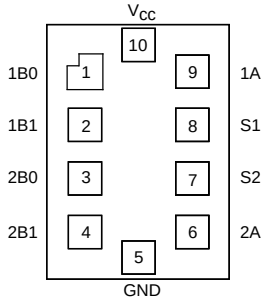

Figure 4. 10-Pin MicroPak™ (Top Through View)

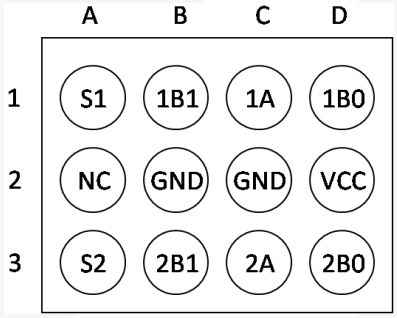

Figure 5. 12-Ball WLCSP (Bump Side View)

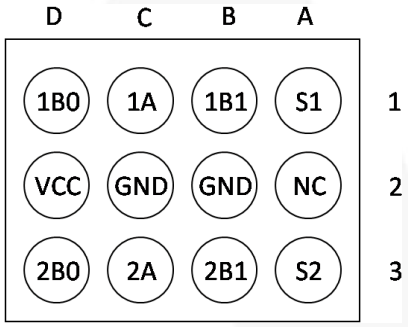

Figure 6. 12-Ball WLCSP (Top Side View)

Pin Descriptions

Pin # UMLP	Pin # Micropak	WLCSP	Name	Description
1	2	B1	1B1	Data Ports
2	3	D3	2B0	Data Ports
3	4	B3	2B1	Data Ports
4	5	B2, C2	GND	Ground
5	6	C3	2A	Data Ports
6	7	A3	S2	Switch Select Pins
7	8	A1	S1	Switch Select Pins
8	9	C1	1A	Data Ports
9	10	D2	V_{CC}	Supply Voltage
10	1	D1	1B0	Data Ports

Truth Table

Control Input, Sn	Function
LOW Logic Level	nB0 connected to nA (FSA2269/2269TS); nB1 terminated to GND (FSA2269TS only)
HIGH Logic Level	nB1 connected to nA (FSA2269/2269TS); nB0 terminated to GND (FSA2269TS only)

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. Functional operation above the recommended operating conditions is not implied. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. Absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage		-0.5	5.5	V
V_{SW}	Switch I/O Voltage[1]	1B0, 1B1, 2B0, 2B1, 1A, 2A Pins	V_{CC} -4.6	5.5	V
V_{CNTRL}	Control Input Voltage[1]	S1, S2	-0.5	V_{CC} +0.3	V
I_{SW}	Switch I/O Current (Continuous)			350	mA
I_{SWPEAK}	Peak Switch Current	Pulsed at 1ms Duration, <10% Duty Cycle		500	mA
T_{STG}	Storage Temperature Range		-65	+150	°C
T_J	Maximum Junction Temperature			+150	°C
T_L	Lead Temperature	Soldering, 10 Seconds		+260	°C
MSL	Moisture Sensitivity Level, JEDEC J-STD-020A		1		
ESD	Human Body Model, JEDEC: JESD22-A114	I/O to GND		12	kV
		I/O to GND FSA2269UCX		11	
		Power to GND		8	
		All Other Pins		7	
	Charged Device Model, JEDEC: JESD22-C101			2	

Note:
1. Input and output negative ratings may be exceeded if input and output diode current ratings are observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage[2]	1.65	4.50	V
$V_{S1, S2}$	Control Input Voltage	0V	V_{CC}	V
V_{SW}	Switch I/O Voltage	V_{CC} -4.3	V_{CC}	V
T_A	Operating Temperature	-40	+85	ºC

Note:
2. For 4.5 V operation, SEL frequency (pins S1 & S2) should not exceed 100 Hz and 50 ns edge rate.

DC Electrical Characteristics

All typical values are T_A=25°C unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} (V)	T_A=+25°C			T_A=-40 to +85°C		Unit
				Min.	Typ.	Max.	Min.	Max.	
V_{IH}	Input Voltage High		3.60 to 4.50				1.70		
			3.00 to 3.60				1.50		V
			2.70 to 3.00				1.35		
			2.30 to 2.70				1.30		
			1.65 to 1.95				0.90		
V_{IL}	Input Voltage Low		3.60 to 4.50					0.7	V
			2.70 to 3.60					0.5	V
			2.30 to 2.70					0.4	
			1.65 to 1.95					0.4	
I_{IN}	Control Input Leakage (S1, S2)	V_{IN}=0 to V_{CC}	1.65 to 4.50				-0.5	0.5	µA
$I_{NO(0FF)}$, $I_{NC(OFF)}$	Off Leakage Current of Port nB0 and nB1 (FSA2269 only)	nA=0.5 V, V_{CC}–0.5 V nB0 or nB1=V_{CC}-0.5 V, 0.5 V, or Floating Figure 8	1.95 to 4.50	-50		50	-250	250	nA
$I_{A(ON)}$	On Leakage Current of Port nA	nA=0.5 V, V_{CC}–0.5 V nB0 or nB1=V_{CC}-0.5 V, 0.5 V, or Floating Figure 9	1.95 to 4.50	-20		20	-150	150	nA
I_{OFF}	Power-Off Leakage Current (Common Port Only 1A, 2A) (FSA2269)	Common Port (1A, 2A), V_{IN}=0 V to 4.5 V, V_{CC}=0V nB0, nB1=Floating	0					±1	µA
	Power-Off Leakage Current (Common Port Only 1A, 2A) (FSA2269TS)	Common Port (1A, 2A), V_{IN}=0V to 4.5 V, V_{CC}=0 V nB0, nB1=0 V or Floating	0					±45	µA
R_{ON}	Switch On Resistance(3,6)	I_{ON}=100 mA, nB0 or nB1=0.7 V, 3.6 V, 4.5 V, Figure 7	4.50		0.30				Ω
		I_{ON}=100 mA, nB0 or nB1=0.7 V, 3.6 V, Figure 7	3.00		0.40			0.80	
		I_{ON}=100mA, nB0 or nB1=0V, 0.7 V, 1.6 V, 2.3 V, Figure 7	2.30		0.52				
		I_{ON}=100 mA, nB0 or nB1=0V, 0.7 V, 1.65 V, Figure 7	1.65		1.00				
ΔR_{ON}	On Resistance Matching Between Channels(4)	I_{ON}=100 mA, nB0 or nB1=0.7 V	4.50		0.04			0.13	Ω
			3.00		0.06			0.13	
			2.30		0.12				
			1.65		1.00				

Continued on the following page…

DC Electrical Characteristics (Continued)

All typical values are T_A=25°C unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} (V)	T_A=+25ºC			T_A= -40 to +85ºC		Unit
				Min.	Typ.	Max.	Min.	Max.	
$R_{FLAT(ON)}$	On Resistance Flatness[5]	I_{OUT}=100 mA, nB0 or nB1=0V to V_{CC}	4.50					0.25	Ω
			3.00					0.25	
			2.30		0.5				
			1.65		0.6				
R_{TERM}	Internal Termination Resistors[6] (FSA2269TS only)				10				kΩ
I_{CC}	Quiescent Supply Current	V_{IN}=0 or V_{CC}, I_{OUT}=0	4.50	-100		100	-500	500	nA
I_{CCT}	Increase in I_{CC} per Input	Input at 2.6 V	4.50		3.0			10.0	µA
		Input at 1.8 V			7.0			15.0	

Notes:

3. On resistance is determined by the voltage drop between A and B pins at the indicated current through the switch.
4. $\Delta R_{ON}=R_{ON\,max}-R_{ON\,min}$ measured at identical V_{CC}, temperature, and voltage.
5. Flatness is defined as the difference between the maximum and minimum value of on resistance (R_{ON}) over the specified range of conditions.
6. Guaranteed by characterization, not production tested.

AC Electrical Characteristics

All typical value are T_A=25°C unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} (V)	T_A=+25ºC			T_A= -40 to +85°C		Unit	Figure
				Min.	Typ.	Max.	Min.	Max.		
t_{ON}	Turn-On Time FSA2269	nB0 or nB1=1.5 V, R_L=50 Ω, C_L=35 pF	3.60 to 4.50			55	15	60	ns	Figure 10 Figure 11
			2.70 to 3.60			60	15	65		
			2.30 to 2.70			100	15	110		
			1.65 to 1.95		70					
	Turn-On Time FSA2269UCX	nB0 or nB1=1.5 V, R_L=50 Ω, C_L=35 pF	3.60 to 4.50			105	15	110	ns	Figure 10 Figure 11
			2.70 to 3.60			115	15	150		
			2.30 to 2.70			180	15	185		
			1.65 to 1.95		110					
	Turn-On Time FSA2269TS	nB0 or nB1=1.5 V, R_L=50 Ω, C_L=35 pF	3.60 to 4.50			3.5	0.5	4.0	µs	Figure 10 Figure 11
			2.70 to 3.60			4.5	0.5	5.0		
			2.30 to 2.70			6.0	0.5	7.0		
			1.65 to 1.95		8.0					
t_{OFF}	Turn-Off Time FSA2269	nB0 or nB1=1.5 V, R_L=50 Ω, C_L=35 pF	3.60 to 4.50			50	5	55	ns	Figure 10 Figure 11
			2.70 to 3.60			55	5	60		
			2.30 to 2.70			60	5	65		
			1.65 to 1.95		40					
	Turn-Off Time FSA2269UCX	nB0 or nB1=1.5 V, R_L=50 Ω, C_L=35 pF	3.60 to 4.50			100	5	105	ns	Figure 10 Figure 11
			2.70 to 3.60			110	5	115		
			2.30 to 2.70			120	5	125		
			1.65 to 1.95		80					
	Turn-Off Time FSA2269TS	nB0 or nB1=1.5 V, R_L=50 Ω, C_L=35 pF	3.60 to 4.50			45	5	50	ns	Figure 10 Figure 11
			2.70 to 3.60			50	5	55		
			2.30 to 2.70			55	5	60		
			1.65 to 1.95		50					
t_{BBM}	Break-Before-Make Time FSA2269[7]	nB0 or nB1=1.5 V, R_L=50 Ω, C_L=35 pF	3.60 to 4.50		3		1		ns	Figure 12
			2.70 to 3.60		5		2			
			2.30 to 2.70		10		2			
			1.65 to 1.95		5		2			
t_{BBM}	Break-Before-Make Time FSA2269UCX[7]	nB0 or nB1=1.5 V, R_L=50 Ω, C_L=35 pF	3.60 to 4.50		9.5		5.5		ns	Figure 12
			2.70 to 3.60		17.0		15.0			
			2.30 to 2.70		22.0		20.0			
			1.65 to 1.95		46.0		41.0			
t_{BBM}	Break-Before-Make Time FSA2269TS[7]	nB0 or nB1=1.5 V, R_L=50 Ω, C_L=35 pF	3.60 to 4.50		1.5		1.0		µs	Figure 12
			2.70 to 3.60		3.0		1.5			
			2.30 to 2.70		4.0		2.5			
			1.65 to 1.95		5.0		3.0			

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AC Electrical Characteristics (Continued)

All typical value are T_A=25°C unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} (V)	T_A=+25ºC			T_A=-40 to +85°C		Unit	Figure
				Min.	Typ.	Max.	Min.	Max.		
Q	Charge Injection	C_L=1.0 nF, V_S=0 V, R_S=0 Ω	1.65 to 4.50		25				pC	Figure 16
OIRR	Off Isolation	f=100 kHz, R_L=50 Ω, C_L=0 pF	1.65 to 4.50		-70				dB	Figure 14
Xtalk	Crosstalk	f=100 kHz, R_L=50 Ω, C_L=0 pF	1.65 to 4.50		-70				dB	Figure 15
BW	-3db Bandwidth	R_L=50 Ω, C_L=0 pF	1.65 to 4.50		>50				MHz	Figure 13
THD	Total Harmonic Distortion	f=20 Hz to 20 kHz, R_L=32 Ω, V_{IN}=2 V_{PP} V_{BIAS}=0 V	1.65 to 4.50		.06				%	Figure 19

Notes:

7. Guaranteed by characterization, not production tested.

Capacitance

Symbol	Parameter	Conditions	V_{CC} (V)	T_A=+25°C			Unit	Figure
				Min.	Typ.	Max.		
C_{IN}	Control Pin Input Capacitance	f=1 MHz	0		2.5		pF	Figure 17
C_{OFF}	B Port Off Capacitance	f=1 MHz	3.3		30		pF	Figure 17
C_{ON}	A Port On Capacitance	f=1 MHz	3.3		120		pF	Figure 18

Test Diagrams

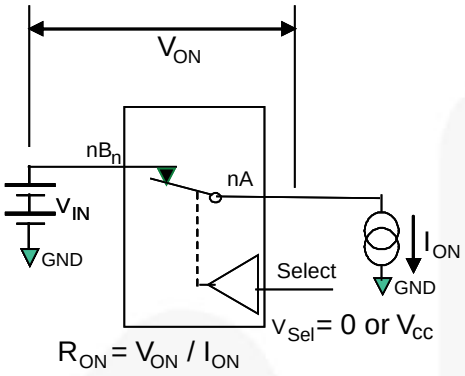
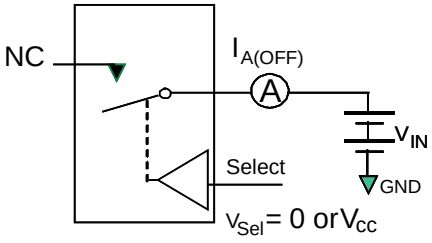


Figure 7. On Resistance



**Each switch port is tested separately.

Figure 8. Off Leakage

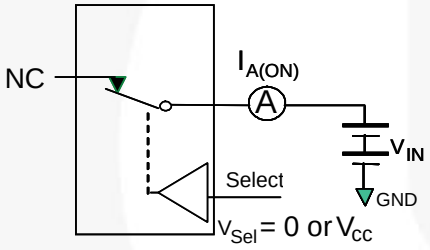


Figure 9. On Leakage

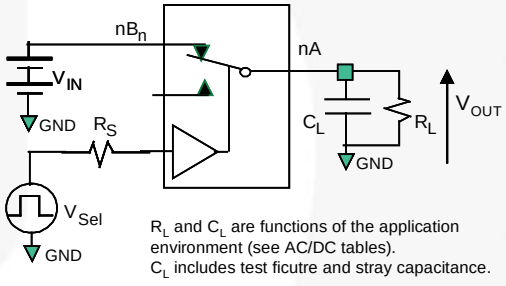


Figure 10. Test Circuit Load

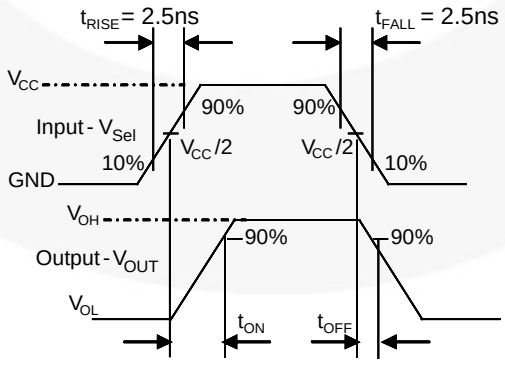
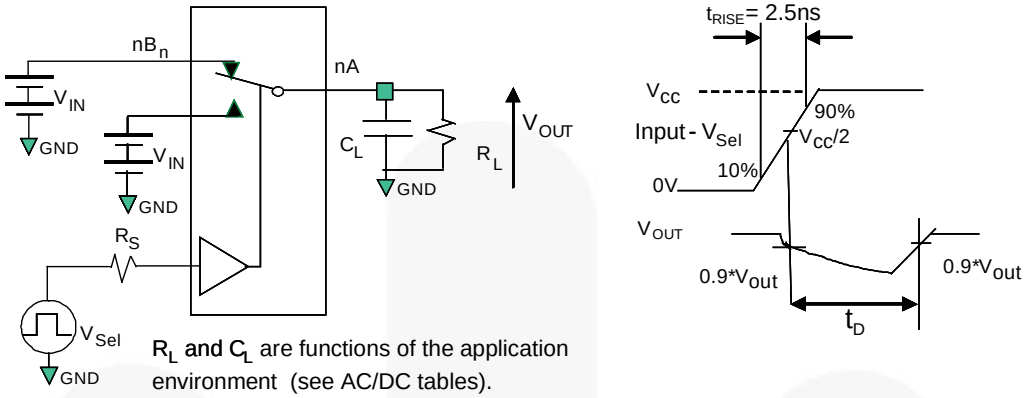


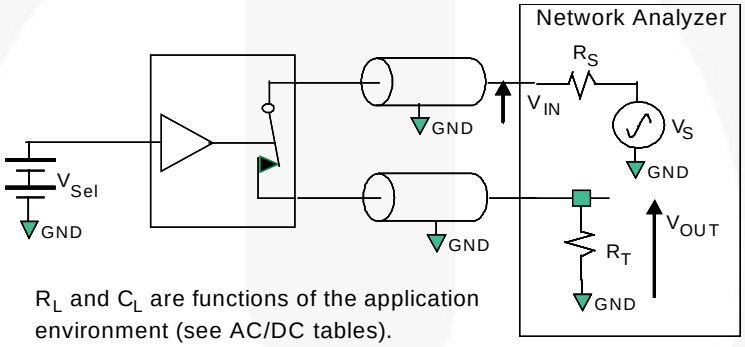
Figure 11. Turn-On / Turn-Off Waveforms

Test Diagrams (Continued)



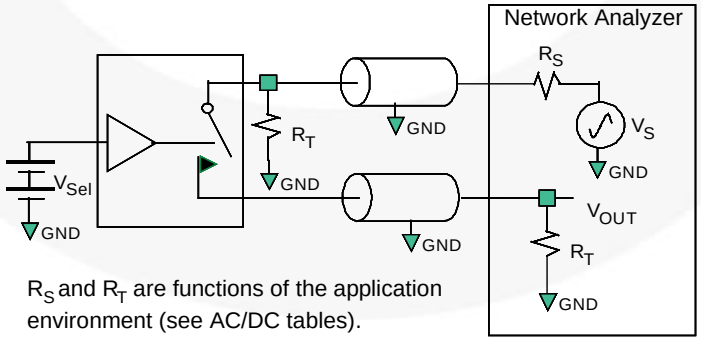
R_L and C_L are functions of the application environment (see AC/DC tables).
C_L includes test fixture and stray capacitance.

Figure 12. Break-Before-Make Interval Timing



R_L and C_L are functions of the application environment (see AC/DC tables).
C_L includes test fixture and stray capacitance.

Figure 13. Bandwidth



R_S and R_T are functions of the application environment (see AC/DC tables).

Off-Isolation = 20 Log (V_{OUT} / V_{IN})

Figure 14. Channel Off Isolation

Test Diagrams (Continued)

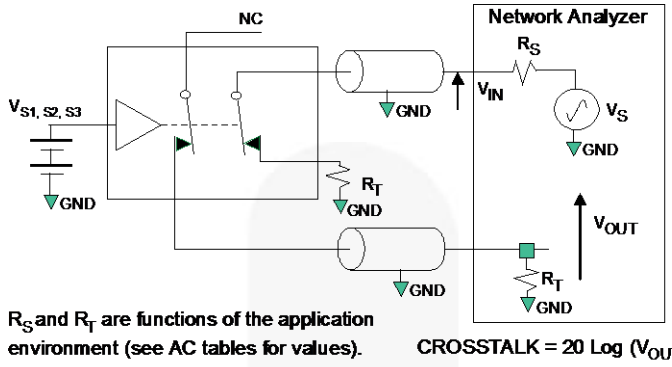


Figure 15. Adjacent Channel Crosstalk

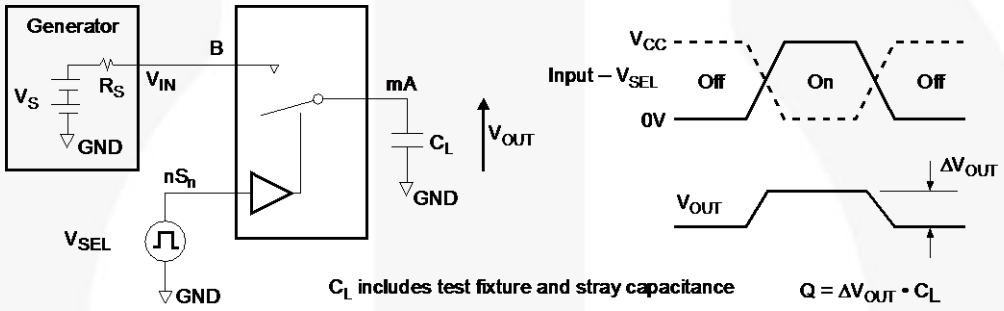


Figure 16. Charge Injection Test

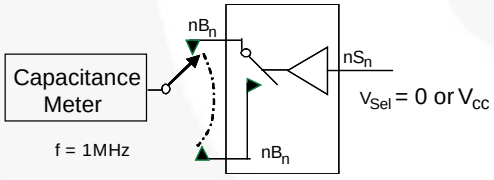


Figure 17. Channel Off Capacitance

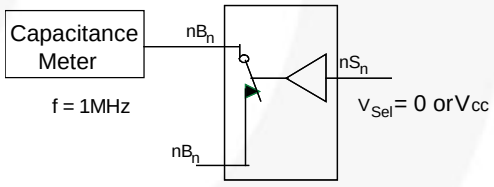
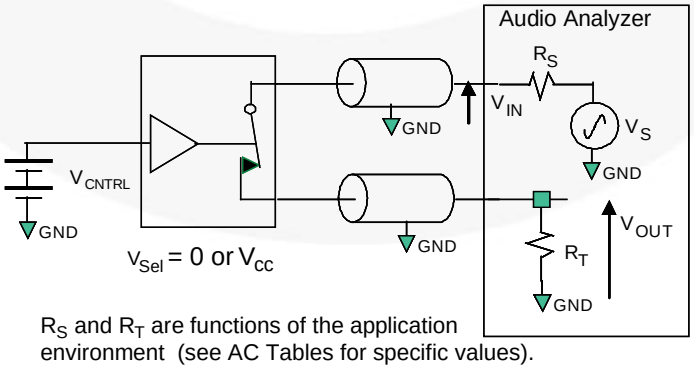


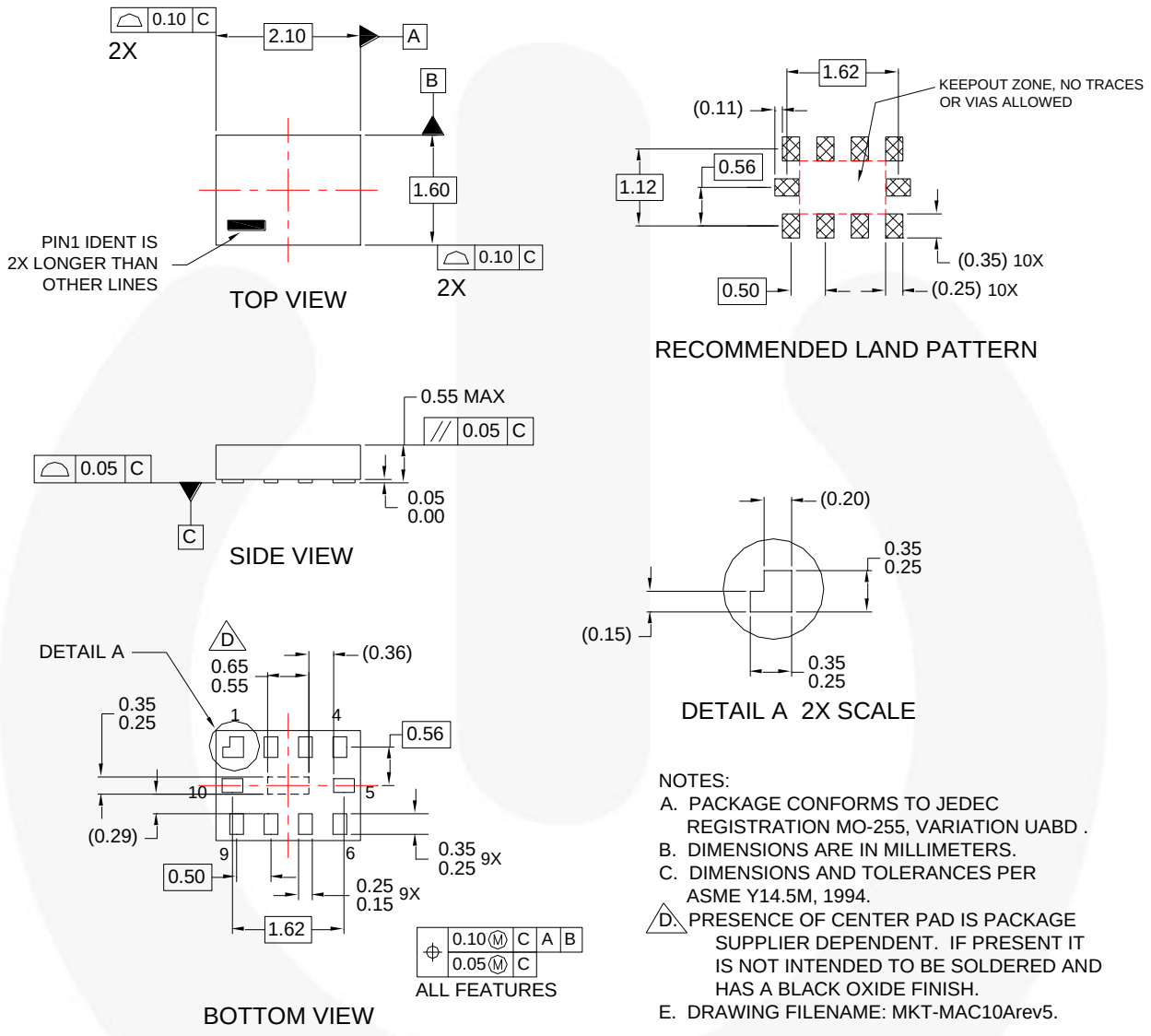
Figure 18. Channel On Capacitance



R_S and R_T are functions of the application environment (see AC Tables for specific values).

Figure 19. Total Harmonic Distortion

Physical Dimensions



NOTES:

A. PACKAGE CONFORMS TO JEDEC REGISTRATION MO-255, VARIATION UABD .

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.

D. PRESENCE OF CENTER PAD IS PACKAGE SUPPLIER DEPENDENT. IF PRESENT IT IS NOT INTENDED TO BE SOLDERED AND HAS A BLACK OXIDE FINISH.

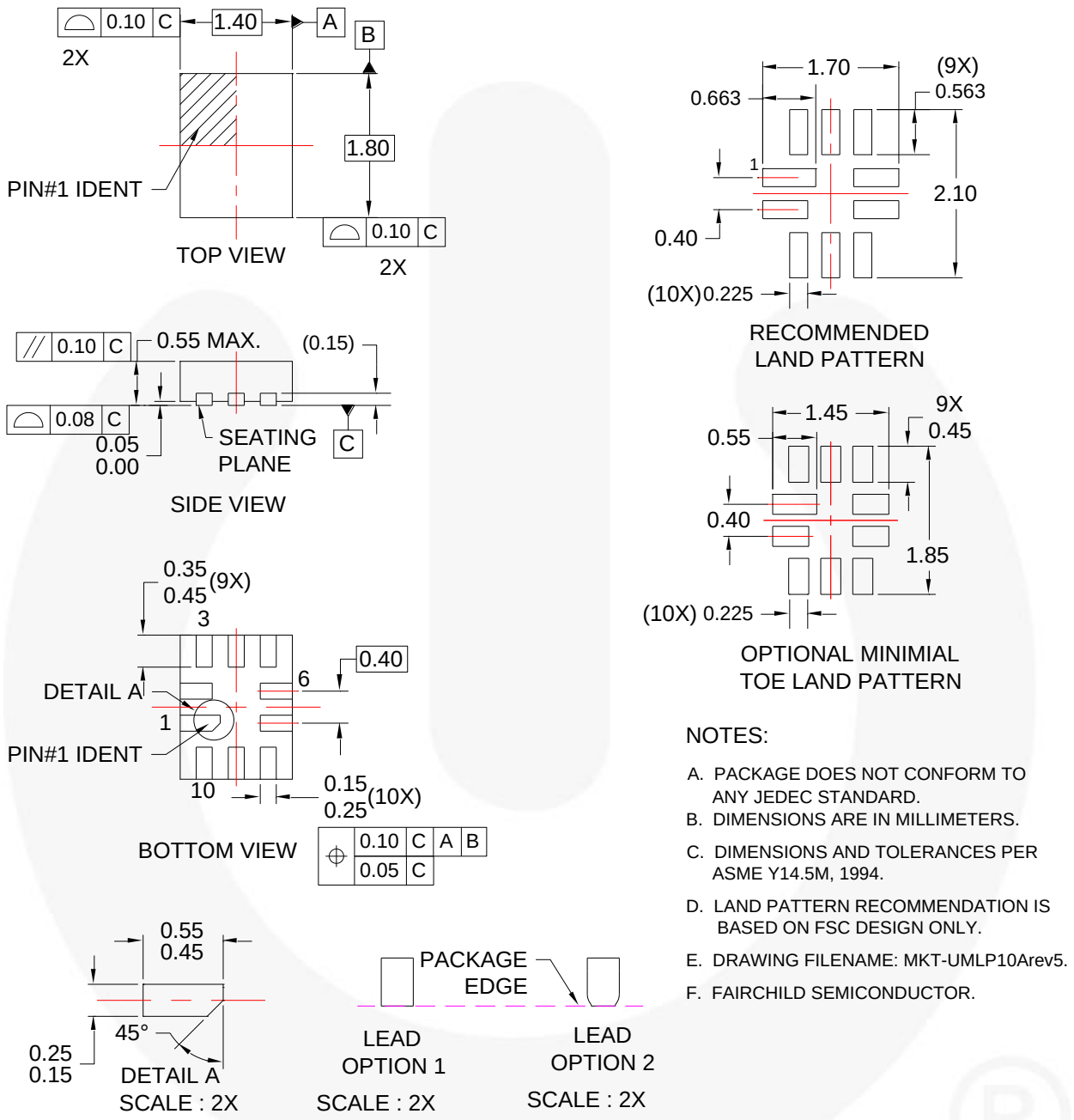
E. DRAWING FILENAME: MKT-MAC10Arev5.

Figure 20. 10-Lead MicroPak™

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:
http://www.fairchildsemi.com/packaging/.

Physical Dimensions (Continued)



NOTES:

A. PACKAGE DOES NOT CONFORM TO ANY JEDEC STANDARD.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
D. LAND PATTERN RECOMMENDATION IS BASED ON FSC DESIGN ONLY.
E. DRAWING FILENAME: MKT-UMLP10Arev5.
F. FAIRCHILD SEMICONDUCTOR.

Figure 21. 10-Lead, Quad Ultrathin Molded Leadless Package (UMLP)

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers F*airchild products.*

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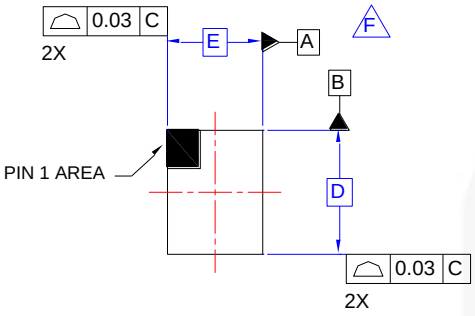
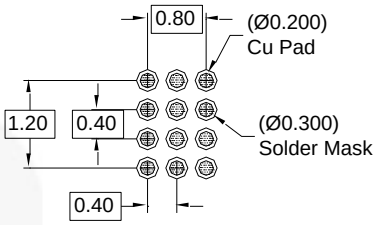
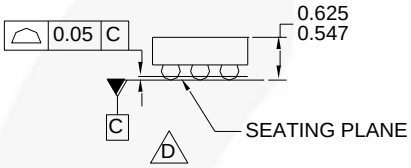
Physical Dimensions (Continued)

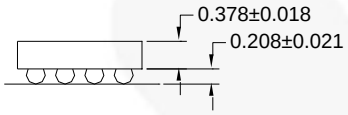


TOP VIEW

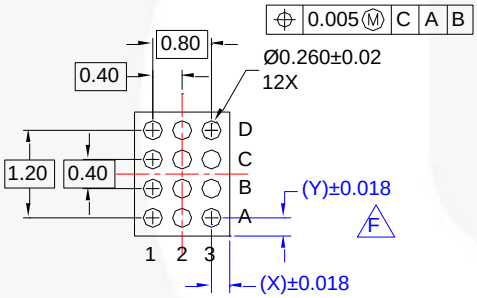


RECOMMENDED LAND PATTERN
(NSMD PAD TYPE)





SIDE VIEWS



BOTTOM VIEW

NOTES:

A. NO JEDEC REGISTRATION APPLIES.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.

D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E. PACKAGE NOMINAL HEIGHT IS 586 MICRONS ±39 MICRONS (547-625 MICRONS).

F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

G. DRAWING FILENAME: MKT-UC012ACrev1.

Product-Specific Dimensions

Product	D	E	X	Y
FSA2269UCX	1.560 mm	1.160 mm	0.180 mm	0.180 mm

Figure 22. 12-Ball, Wafer Level Chip-Scale Package (WLCSP)

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Definition of Terms

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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