March 2004

# FDP7045L/FDB7045L

## N-Channel Logic Level PowerTrench® MOSFET

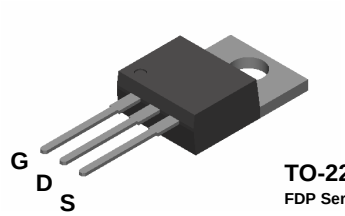
### General Description

This N-Channel Logic Level MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers.

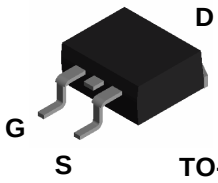
These MOSFETs feature faster switching and lower gate charge than other MOSFETs with comparable $R_{DS(ON)}$ specifications resulting in DC/DC power supply designs with higher overall efficiency.

### Features

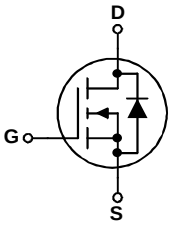
- 100 A, 30 V $R_{DS(ON)}$ = 4.5 mΩ @ $V_{GS}$ = 10 V
  $R_{DS(ON)}$ = 6.0 mΩ @ $V_{GS}$ = 4.5 V
- Critical DC electrical parameters specified at elevated temperature
- High performance trench technology for extremely low $R_{DS(ON)}$
- 175°C maximum junction temperature rating




**TO-220**
**FDP Series**




**TO-263AB**
**FDB Series**




## Absolute Maximum Ratings

$T_A$=25°C unless otherwise noted

| Symbol | Parameter | Ratings | Units |
|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | 30 | V |
| $V_{GSS}$ | Gate-Source Voltage | ± 20 | V |
| $I_D$ | Drain Current – Continuous (Note 1) | 100 | A |
| | | 75 | |
| | – Pulsed (Note 1) | 300 | |
| $P_D$ | Total Power Dissipation @ $T_C$ = 25°C | 107 | W |
| | Derate above 25°C | 0.7 | W/°C |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | –55 to +175 | °C |

## Thermal Characteristics

| | | | |
|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | 1.4 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | 62.5 | °C/W |

## Package Marking and Ordering Information

| Device Marking | Device | Reel Size | Tape width | Quantity |
|---|---|---|---|---|
| FDB7045L | FDB7045L | 13'' | 24mm | 800 units |
| FDP7045L | FDP7045L | Tube | n/a | 45 |

## Electrical Characteristics

$T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Drain-Source Avalanche Ratings (Note 1)** | | | | | | |
| $W_{DSS}$ | Single Pulse Drain-Source Avalanche Energy | $V_{DD}$ = 15 V, $I_D$ = 75 A | | | 330 | mJ |
| $I_{AR}$ | Maximum Drain-Source Avalanche Current | | | | 75 | A |
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain–Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = 250 µA | 30 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 µA, Referenced to 25°C | | 25 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 24 V, $V_{GS}$ = 0 V | | | 1 | µA |
| $I_{GSS}$ | Gate–Body Leakage | $V_{GS}$ = ± 20 V, $V_{DS}$ = 0 V | | | ± 100 | nA |
| **On Characteristics (Note 2)** | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 1 | 1.8 | 3 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate Threshold Voltage Temperature Coefficient | $I_D$ = 250 µA, Referenced to 25°C | | –6 | | mV/°C |
| $R_{DS(on)}$ | Static Drain–Source On–Resistance | $V_{GS}$ = 10 V, $I_D$ = 50 A<br>$V_{GS}$ = 4.5 V, $I_D$ = 40 A<br>$V_{GS}$= 10 V, $I_D$ = 50 A, $T_J$=125°C | | 3.5<br>4.0<br>5.5 | 4.5<br>6.0<br>7.0 | mΩ |
| $I_{D(on)}$ | On–State Drain Current | $V_{GS}$ = 10 V, $V_{DS}$ = 10 V | 50 | | | A |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 5V, $I_D$ = 50 A | | 165 | | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 15 V, $V_{GS}$ = 0 V, f = 1.0 MHz | | 4357 | | pF |
| $C_{oss}$ | Output Capacitance | | | 1092 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 399 | | pF |
| $R_G$ | Gate Resistance | $V_{GS}$ = 15 mV, f = 1.0 MHz | | 1.4 | | Ω |
| **Switching Characteristics (Note 2)** | | | | | | |
| $t_{d(on)}$ | Turn–On Delay Time | $V_{DD}$ = 15V, $I_D$ = 1 A, $V_{GS}$ = 10 V, $R_{GEN}$ = 6 Ω | | 16 | 29 | ns |
| $t_r$ | Turn–On Rise Time | | | 13 | 24 | ns |
| $t_{d(off)}$ | Turn–Off Delay Time | | | 74 | 119 | ns |
| $t_f$ | Turn–Off Fall Time | | | 41 | 66 | ns |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = 15 V, $I_D$ = 50 A, $V_{GS}$ = 5 V | | 41 | 58 | nC |
| $Q_{gs}$ | Gate–Source Charge | | | 12 | | nC |
| $Q_{gd}$ | Gate–Drain Charge | | | 14 | | nC |
| **Drain–Source Diode Characteristics and Maximum Ratings** | | | | | | |
| $I_S$ | Maximum Continuous Drain–Source Diode Forward Current | | | | 75 | A |
| $V_{SD}$ | Drain–Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 50 A (Note 1) | | 0.91 | 1.2 | V |
| $t_{rr}$ | Diode Reverse Recovery Time | $I_F$ = 50 A, $d_{iF}/d_t$ = 100 A/µs | | 48 | | nS |
| $Q_{rr}$ | Diode Reverse Recovery Charge | | | 42 | | nC |

**Notes:**

1. Calculated continuous current based on maximum allowable junction temperature. Actual maximum continuous current limited by package constraints to 75A.
2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

## Typical Characteristics

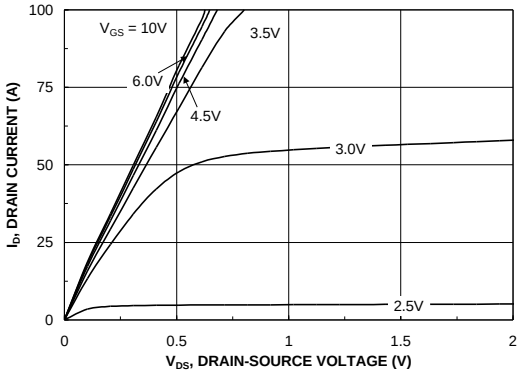



**Figure 1. On-Region Characteristics.**

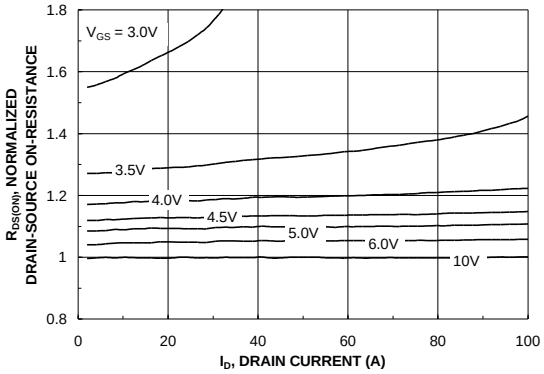



**Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.**

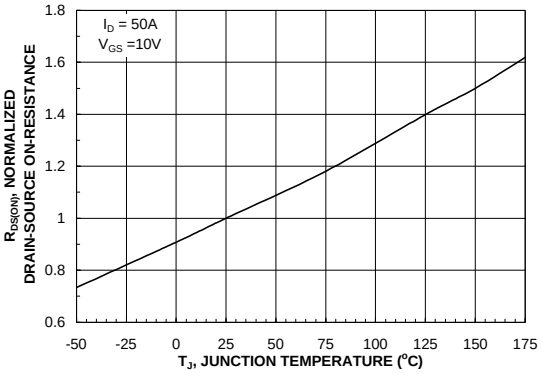



**Figure 3. On-Resistance Variation with Temperature.**

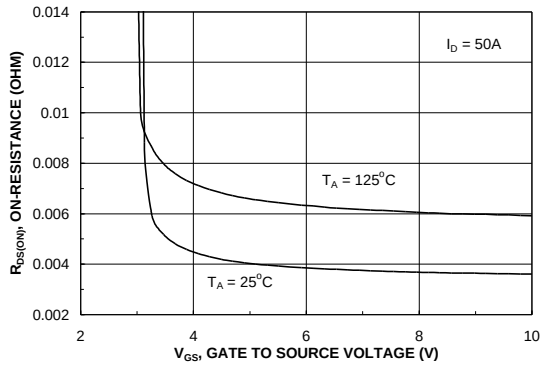



**Figure 4. On-Resistance Variation with Gate-to-Source Voltage.**

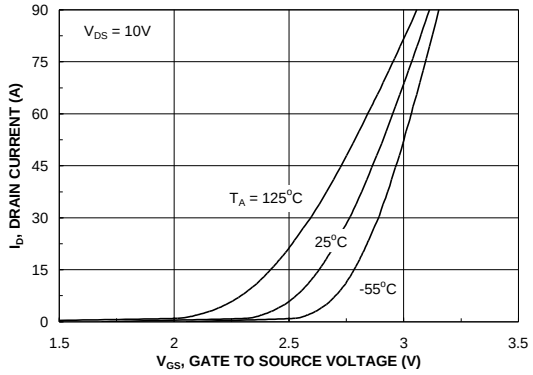



**Figure 5. Transfer Characteristics.**

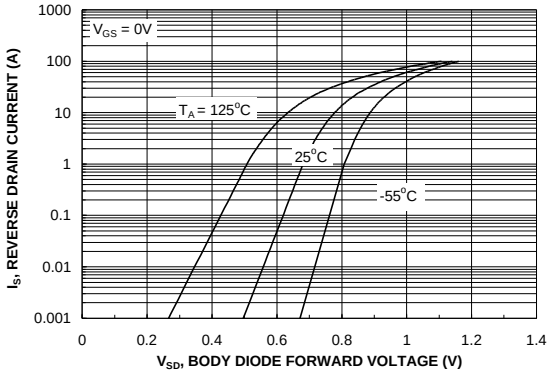



**Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.**

## Typical Characteristics

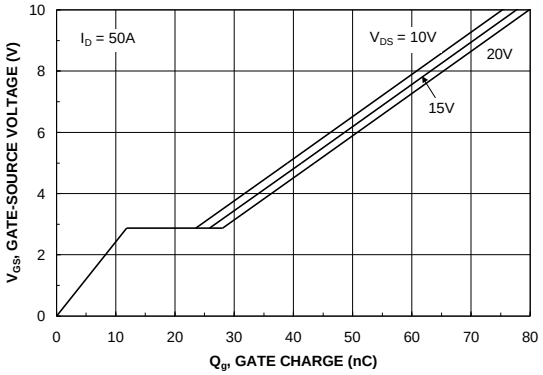



**Figure 7. Gate Charge Characteristics.**

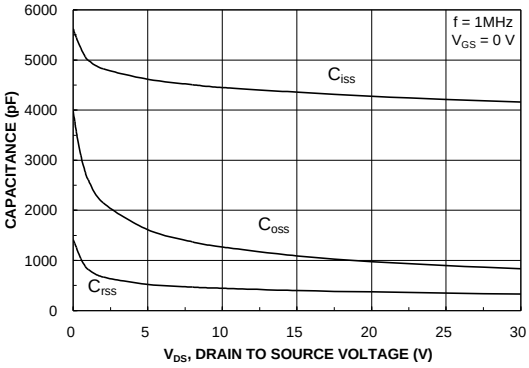



**Figure 8. Capacitance Characteristics.**

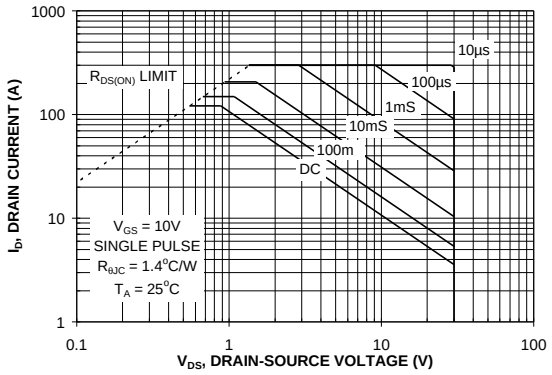



**Figure 9. Maximum Safe Operating Area.**

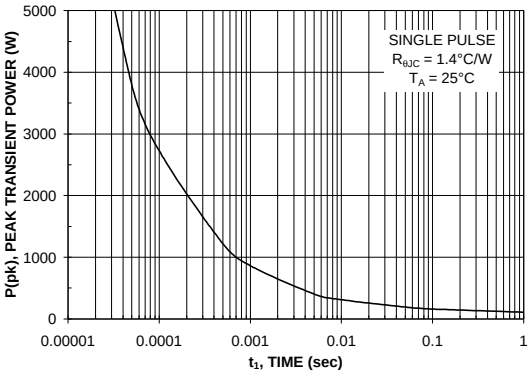



**Figure 10. Single Pulse Maximum Power Dissipation.**

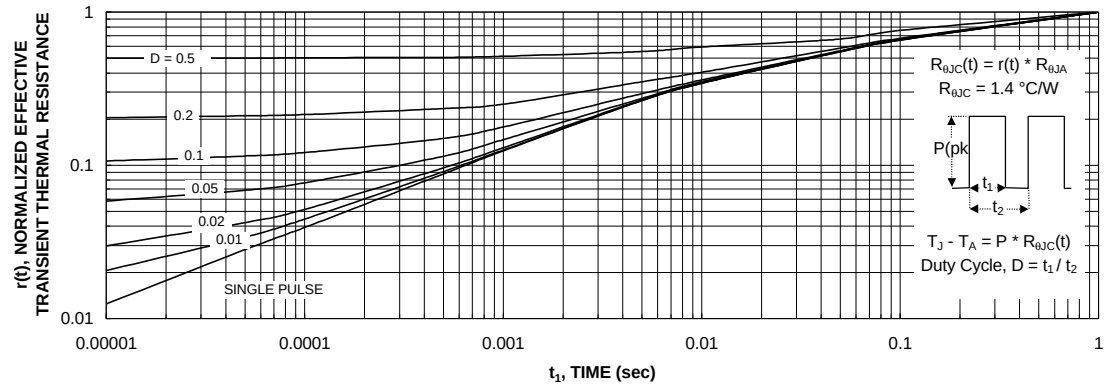



**Figure 11. Transient Thermal Response Curve.**

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