

74F640 • 74F645 Octal Bus Transceiver with 3-STATE Outputs

General Description

These devices are octal bus transceivers designed for asynchronous two-way data flow between the A and B busses. Both busses are capable of sinking 64 mA, have 3-STATE outputs, and a common output enable pin. The direction of data flow is determined by the transmit/receive (T/\bar{R}) input. The 'F645 is a high speed/low power version of the 'F245. The 'F640 is an inverting option of the 'F645.

- Outputs sink 64 mA
- Transmit/receive (T/\bar{R}) input controls the direction of data flow
- Guaranteed 4000V minimum ESD protection
- 'F645 is a lower power, faster version of the 'F245
- 'F640 is an inverting option of the 'F645

Features

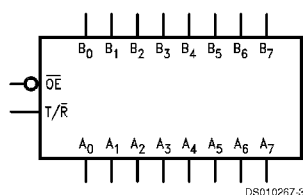
- Designed for asynchronous two-way data flow between busses

Ordering Code:

Commercial	Package Number	Package Description
74F640PC	N20A	20-Lead (0.300" Wide) Molded Dual-In-Line
74F640SC (Note 1)	M20B	20-Lead (0.300" Wide) Molded Small Outline, JEDEC
74F645PC	N20A	20-Lead (0.300" Wide) Molded Dual-In-Line

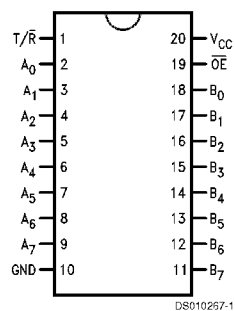
Note 1: Devices also available in 13" reel. Use suffix = SCX.

Logic Symbol



Connection Diagram

Pin Assignment for DIP and SOIC



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Unit Loading/Fan Out

Pin Names	Description	74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
\overline{OE}	Output Enable Input (Active LOW)	1.0/1.0	20 μA / -0.6 mA
T/\overline{R}	Transmit/Receive Input	1.0/1.0	20 μA / -0.6 mA
A_0 - A_7	Side A Inputs or 3-STATE Outputs	3.5/0.667 600/106.6	70 μA / -0.4 mA -12 mA / 64 mA
B_0 - B_7	Side B Inputs or 3-STATE Outputs	3.5/0.667 600/106.6	70 μA / -0.4 mA -12 mA / 64 mA

Functional Description

The output enable (\overline{OE}) is active LOW. If the device is disabled (\overline{OE} HIGH), the outputs are in the high impedance state. The transmit/receive input (T/\overline{R}) controls whether data

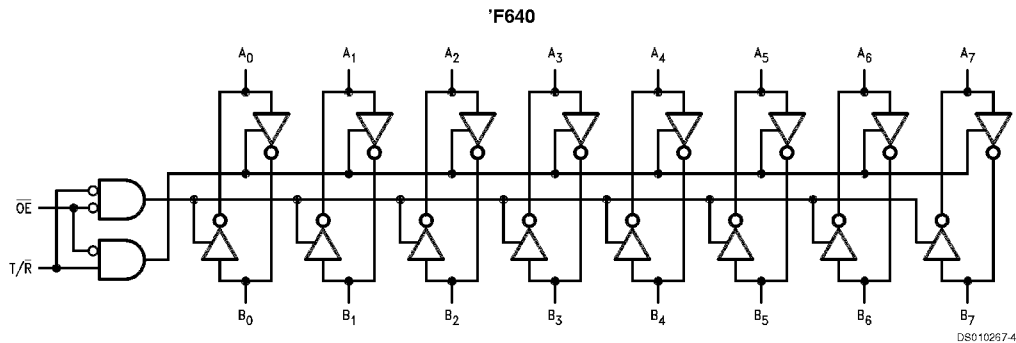
is transmitted from the A bus to the B bus or from the B bus to the A bus. When T/\overline{R} is LOW, B data is sent to the A bus. If T/\overline{R} is HIGH, A data is sent to the B bus.

Function Table

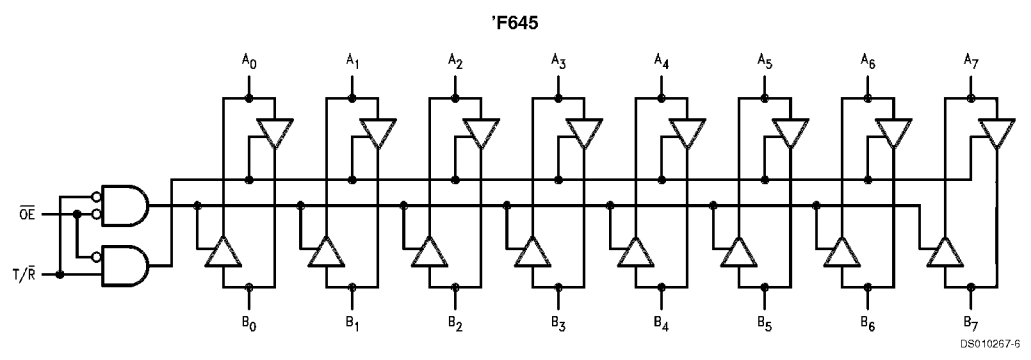
Inputs		Outputs	
\overline{OE}	T/\overline{R}	'F640	'F645
L	L	Bus \overline{B} data to Bus A	Bus B data to Bus A
L	H	Bus \overline{A} data to Bus B	Bus A data to Bus B
H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance state

Logic Diagrams



Logic Diagrams (Continued)



Absolute Maximum Ratings (Note 2)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
Plastic	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 3)	-0.5V to +7.0V
Input Current (Note 3)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}
3-STATE Output	-0.5V to +5.5V
Current Applied to Output	

in LOW State (Max) twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min) 4000V

Recommended Operating Conditions

Free Air Ambient Temperature	
Commercial	0°C to +70°C
Supply Voltage	
Commercial	+4.5V to +5.5V

Note 2: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 3: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

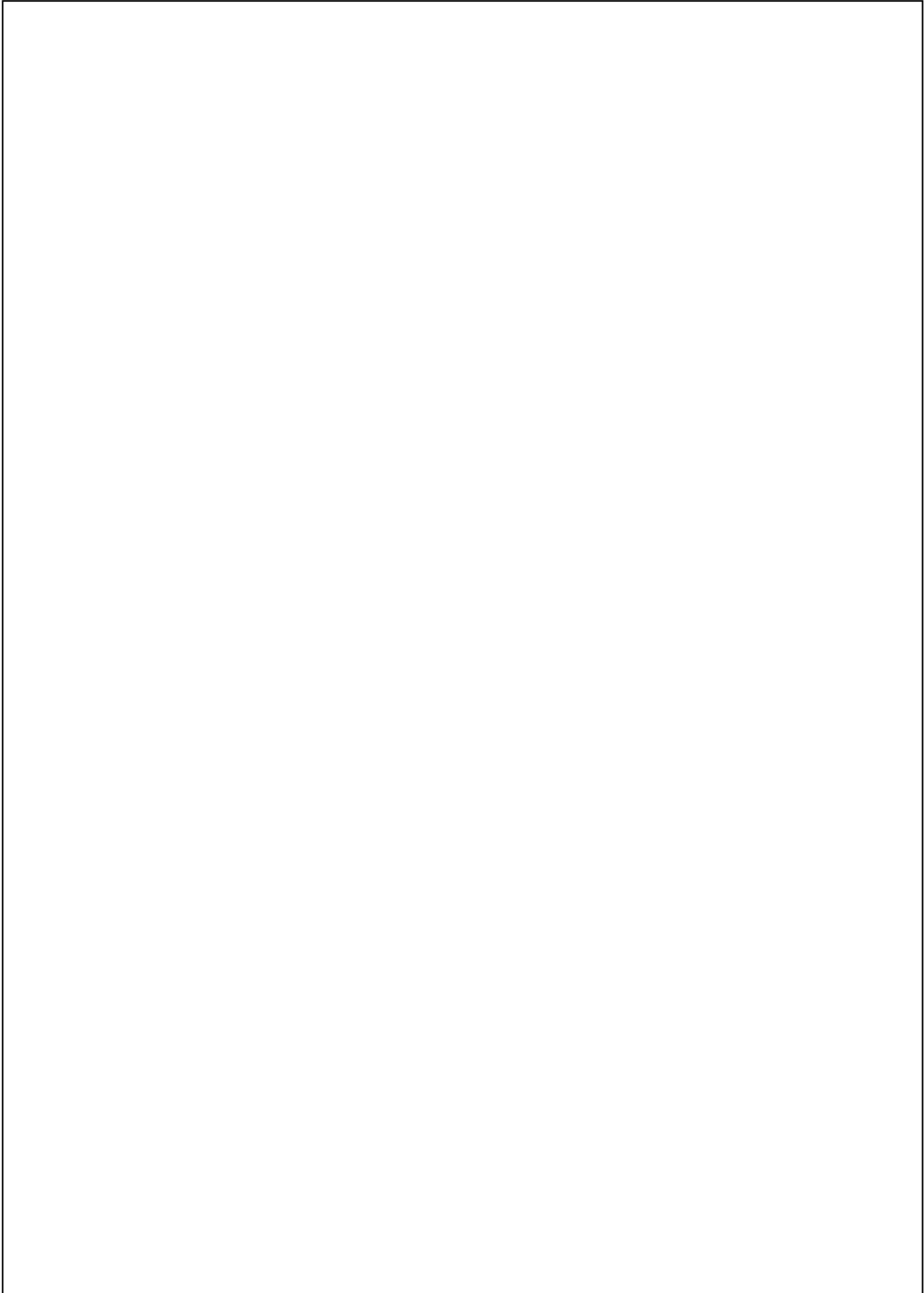
Symbol	Parameter	74F			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage	0.8			V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage	-1.2			V	Min	I _{IN} = -18 mA (Non I/O Pins)
V _{OH}	Output HIGH Voltage	74F 10% V _{CC}	2.0		V	Min	I _{OH} = -15 mA (A _n , B _n)
V _{OL}	Output LOW Voltage	74F 10% V _{CC}	0.55		V	Min	I _{OL} = 64 mA (A _n , B _n)
I _{IH}	Input HIGH Current	74F	5.0		μA	Max	V _{IN} = 2.7V (Non I/O Pins)
I _{BVI}	Input HIGH Current Breakdown Test	74F	7.0		μA	Max	V _{IN} = 7.0V (Non I/O Pins)
I _{BVIT}	Input HIGH Current Breakdown (I/O)	74F	0.5		mA	Max	V _{IN} = 5.5V (A _n , B _n)
I _{CEX}	Output HIGH Leakage Current	74F	50		μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	74F	4.75		V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current	74F	3.75		μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current		-0.6		mA	Max	V _{IN} = 0.5V (Non I/O Pins)
I _{IH} + I _{OZH}	Output Leakage Current		70		μA	Max	V _{OUT} = 2.7V (A _n , B _n)
I _{IL} + I _{OZL}	Output Leakage Current		-650		μA	Max	V _{OUT} = 0.5V (A _n , B _n)
I _{OS}	Output Short-Circuit Current		-100	-225	mA	Max	V _{OUT} = 0V
I _{ZZ}	Bus Drainage Test		500		μA	0.0V	V _{OUT} = 5.25
I _{CCH}	Power Supply Current ('F640)		80		mA	Max	V _O = HIGH, V _{IN} = 0.2V
I _{CCL}	Power Supply Current ('F640)		80		mA	Max	V _O = LOW
I _{CCZ}	Power Supply Current ('F640)		96		mA	Max	V _O = HIGH Z
I _{CCH}	Power Supply Current ('F645)		65		mA	Max	V _O = HIGH
I _{CCL}	Power Supply Current ('F645)		80		mA	Max	V _O = LOW, V _{IN} = 0.2V
I _{CCZ}	Power Supply Current ('F645)		90		mA	Max	V _O = HIGH Z

'F640 AC Electrical Characteristics:

Symbol	Parameter	74F			74F		Units
		T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A , V _{CC} = Com C _L = 50 pF		
		Min	Typ	Max	Min	Max	
t _{PLH}	Propagation Delay	2.5		7.5	2.0	8.0	ns
t _{PHL}	A Input to B Output	2.0		7.0	2.0	7.0	
t _{PLH}	Propagation Delay	2.5		7.5	2.0	8.0	ns
t _{PHL}	B Input to A Output	2.0		7.0	2.0	7.0	
t _{PZH}	Enable Time	2.5		7.5	2.0	9.0	ns
t _{PZL}	\overline{OE} Input to A Output	2.5		8.0	2.0	8.5	
t _{PHZ}	Disable Time	1.5		7.0	1.0	7.5	
t _{PLZ}	\overline{OE} Input to A Output	1.5		6.0	1.5	6.0	ns
t _{PZH}	Enable Time	2.5		7.5	2.0	9.0	
t _{PZL}	\overline{OE} Input to B Output	2.5		8.0	2.0	8.5	
t _{PHZ}	Disable Time	1.5		7.0	1.0	7.5	ns
t _{PLZ}	\overline{OE} Input to B Output	1.5		6.0	1.5	6.0	

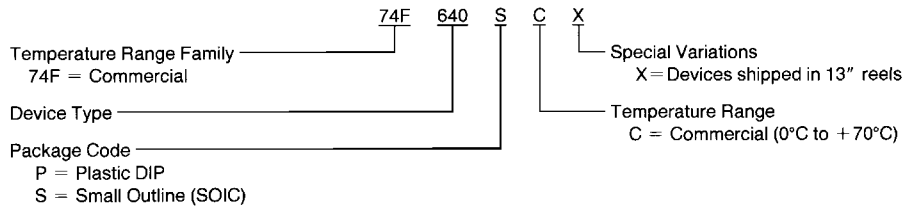
'F645 AC Electrical Characteristics:

Symbol	Parameter	74F			74F		Units
		T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A , V _{CC} = Com C _L = 50 pF		
		Min	Typ	Max	Min	Max	
t _{PLH}	Propagation Delay	1.5		6.0	1.5	7.0	ns
t _{PHL}	A Input to B Output	2.0		7.0	2.0	7.5	
t _{PLH}	Propagation Delay	1.5		6.0	1.5	7.0	ns
t _{PHL}	B Input to A Output	2.0		7.0	2.0	7.5	
t _{PZH}	Enable Time	2.5		8.0	2.0	9.0	ns
t _{PZL}	\overline{OE} Input to A Output	2.5		8.5	2.0	8.5	
t _{PHZ}	Disable Time	1.5		7.0	1.0	8.0	
t _{PLZ}	\overline{OE} Input to A Output	1.0		5.5	1.0	5.5	ns
t _{PZH}	Enable Time	2.5		7.5	2.0	9.5	
t _{PZL}	\overline{OE} Input to B Output	2.5		8.5	2.5	9.0	
t _{PHZ}	Disable Time	1.5		6.5	1.0	7.5	ns
t _{PLZ}	\overline{OE} Input to B Output	1.0		5.5	1.0	5.5	



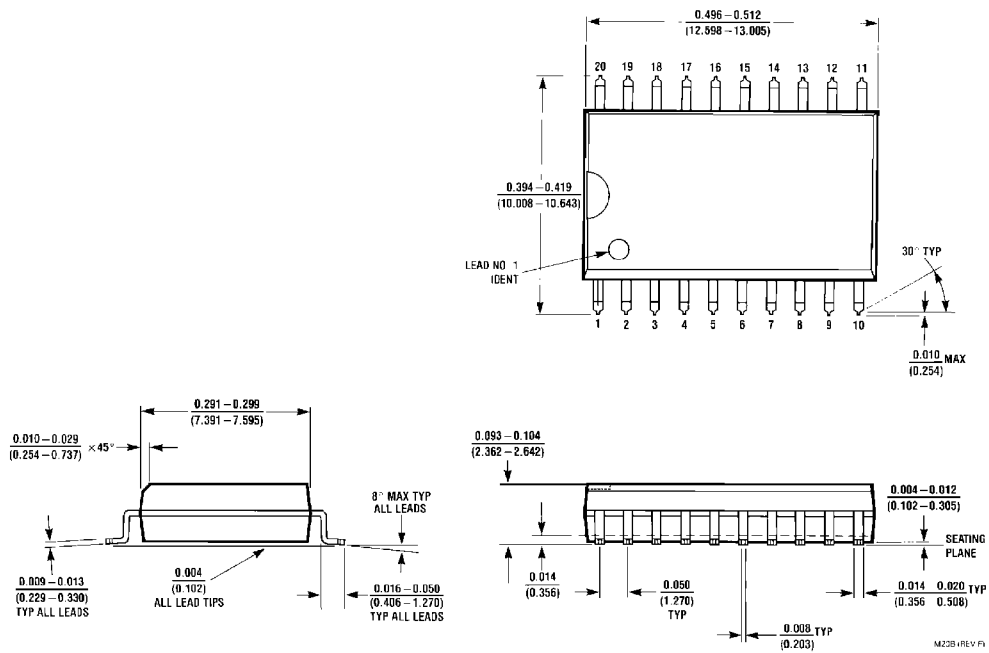
Ordering Information

The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:



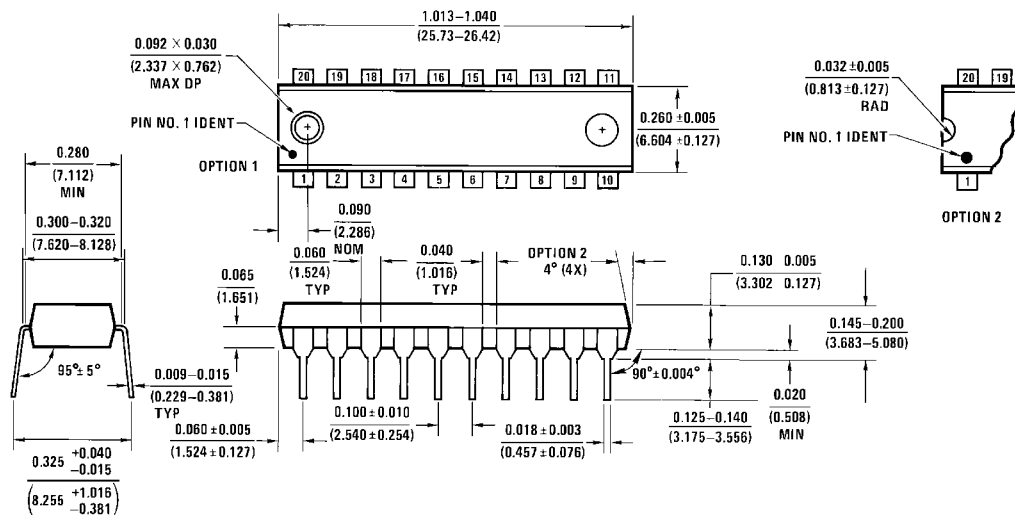
DS010267-7

Physical Dimensions inches (millimeters) unless otherwise noted



20-Lead (0.300" Wide) Molded Small Outline Package, JEDEC (S)
 Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



N20A (REV G)

**20-Lead (0.300" Wide) Molded Dual-In-Line Package (P)
Package Number N20A**

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Fairchild Semiconductor Corporation
Americas
Customer Response Center
Tel: 1-888-522-5372

Fairchild Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 8 141-35-0
English Tel: +44 (0) 1 793-85-68-56
Italy Tel: +39 (0) 2 57 5631

Fairchild Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: +852 2737-7200
Fax: +852 2314-0061

National Semiconductor Japan Ltd.
Tel: 81-3-5620-6175
Fax: 81-3-5620-6179

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