50MHz, Zero-Crossover, Low-Distortion, High CMRR, RRI/O, Single-Supply Operational Amplifier

1 FEATURES

- **GAIN BANDWIDTH:50MHz**
- **Zero-Crossover Distortion Topology:**
  CMRR: 100 dB (TYP)
- **Rail-to-Rail Input and Output**
- **Low Noise: 4.4uVpp at 0.1Hz ~10Hz**
- **Slew Rate: 40V/µs**
- **Fast Settling: 270ns to 0.01%**
- **Precision:**
  Low Offset: 100uV (TYP)
  Low Input Bias Current: 50pA (TYP)
- **SUPPLY RANGE: +2.2V to +5.5V**
- **SPECIFIED UP TO +125°C**
- **Micro SIZE PACKAGES: SOT23-5、SOIC-8(SOP8)、MSOP-8、SOIC-14(SOP14)**

2 APPLICATIONS

- **Signal Conditioning**
- **Data Acquisition**
- **Process Control**
- **Active Filters**
- **Test Equipment**
- **Audio**
- **Wideband Amplifiers**

3 DESCRIPTIONS

The RS870X zero-crossover series, rail-to-rail, high performance, CMOS operational amplifiers are optimized for very low voltage, single-supply applications. Rail-to-rail input or output, low-noise (4.4uVpp) and high-speed operation (50MHz Gain Bandwidth) make these devices ideal for driving sampling analog-to-digital converters (ADCs). Applications include audio, signal conditioning, and sensor amplification. The RS870X family of op amps are also well-suited for cell phone power amplifier control loops.

Special features include an excellent common-mode rejection ratio (CMRR), no input stage crossover distortion, high input impedance, and rail-to-rail input and output swing. The input common-mode range includes both the negative and positive supplies.

The devices are ideal for sensor interfaces, active filters and portable applications. The RS870X families of operational amplifiers are specified at the full temperature range of -40°C to +125°C under single or dual power supplies of 2.2V to 5.5V.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS8701	SOT23-5	2.92mm×1.62mm
RS8702	SOIC-8(SOP8)	4.90mm×3.90mm
	MSOP-8	3.00mm×3.00mm
RS8704	SOIC-14 (SOP14)	8.65mm×3.90mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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4 Revision History

Note: Page numbers for previous revisions may different from page numbers in the current version.

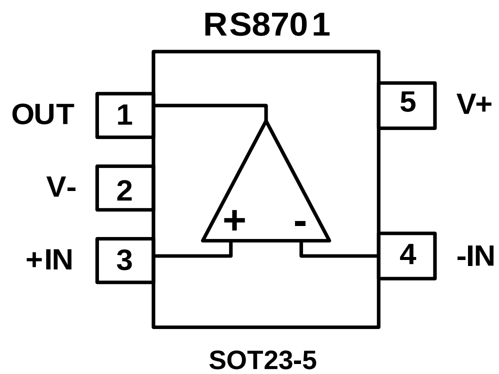
Version	Change Date	Change Item
A.0	2022/04/13	Initial version completed
A.1	2022/10/20	Update ELECTRICAL CHARACTERISTICS and TYPICAL CHARACTERISTICS
A.2	2023/03/08	1.Update ELECTRICAL CHARACTERISTICS 2.Add Open-Loop Gain and Phase vs Frequency curve in 7.5 TYPICAL CHARACTERISTICS
A.3	2023/06/07	Add RS8701XF and RS8704XP ORDERING NUMBER

5 PACKAGE/ORDERING INFORMATION [1]

PRODUCT	ORDERING NUMBER	TEMPERATURE RANGE	PACKAGE LEAD	PACKAGE MARKING [2]	PACKAGE OPTION
RS870X	RS8701XF	-40°C ~125°C	SOT23-5	8701	Tape and Reel,3000
	RS8702XK	-40°C ~125°C	SOIC-8(SOP8)	RS8702	Tape and Reel,4000
	RS8702XM	-40°C ~125°C	MSOP-8	RS8702	Tape and Reel,4000
	RS8704XP	-40°C ~125°C	SOIC-14(SOP14)	RS8704	Tape and Reel,4000

NOTE:
(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.
(2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

6 Pin Configuration and Functions (Top View)



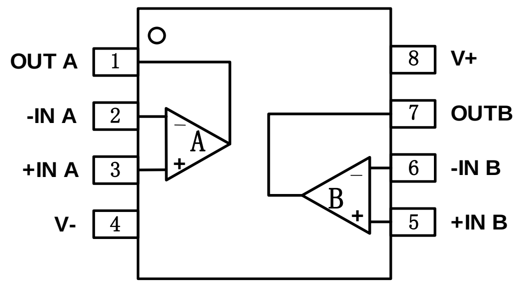
Pin Description

NAME	PIN RS8701 SOT23-5	I/O (1)	DESCRIPTION
-IN	4	I	Negative (inverting) input
+IN	3	I	Positive (noninverting) input
OUT	1	O	Output
V-	2	-	Negative (lowest) power supply
V+	5	-	Positive (highest) power supply

(1) I = Input, O = Output.

Pin Configuration and Functions (Top View)

RS8702



SOIC-8(SOP8)/MSOP-8

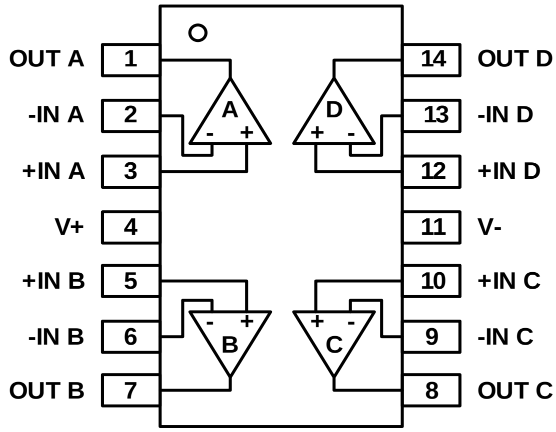
Pin Description

NAME	PIN	I/O (1)	DESCRIPTION
	RS8702		
	SOIC-8(SOP8)/MSOP-8		
-INA	2	I	Inverting input, channel A
+INA	3	I	Noninverting input, channel A
-INB	6	I	Inverting input, channel B
+INB	5	I	Noninverting input, channel B
OUTA	1	O	Output, channel A
OUTB	7	O	Output, channel B
V-	4	-	Negative (lowest) power supply
V+	8	-	Positive (highest) power supply

(1) I = Input, O = Output.

Pin Configuration and Functions (Top View)

RS8704



SOIC-14(SOP14)

Pin Description

NAME	PIN	I/O [(1)]	DESCRIPTION
	SOIC-14(SOP14)		
-INA	2	I	Inverting input, channel A
+INA	3	I	Noninverting input, channel A
-INB	6	I	Inverting input, channel B
+INB	5	I	Noninverting input, channel B
-INC	9	I	Inverting input, channel C
+INC	10	I	Noninverting input, channel C
-IND	13	I	Inverting input, channel D
+IND	12	I	Noninverting input, channel D
OUTA	1	O	Output, channel A
OUTB	7	O	Output, channel B
OUTC	8	O	Output, channel C
OUTD	14	O	Output, channel D
V-	11	-	Negative (lowest) power supply
V+	4	-	Positive (highest) power supply

(1) I = Input, O = Output.

7 SPECIFICATIONS

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
Voltage	Supply, V_S=(V+) - (V-)			5.5	V
	Signal input pin (2)		-0.5	+0.5	
Current	Signal input pin (2)		-10	10	mA
	Output short-circuit (3)		Continuous		
θ_{JA}	Package thermal impedance (4)	SOT23-5		230	°C/W
		SOIC-8(SOP8)		110	
		MSOP-8		165	
		SOIC-14(SOP14)		105	
Temperature	Operating range, T_A		-40	125	°C
	Junction, T_J (5)		-40	150	
	Storage, T_{stg}		-65	150	

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current-limited to 10mA or less.
(3) Short-circuit to ground, one amplifier per package.
(4) The package thermal impedance is calculated in accordance with JESD-51.
(5) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

7.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	
		Machine Model (MM)	±400	

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
Supply voltage，V_S= (V+) - (V-）	Single-supply	2.2		5.5	V
Operating range, T_A		-40		125	°C

7.4 ELECTRICAL CHARACTERISTICS

(At T_A = +25°C, V_S=2.2V to 5.5V, V_{CM}=V_S/2, V_{OUT}=0V and R_L = 10kΩ connected to 0V, FULL(9)=-40°C ~+125°C, unless otherwise noted.) (1)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN(2)	TYP(3)	MAX(2)	UNIT
POWER SUPPLY							
Operating Voltage Range	V_S		FULL	2.2		5.5	V
Quiescent Current/Amplifier	I_Q	I_{OUT}=0mA	25°C		7	10	mA
			FULL			12	
INPUT CHARACTERISTICS							
Input Offset Voltage	V_{OS}	V_{CM}= V_S/2	25°C	-200	±100	200	uV
Input Offset Voltage Average Drift	V_{OS} T_C		FULL		±1.6		uV/°C
Power-Supply Rejection Ratio	PSRR	V_S=2.2V to 5.5V	25°C	85	107		dB
			FULL		103		
Input Bias Current (4) (5)	I_B		25°C		50	500	pA
			FULL		500		pA
Input Offset Current (4)	I_{OS}		25°C		50	500	pA
			FULL		500		pA
Common-Mode Voltage Range	V_{CM}		FULL	(V-)		(V+)+0.1	V
Common-Mode Rejection Ratio	CMRR	V_S= 5.5V, (V-)<V_{CM}<(V+)	25°C	85	100		dB
			FULL		100		
Open-Loop Voltage Gain	A_{OL}	V_S= 5V, R_L=10KΩ, Vo=(V-)+0.15V to (V+)-0.15V	25°C	101	124		dB
			FULL		120		
NOISE PERFORMANCE							
Input Voltage Noise	e_{np-p}	f= 0.1Hz to 10Hz	25°C		4.4		μV_{PP}
Input Voltage Noise Density (4)	e_n	f = 100KHz	25°C		4		$nV/\sqrt{HZ}$
DYNAMIC PERFORMANCE							
Slew Rate (8)	SR	G=+1	25°C		40		V/us
Gain-Bandwidth Product	GBP	V_{IN} = 50mV_{P-P}	25°C		50		MHz
Phase Margin (4)	φ_O	V_{OUT} = 100mV_{P-P}, C_L = 70pF	25°C		60		°
Settling Time,0.01%	t_S	V_S = 5V, V_{PP}=4V, G = +1, C_L=100PF	25°C		270		ns
Overload Recovery Time	t_{OR}	V_{IN} × G ≥ V_S	25°C		54		ns
OUTPUT CHARACTERISTICS							
Output Voltage Swing from Rail	V_{OH}	V_S=5V, R_L=10 KΩ	25°C		7	16	mV
	V_{OL}		25°C		21	30	
Output Source Current (6) (7)	I_{SOURCE}	V_S = 5V	25°C	90	150		mA
Output Sink Current (6) (7)	I_{SINK}			50	118		

NOTE:

(1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.
(4) This parameter is ensured by design and/or characterization and is not tested in production.
(5) Positive current corresponds to current flowing into the device.
(6) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{θJA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is PD = ($T_{J(MAX)}$ - T_A) / $R_{θJA}$. All numbers apply for packages soldered directly onto a PCB.
(7) Short circuit test is a momentary test.
(8) Number specified is the slower of positive and negative slew rates.
(9) Specified by characterization only.

7.5 TYPICAL CHARACTERISTICS

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At T_A = +25°C, V_S=5V, unless otherwise noted.

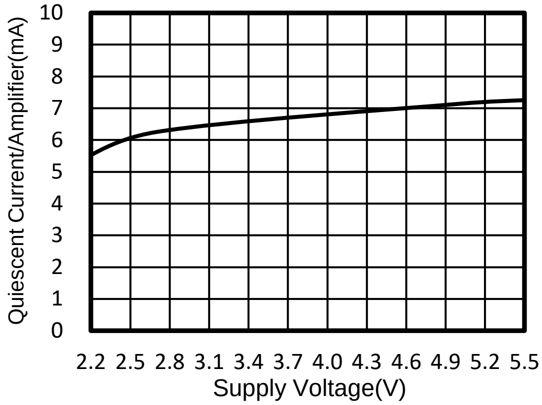


Figure 1. Quiescent Current vs Supply Voltage

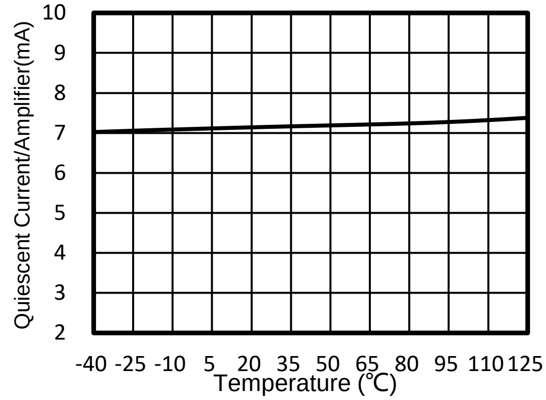


Figure 2. Quiescent Current vs Temperature

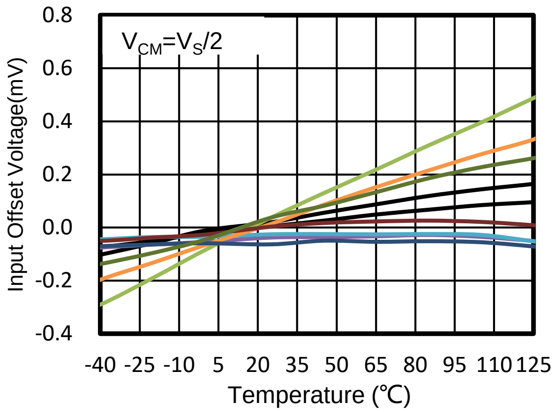


Figure 3. Input Offset Voltage vs Temperature

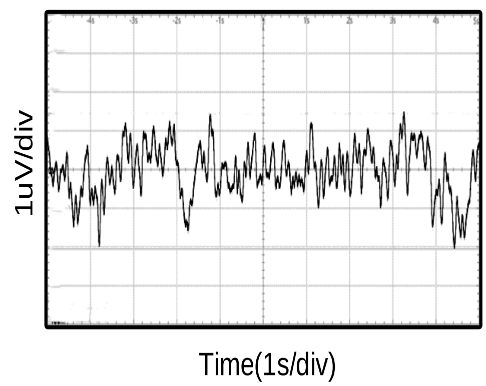


Figure 4. 0.1HZ to 10HZ Input Voltage Noise

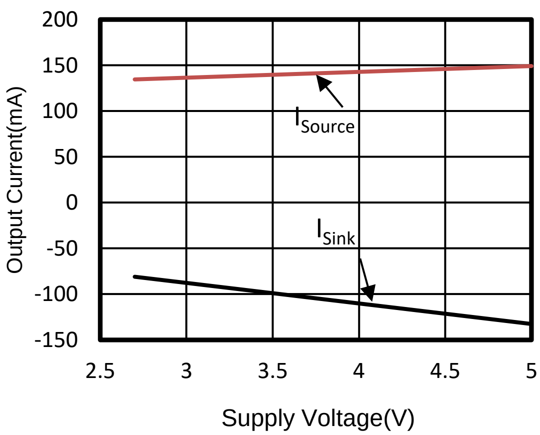


Figure 5. Supply Voltage vs Output Current

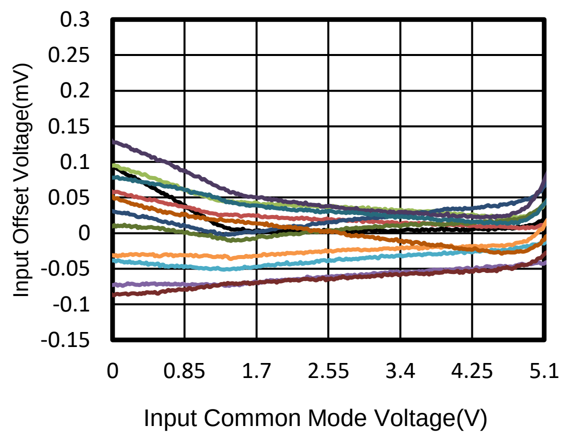


Figure 6. Input Offset Voltage vs Input Common Mode Voltage

TYPICAL CHARACTERISTICS

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At T_A = +25°C, V_S=5V, unless otherwise noted.

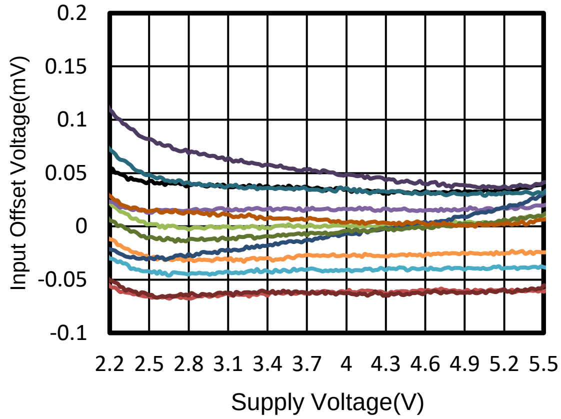


Figure 7. Input Offset Voltage vs Supply Voltage

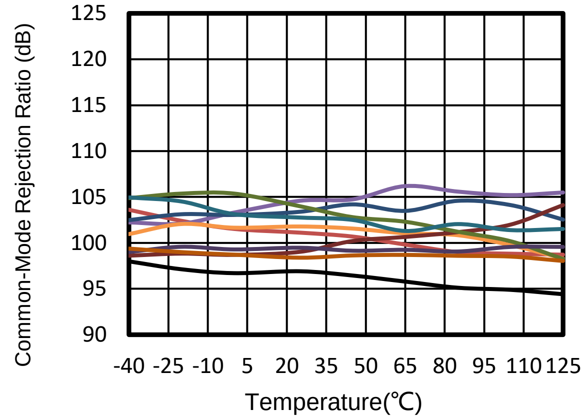


Figure 8. Common-Mode Rejection Ratio vs Temperature

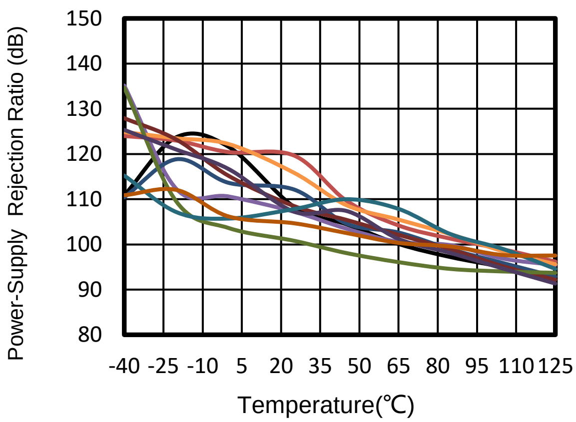


Figure 9. Power-Supply Rejection Ratio vs Temperature

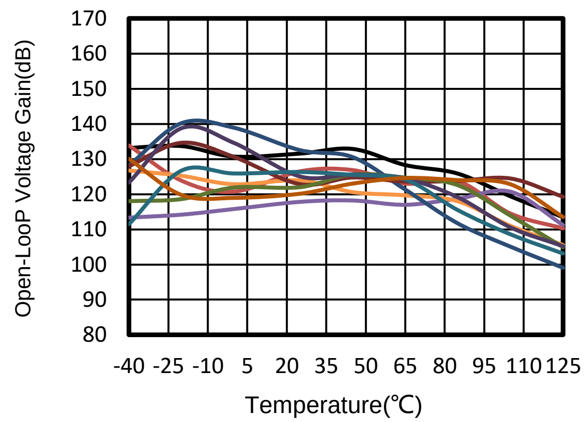


Figure 10. Open-Loop Voltage Gain vs Temperature

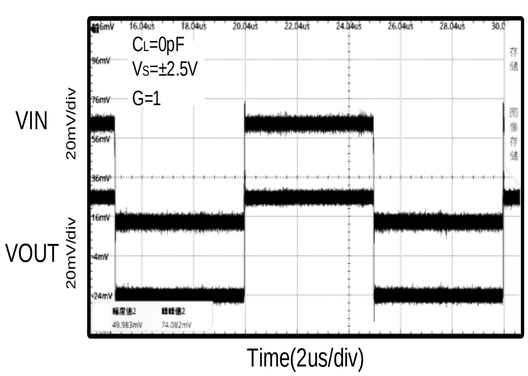


Figure 11. Small-Signal Step Response

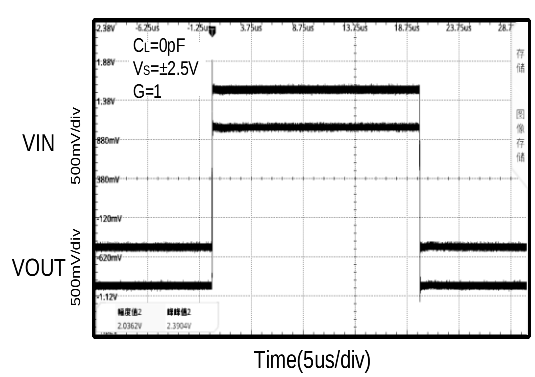


Figure 12. Large-Signal Step Response

TYPICAL CHARACTERISTICS

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At T_A = +25°C, V_S=5V, unless otherwise noted.

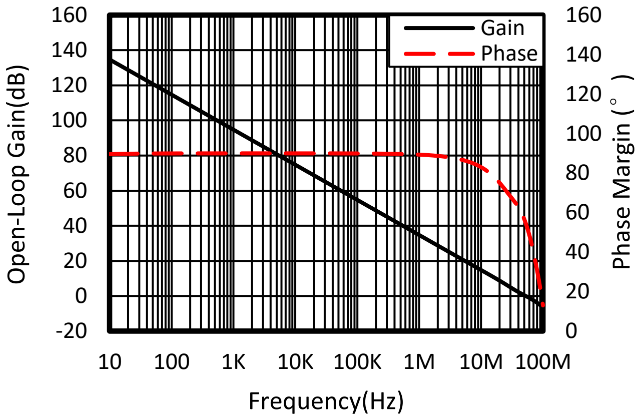


Figure 13. Open-Loop Gain and Phase vs Frequency

8 Application and Implementation

Information in the following applications sections is not part of the RUNIC component specification, and RUNIC does not warrant its accuracy or completeness. RUNIC's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Basic Amplifier Configurations

As with other single-supply op amps, the RS870X may be operated with either a single supply or dual supplies. A typical dual-supply connection is shown in Figure 14, which is accompanied by a single-supply connection. The RS870X is configured as a basic inverting amplifier with a gain of −10 V/V. The dual-supply connection has an output voltage centered on zero, while the single-supply connection has an output centered on the common-mode voltage V_{CM}. For the circuit shown, this voltage is 1.5 V, but may be any value within the common-mode input voltage range.

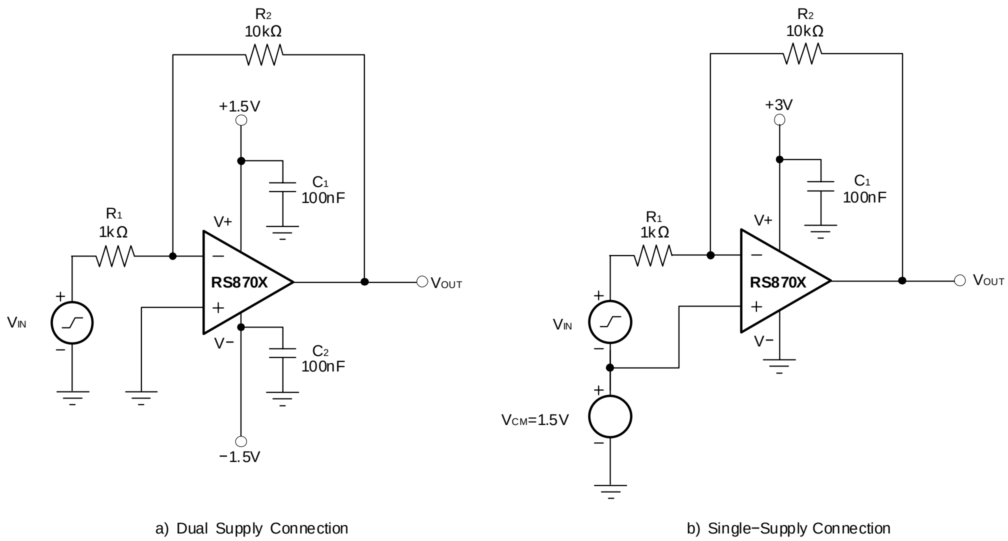


Figure 14. Basic Circuit Connections

Figure 15 shows a single-supply, electret microphone application where V_{CM} is provided by a resistive divider. The divider also provides the bias voltage for the electret element.

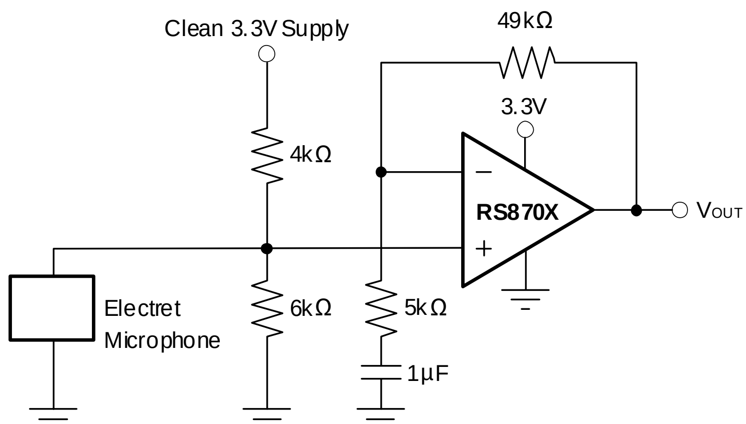


Figure 15. Microphone Preamplifier

8.2 Typical Application

Low-pass filters are commonly employed in signal processing applications to reduce noise and prevent aliasing. The RS870X is ideally suited to construct high-speed, high-precision active filters. Figure 16 illustrates a second-order low-pass filter commonly encountered in signal processing applications.

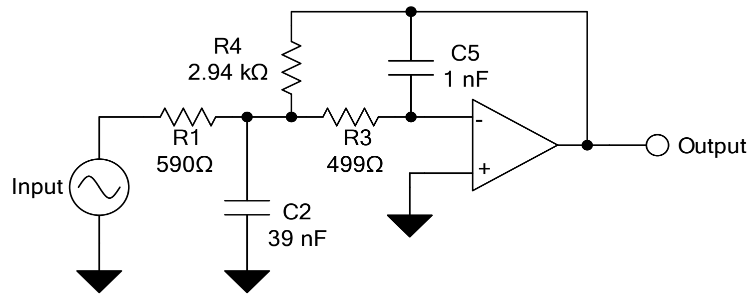


Figure 16. Second-Order Low-Pass Filter

8.2.1 Design Requirements

Use the following parameters for this design example:

• Gain = 5 V/V (inverting gain)
• Low-pass cutoff frequency = 25 kHz
• Second-order Chebyshev filter response with 3-dB gain peaking in the passband

8.2.2 Detailed Design Procedure

The infinite-gain multiple-feedback circuit for a low-pass network function is shown in Figure 16. Use Equation 1 to calculate the voltage transfer function.

$$\frac{\text{Output}}{\text{Input}}(s) = \frac{-1/R_1R_3C_2C_5}{S^2+(S/C_2)(1/R_1+1/R_3+1/R_4)+1/R_3R_4C_2C_5} \quad (1)$$

This circuit produces a signal inversion. For this circuit the gain at DC and the low-pass frequency can be calculated by Equation 2:

$$\text{Gain} = \frac{R_4}{R_1}$$

$$f_C = \frac{1}{2\pi}\sqrt{(1/R_3R_4C_2C_5)} \quad (2)$$

8.2.3 Application Curve

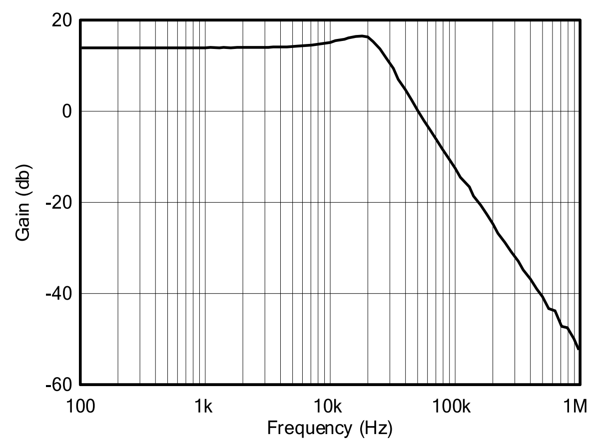


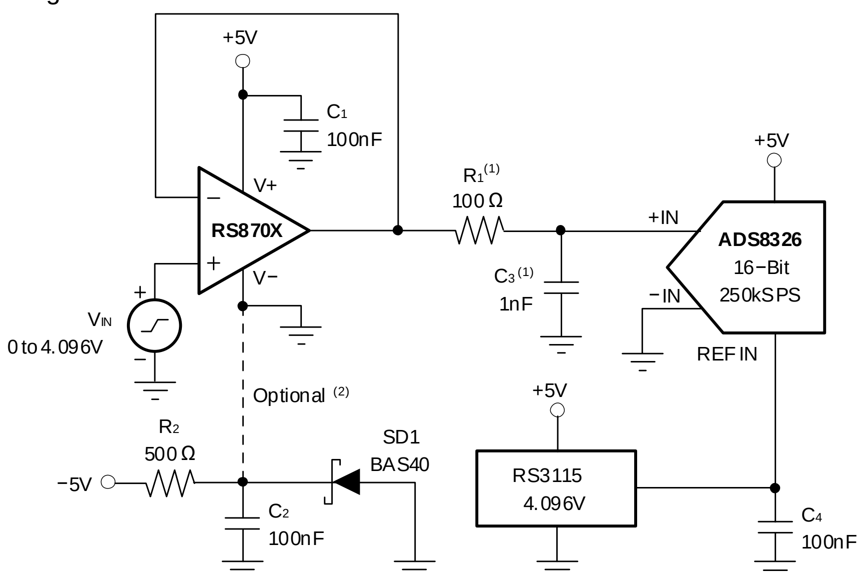
Figure 17. RS870X Second-Order 25 kHz, Chebyshev, Low-Pass Filter

9 System Examples

9.1 Driving an Analog-to-Digital Converter

Very wide common-mode input range, rail-to-rail input and output voltage capability, and high speed make the RS870X an ideal driver for modern ADCs. Also, because it is free of the input offset transition characteristics inherent to some rail-to-rail CMOS op amps, the RS870X provides low THD and excellent linearity throughout the input voltage swing range.

Figure 18 shows the RS870X driving an ADS8326, 16-bit, 250-kSPS converter. The amplifier is connected as a unity-gain, noninverting buffer and has an output swing to 0 V, making it directly compatible with the ADC minus full-scale input level. The 0V level is achieved by powering the RS870X V− pin with a small negative voltage established by the diode forward voltage drop. A small, signal-switching diode or Schottky diode provides a suitable negative supply voltage of −0.3 V to −0.7 V. The supply rail-to-rail is equal to V+, plus the small negative voltage.



(1) Suggested value; may require adjustment based on specific application.

(2) Single-supply applications lose a small number of ADC codes near ground due to op amp output swing limitation. If a negative power supply is available, this simple circuit creates a −0.3-V supply to allow output swing to true ground potential.

Figure 18. Driving the ADS8326

10 LAYOUT

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and operational amplifier itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
  - The RS870X is capable of high-output current (in excess of 150 mA). Applications with low impedance loads or capacitive loads with fast transient signals demand large currents from the power supplies. Larger bypass capacitors such as 1μF solid tantalum capacitors may improve dynamic performance in these applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in Figure 20, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

10.2 Layout Example

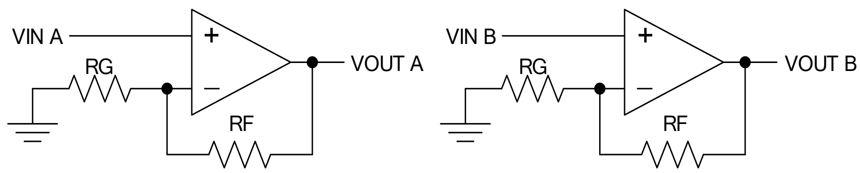


Figure 19. Schematic Representation

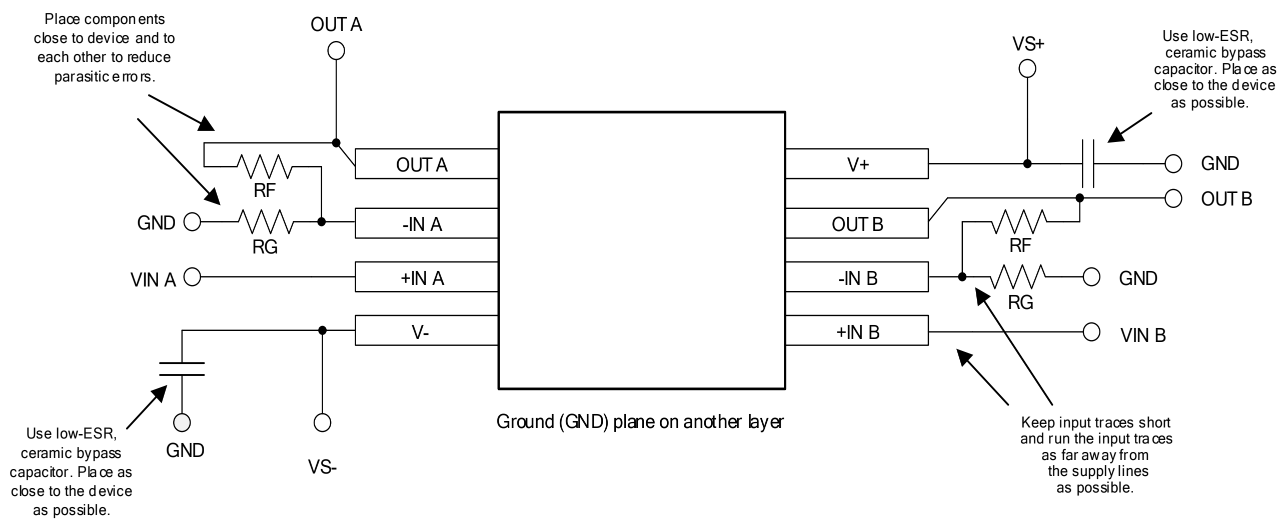
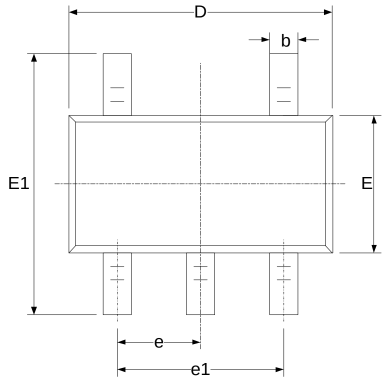


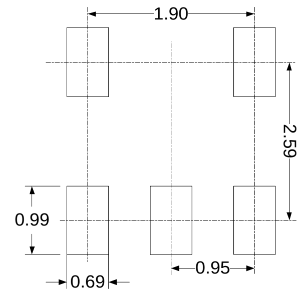
Figure 20. Layout Recommendation

NOTE: Layout Recommendations have been shown for dual op-amp only, follow similar precautions for Single and four.

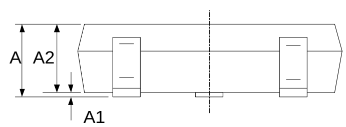
11 PACKAGE OUTLINE DIMENSIONS

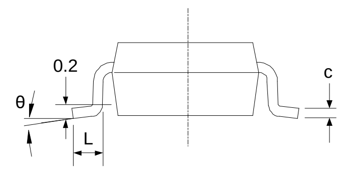
SOT23-5





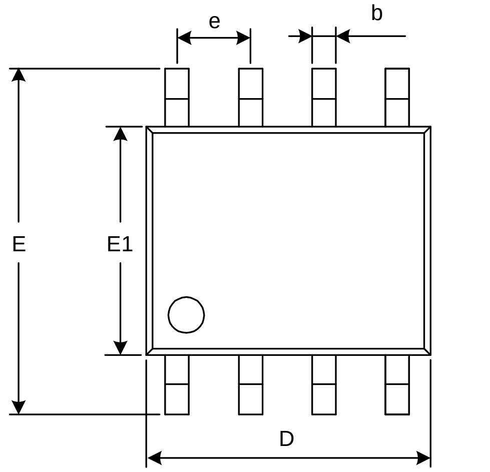
RECOMMENDED LAND PATTERN (Unit: mm)

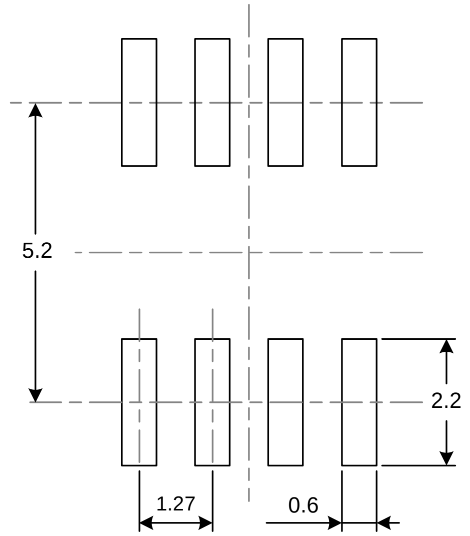




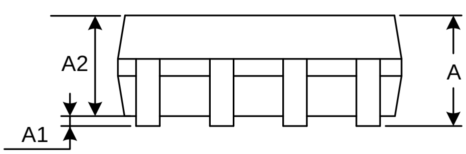
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

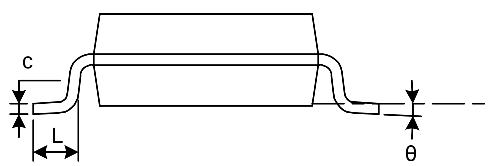
SOIC-8(SOP8)





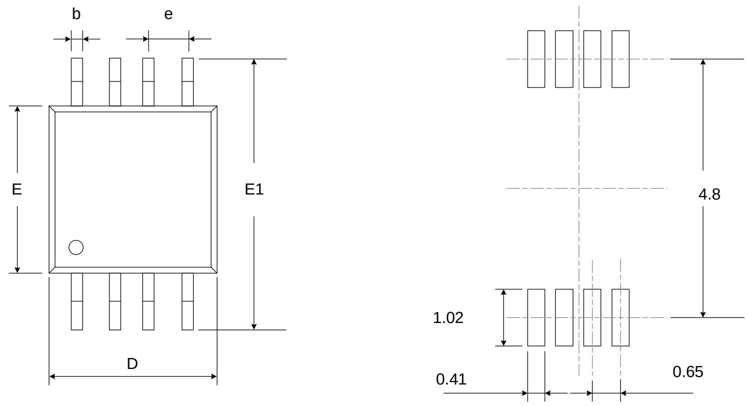
RECOMMENDED LAND PATTERN (Unit: mm)



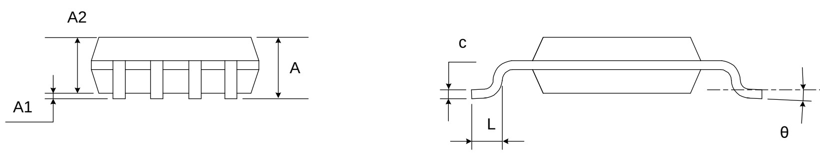


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270(BSC)		0.050(BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

MSOP-8

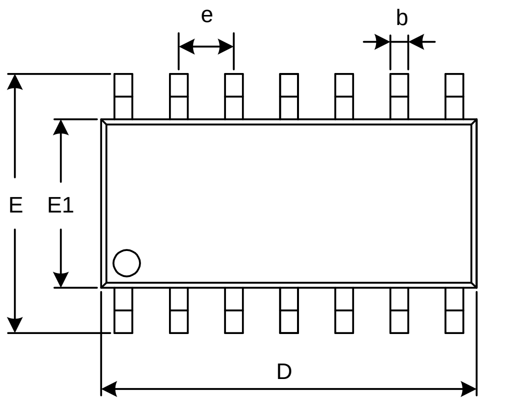


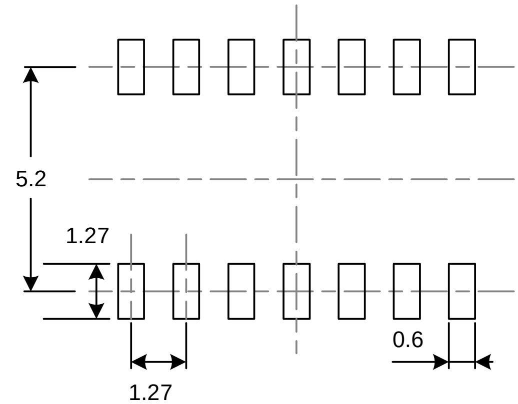
RECOMMENDED LAND PATTERN (Unit: mm)



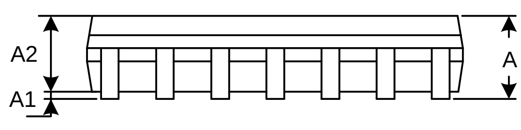
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
e	0.650 (BSC)		0.026 (BSC)	
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

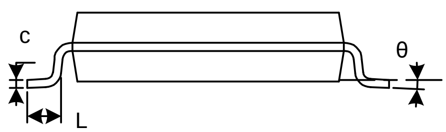
SOIC-14(SOP14)





RECOMMENDED LAND PATTERN (Unit: mm)





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D	8.450	8.850	0.333	0.348
e	1.270(BSC)		0.050(BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

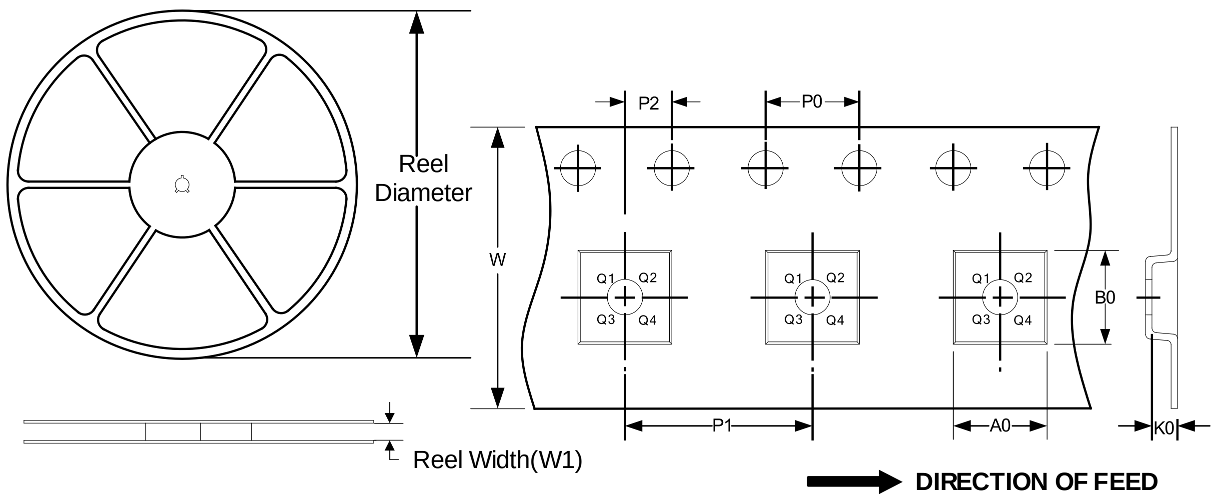
NOTE:

A. All linear dimension is in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. BSC: Basic Dimension. Theoretically exact value shown without tolerances.

12 TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT23-5	7"	9.5	3.20	3.20	1.40	4.0	4.0	2.0	8.0	Q3
SOIC-8(SOP8)	13"	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1
MSOP-8	13"	12.4	5.20	3.30	1.50	4.0	8.0	2.0	12.0	Q1
SOIC-14(SOP14)	13"	16.4	6.60	9.30	2.10	4.0	8.0	2.0	16.0	Q1

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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