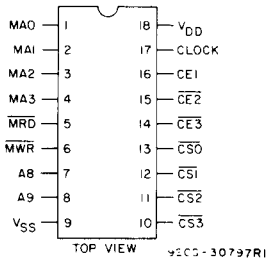


TERMINAL DIAGRAM
CDP1866, CDP1868

CMOS 4-Bit Latch and Decoder Memory Interfaces

Features:

- *Performs memory address latch and decoder functions multiplexed or non-multiplexed*
- *Interfaces directly with all CDP1800 family CPUs*

The RCA-CDP1866, CDP1867, and CDP1868 are CMOS 4-bit memory latch and decoder circuits intended for use in CDP1800 series microprocessor systems. They can interface directly with the multiplexed address bus of this system at maximum clock frequency, and up to eight 4096-bit random-access memories to provide a 4096-byte RAM system. All the necessary chip selects are provided as outputs along with additional enable inputs so that in larger memory systems, the 9-chip 4096-byte blocks can be readily accessed.

These devices are also compatible with non-multiplexed address bus microprocessors.

By connecting the clock input to V_{DD}, the latches are in the data-following mode and the decoded outputs can be used in general-purpose memory-system applications.

The CDP1866 and CDP1868 are intended for use with 1024-word RAMs and are identical except that in the CDP1868, CE1 and $\overline{CE2}$ are latched and $\overline{CS2}$ is valid on $\overline{MWR}$ only. This allows the CDP1868 to be used in a color display system with the CDP1861 and CDP1862 (see Fig. 9). The CDP1867 is intended for use with 4096-word RAMs.

The CDP1866, CDP1867, and CDP1868 are supplied in an 18-lead hermetic dual-in-line ceramic package (D suffix) and an 18-lead plastic package (E suffix). The CDP1866C, CDP1867C, and the CDP1868C are available in chip form (H suffix).

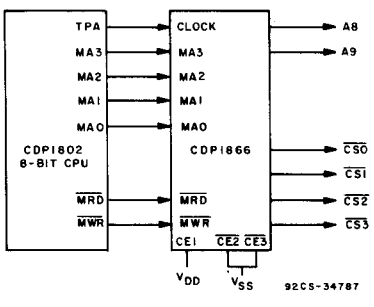
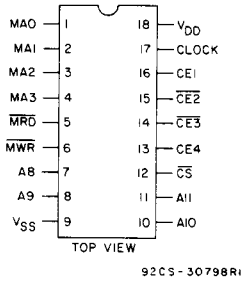


Fig. 1 - CDP1866 used as a high-order address latch decoder.



TERMINAL DIAGRAM
CDP1867

CDP1866, CDP1867, CDP1868

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltage referenced to V_{SS} Terminal)
CDP1866, CDP1867, CDP1868 ..... -0.5 to 11 V
CDP1866C, CDP1867C, CDP1868C ..... -0.5 to 7 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} + 0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/°C to 200 mW
For T_A = -55 to +100°C (PACKAGE TYPE D) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE D) ..... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 40 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE D ..... -55 to +125°C
PACKAGE TYPE E ..... -40 to + 85°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

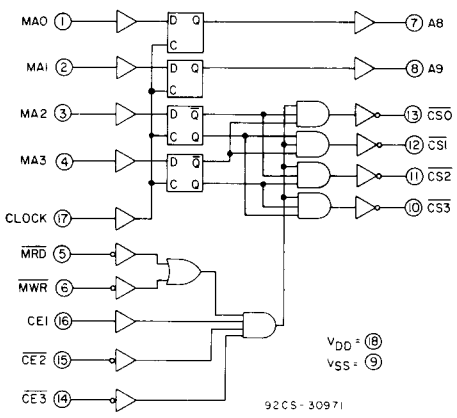


Fig. 2 - Functional diagram for the CDP1866.

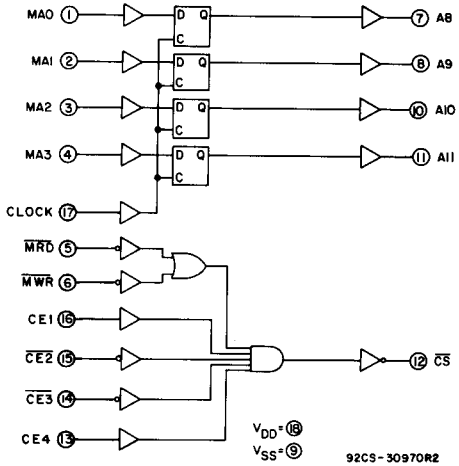


Fig. 3 - Functional diagram for the CDP1867.

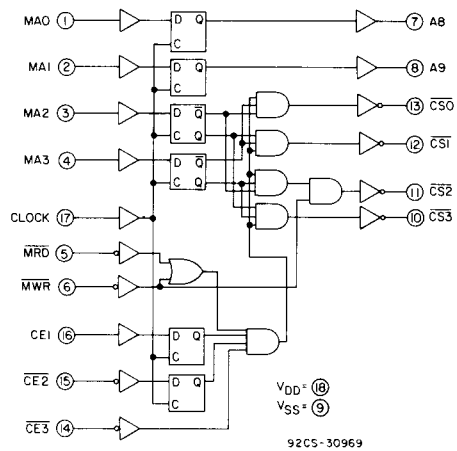


Fig. 4 - Functional diagram for the CDP1868.

CDP1866, CDP1867, CDP1868

OPERATING CONDITIONS at T_A = Full Package-Temperature Range.
For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1866, CDP1867, CDP1868		CDP1866C, CDP1867C, CDP1868C		
	Min.	Max.	Min.	Max.	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	

STATIC ELECTRICAL CHARACTERISTICS at T_A = −40 to +85°C, V_{DD} ± 5%, Except as noted

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
				CDP1866, CDP1867, CDP1868			CDP1866C, CDP1867C, CDP1868C			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current I_{DD}	— —	0,5 0,10	5 10	— —	1 10	10 100	— —	5 —	50 —	μA
Output Low Drive (Sink) Current I_{OL}	0.4 0.5	0,5 0,10	5 10	1.6 2.6	3.2 5.2	— —	1.6 —	3.2 —	— —	mA
Output High Drive (Source) Current I_{OH}	4.6 9.5	0,5 0,10	5 10	−1.15 −2.6	−2.3 −5.2	— —	−1.15 —	−2.3 —	— —	
Output Voltage Low-Level V_{OL}‡	— —	0,5 0,10	5 10	— —	0 0	0.1 0.1	— —	0 —	0.1 —	V
Output Voltage High-Level V_{OH}‡	— —	0,5 0,10	5 10	4.9 9.9	5 10	— —	4.9 —	5 —	— —	
Input Low Voltage V_{IL}	0.5,4.5 0.5,9.5	— —	5 10	— —	— —	1.5 3	— —	— —	1.5 —	
Input High Voltage V_{IH}	0.5,4.5 0.5,9.5	— —	5 10	3.5 7	— —	— —	3.5 —	— —	— —	
Input Leakage Current I_{IN}	Any Input	0,5 0,10	5 10	— —	— —	±1 ±2	— —	— —	±1 —	μA
Input Capacitance C_{IN}	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance C_{OUT}	—	—	—	—	10	15	—	10	15	
Operating Device Current I_{DD1}△	0,5 0,10	0,5 0,10	5 10	— —	50 150	100 300	— —	50 —	100 —	μA
Minimum Data Retention Voltage V_{DR}	$V_{DD} = V_{DR}$			—	2	2.4	—	2	2.4	V
Data Retention Current I_{DR}	V_{DD} = 2.4 V			—	0.01	1	—	0.5	5	μA

*Typical values are for T_A = 25°C. ‡$I_{OL} = I_{OH}$ = 1 μA.
△Operating current is measured at 200 kHz for V_{DD} = 5 V and 400 kHz for V_{DD} = 10 V, with open outputs (worst-case frequencies for CDP1802A system operating at maximum speed of 3.2 MHz).

CDP1866, CDP1867, CDP1868

TRUTH TABLES FOR THE CDP1866 AND CDP1868

INPUTS							OUTPUTS			
$\overline{MRD}$ or $\overline{MWR}$	CE1	$\overline{CE2}$	$\overline{CE3}$	CLK	MA2	MA3	$\overline{CS0}$	$\overline{CS1}$	$\overline{CS2}$	$\overline{CS3}$
0	1	0	0	1	0	0	0	1	1	1
0	1	0	0	1	1	0	1	0	1	1
0*	1	0	0	1	0	1	1	1	0*	1
0	1	0	0	1	1	1	1	1	1	0
0	1	0	0	0	X	X	PREVIOUS STATE			
X	X	X	1	X	X	X	1	1	1	1
X	X	1	X	X	X	X	1	1	1	1
X	0	X	X	X	X	X	1	1	1	1
1	X	X	X	X	X	X	1	1	1	1

*In the CDP1868, $\overline{CS2}$ will be valid ($\overline{CS2}$=0) only if $\overline{MRW}$ is low, regardless of the polarity of $\overline{MRD}$.

INPUTS			OUTPUTS	
CLK	MA0	MA1	A8	A9
1	0	0	0	0
1	0	1	0	1
1	1	0	1	0
1	1	1	1	1
0	X	X	PREVIOUS STATE	

$\overline{MRD}$	$\overline{MWR}$	$\overline{MRD}$ or $\overline{MWR}$
0	0	1
0	1	1
1	0	1
1	1	0

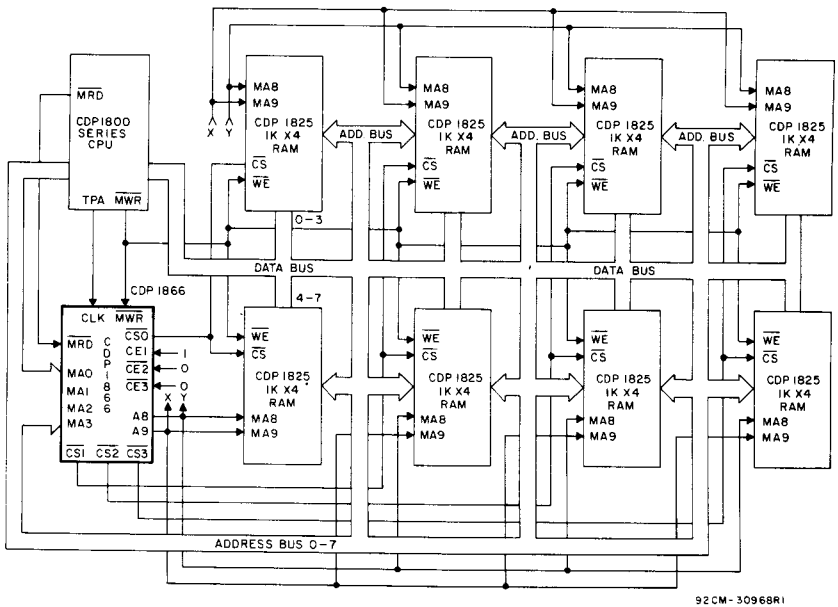
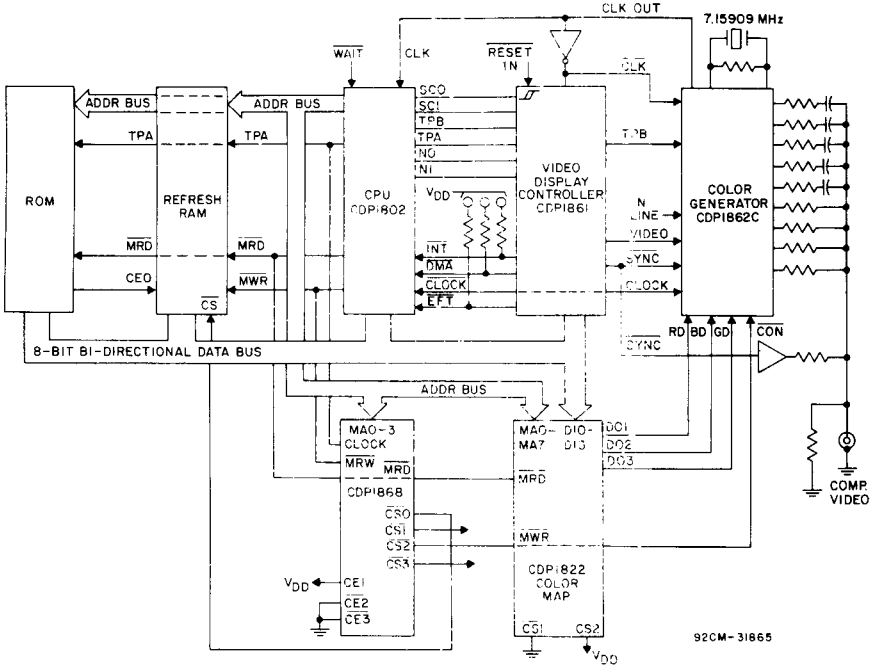


Fig. 5 - 4096-word by 8-bit random-access memory system using the CDP1866.



CHIP SELECT	ADDRESS
CS0	0000 - 03FF
CS1	0400 - 07FF
CS2	0800 - 0BFF
CS3	0C00 - 0FFF

Fig. 6 - Typical color display system using the CDP1868.

The CDP1868 can be used in a color display system to write to the refresh RAM and the color map RAM at different address locations, as shown in Fig. 9. Both the refresh RAM and the color map RAM are read from the same address. The purpose of reading from the same address is that when a byte of data from the refresh RAM is sent to the video display controller (CDP1861), an additional 3 bits of color information are needed from the color map RAM for the color generator (CDP1862). In Fig. 9, the bit display data are written into the refresh RAM at 0000-00FF. The color display data are written into the color map RAM at locations 0800-08FF. Both are read at locations 0000-00FF.

CDP1866, CDP1867, CDP1868

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85°C$, $V_{DD} \pm 5\%$, t_r, $t_f = 20$ ns, $V_{IH} = 0.7\ V_{DD}$, $V_{IL} = 0.3\ V_{DD}$, $C_L = 100$ pF. See Fig. 8

CHARACTERISTIC		V_{DD} (V)	LIMITS						UNITS
			CDP1866			CDP1866C			
			Min.	Typ.•	Max.Δ	Min.	Typ.•	Max.Δ	
Minimum Setup Time, Memory Address to CLOCK,	t_{MACL}	5	—	50	75	—	50	75	ns
		10	—	25	40	—	—	—	
Minimum Hold Time, Memory Address After CLOCK,	t_{CLMA}	5	—	50	75	—	50	75	
		10	—	25	40	—	—	—	
Minimum CLOCK Pulse Width	t_{CLCL}	5	—	50	75	—	50	75	
		10	—	25	40	—	—	—	
Propagation Delay Times:									
Chip Enable to Chip Select,	t_{CECS}	5	—	150	225	—	150	225	
		10	—	75	125	—	—	—	
MRD or MRW to Chip Select,	t_{MCS}	5	—	125	200	—	125	200	
		10	—	65	125	—	—	—	
CLOCK to Chip Select,	t_{CLCS}	5	—	175	275	—	175	275	
		10	—	90	150	—	—	—	
CLOCK to Address,	t_{CLA}	5	—	125	200	—	125	200	
		10	—	65	125	—	—	—	
Memory Address to Chip Select,	t_{MACS}	5	—	150	225	—	150	225	
		10	—	75	125	—	—	—	
Memory Address to Address,	t_{MAA}	5	—	80	125	—	80	125	
		10	—	40	60	—	—	—	

•Typical values are for $T_A = 25°C$.
ΔMaximum limits of minimum characteristics are the values above which all devices function.

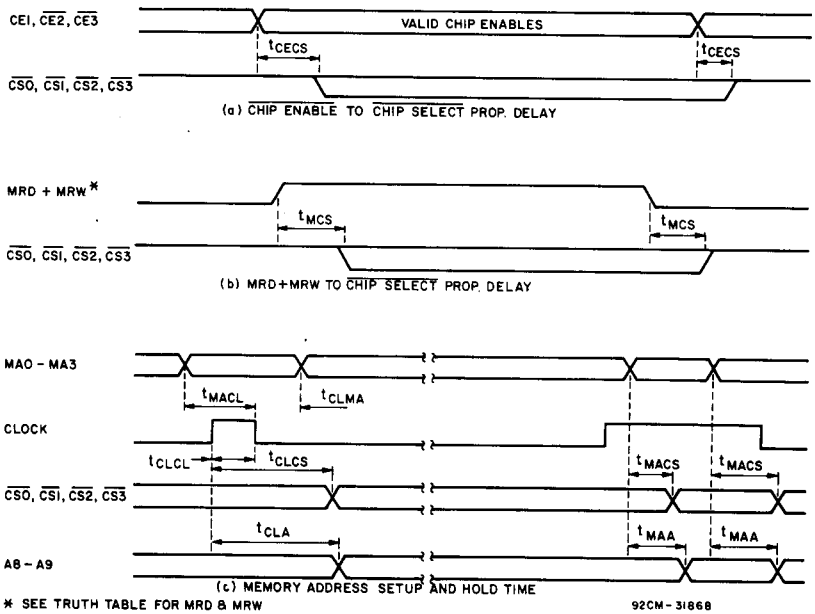


Fig. 8 - CDP1866 timing waveforms.

CDP1866, CDP1867, CDP1868

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85°C$, $V_{DD} \pm 5\%$, t_r, $t_f = 20$ ns, $V_{IH} = 0.7\ V_{DD}$, $V_{IL} = 0.3\ V_{DD}$, $C_L = 100$ pF. See Fig. 9

CHARACTERISTIC		V_{DD} (V)	LIMITS						UNITS
			CDP1867			CDP1867C			
			Min.	Typ.•	Max.Δ	Min.	Typ.•	Max.Δ	
Minimum Setup Time, Memory Address to CLOCK,	t_{MACL}	5	—	50	75	—	50	75	ns
		10	—	25	40	—	—	—	
Minimum Hold Time, Memory Address After CLOCK,	t_{CLMA}	5	—	50	75	—	50	75	
		10	—	25	40	—	—	—	
Minimum CLOCK Pulse Width	t_{CLCL}	5	—	50	75	—	50	75	
		10	—	25	40	—	—	—	
Propagation Delay Times:									
$\overline{\text{Chip Enable}}$ to $\overline{\text{Chip Select}}$,	t_{CECS}	5	—	100	150	—	100	150	
		10	—	50	75	—	—	—	
$\overline{\text{MRD}}$ or MRW to $\overline{\text{Chip Select}}$,	t_{MCS}	5	—	80	125	—	80	125	
		10	—	40	60	—	—	—	
$\overline{\text{CLOCK}}$ to Address,	t_{CLA}	5	—	125	200	—	125	200	
		10	—	65	100	—	—	—	
Memory Address to Address,	t_{MAA}	5	—	75	125	—	75	125	
		10	—	40	60	—	—	—	

•Typical values are for $T_A = 25°C$ and nominal V_{DD}.
ΔMaximum limits of minimum characteristics are the values above which all devices function.

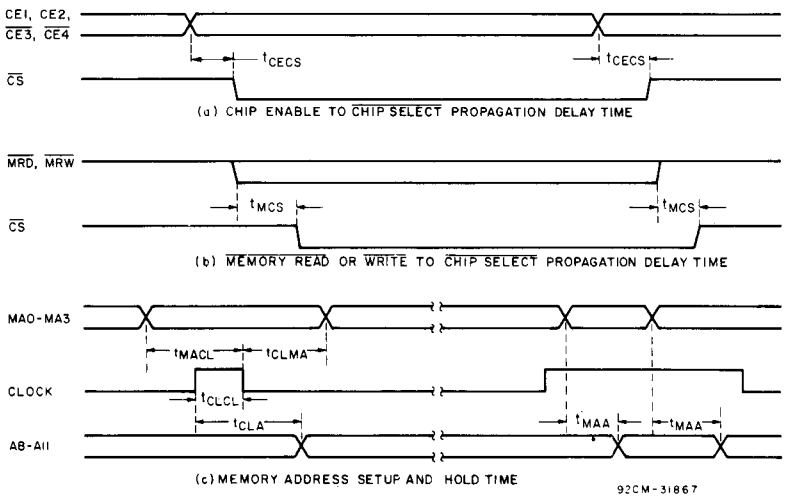


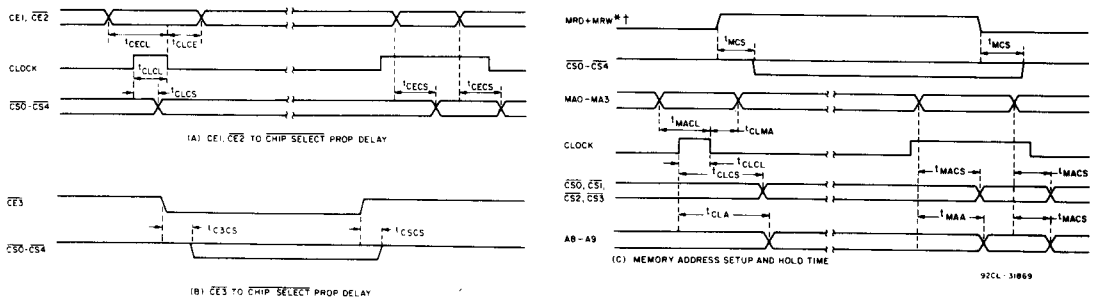
Fig. 9 - CDP1867 timing waveforms.

CDP1866, CDP1867, CDP1868

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = −40 to +85°C, V_{DD} ± 5%, t_r, t_f = 20 ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100 pF. See Fig. 10

CHARACTERISTIC		V_{DD} (V)	LIMITS						UNITS
			CDP1868			CDP1868C			
			Min.	Typ.•	Max.Δ	Min.	Typ.•	Max.Δ	
Minimum Setup Times:									
Chip Enable to CLOCK,	t_{CECL}	5	—	50	75	—	50	75	ns
		10	—	25	40	—	—	—	
Memory Address to CLOCK,	t_{MACL}	5	—	50	75	—	50	75	
		10	—	25	40	—	—	—	
Minimum Hold Times:									
Chip Enable After CLOCK,	t_{CLCE}	5	—	50	75	—	50	75	
		10	—	25	40	—	—	—	
Memory Address After CLOCK,	t_{CLMA}	5	—	50	75	—	50	75	
		10	—	25	40	—	—	—	
Minimum CLOCK Pulse Width,	t_{CLCL}	5	—	50	75	—	50	75	
		10	—	25	40	—	—	—	
Propagation Delay Times:									
CLOCK to Chip Select,	t_{CLCS}	5	—	175	275	—	175	275	
		10	—	90	150	—	—	—	
Chip Enable to Chip Select,	t_{CECS}	5	—	150	225	—	150	225	
		10	—	75	125	—	—	—	
Chip Enable 3 to Chip Select,	t_{C3CS}	5	—	150	225	—	150	225	
		10	—	75	125	—	—	—	
MRD or MRW to Chip Select,	t_{MCS}	5	—	125	200	—	125	200	
		10	—	65	100	—	—	—	
CLOCK to Address,	t_{CLA}	5	—	125	200	—	125	200	
		10	—	65	100	—	—	—	
Memory Address to Chip Select,	t_{MACS}	5	—	125	200	—	125	200	
		10	—	65	100	—	—	—	
Memory Address to Address,	t_{MAA}	5	—	80	120	—	80	120	
		10	—	40	60	—	—	—	

•Typical values are for T_A = 25°C and nominal.
ΔMaximum limits of minimum characteristics are the values above which all devices function.



*SEE TRUTH TABLE FOR MRD+MWR
† CS2 WILL BE VALID (CS2+0) ONLY IF MRW IS LOW REGARDLESS OF MRD SIGNAL POLARITY

Fig. 10 - CDP1868 timing waveforms.