19-1365; Rev 1; 6/99

EVALUATION KIT AVAILABLE

MAXIM

Low-Cost, 1%-Accurate Signal Conditioner for Piezoresistive Sensors

MAX1450

General Description

The MAX1450 sensor signal conditioner is optimized for piezoresistive sensor calibration and temperature compensation. It includes an adjustable current source for sensor excitation and a 3-bit programmable-gain amplifier (PGA). Achieving a total typical error factor within 1% of the sensor's inherent repeatability errors, the MAX1450 compensates offset, full-span output (FSO), offset tempco, FSO tempco, and FSO nonlinearity of silicon piezoresistive sensors via external trimmable resistors, potentiometers, or digital-to-analog converters (DACs).

The MAX1450 is capable of compensating sensors that display close error distributions with a single temperature point, making it ideal for low-cost, medium-accuracy applications. Although optimized for use with popular piezoresistive sensors, it may also be used with other resistive sensor types such as strain gauges.

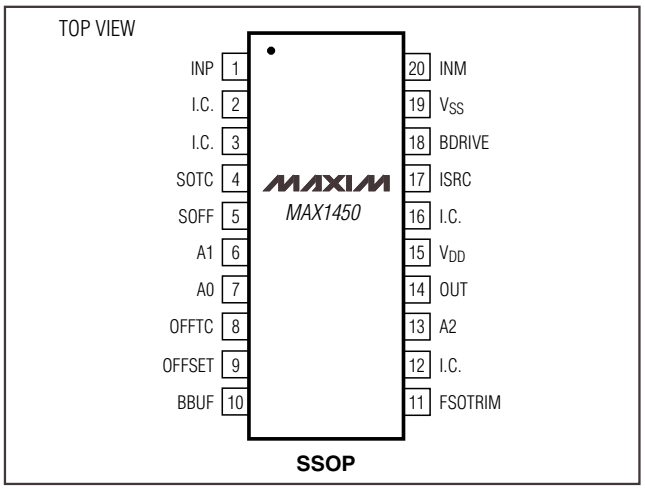
Customization

Maxim can customize the MAX1450 for unique requirements including improved power specifications. With a dedicated cell library consisting of more than 90 sensor-specific functional blocks, Maxim can quickly provide customized MAX1450 solutions. Contact the factory for additional information.

Applications

Piezoresistive Pressure and Acceleration Transducers and Transmitters
Manifold Absolute Pressure (MAP) Sensors
Automotive Systems
Hydraulic Systems
Industrial Pressure Sensors

Pin Configuration



Features

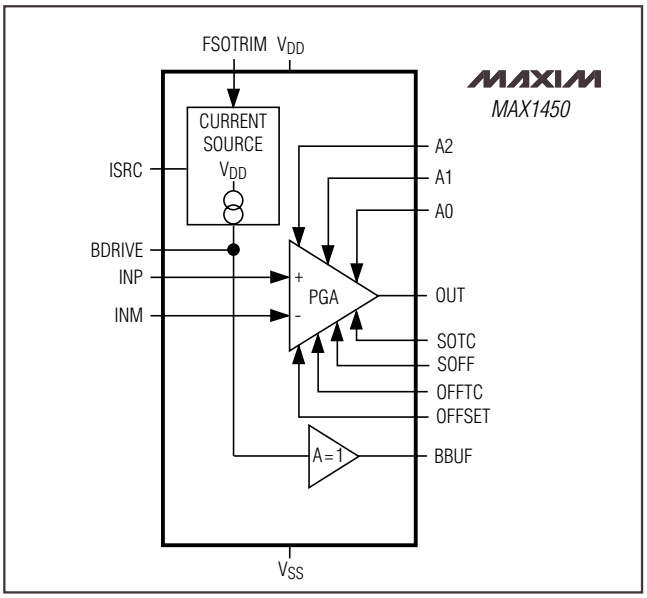
- ♦ **1% Sensor Signal Conditioning**
- ♦ **Corrects Sensor Errors Using Coefficients Stored in External Trimmable Resistors, Potentiometers, or DACs**
- ♦ **Compensates Offset, Offset TC, FSO, FSO TC, and FSO Linearity**
- ♦ **Rail-to-Rail Analog Output**
- ♦ **Programmable Current Source for Sensor Excitation**
- ♦ **Fast Signal-Path Settling Time (< 1ms)**
- ♦ **Accepts Sensor Outputs from 10mV/V to 30mV/V**
- ♦ **Fully Analog Signal Path**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1450CAP	0°C to +70°C	20 SSOP
MAX1450C/D	0°C to +70°C	Dice*
MAX1450AAP	-40°C to +125°C	20 SSOP

**Dice are tested at T_A = +25°C, DC parameters only.*

Functional Diagram



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ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD} to V_{SS}.....-0.3V to +6V
All Other Pins .....(V_{SS} - 0.3V) to (V_{DD} + 0.3V)
Short-Circuit Duration, OUT, BBUF, BDRIVE .....Continuous
Continuous Power Dissipation (T_A = +70°C)
SSOP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Range
MAX1450CAP .....0°C to +70°C
MAX1450AAP .....-40°C to +125°C
Storage Temperature Range .....-65°C to +165°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V, V_{SS} = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL CHARACTERISTICS						
Supply Voltage	V_{DD}		4.5	5.0	5.5	V
Supply Current	I_{DD}	T_A = +25°C (Note 1)		2.8	3.5	mA
ANALOG INPUT (PGA)						
Input Impedance	R_{IN}			1.0		MΩ
Input-Referred Offset Temperature Coefficient		(Notes 2, 3)		±0.5		µV/°C
Amplifier Gain Nonlinearity				0.01		%V_{DD}
Output Step-Response Time		63% of final value		1		ms
Common-Mode Rejection Ratio	CMRR	From V_{SS} to V_{DD}		90		dB
Input-Referred Adjustable Offset Range		(Note 4)		±100		mV
Input-Referred Adjustable Full-Span Output Range		(Note 5)		10 to 30		mV/V
SUMMING JUNCTION (Figure 1)						
Offset Gain	$\left\lvert\frac{\Delta V_{OUT}}{\Delta V_{OFFSET}}\right\rvert$			1.15		V/V
Offset TC Gain	$\left\lvert\frac{\Delta V_{OUT}}{\Delta V_{OFFTC}}\right\rvert$			1.15		V/V
ANALOG OUTPUT (PGA)						
Differential Signal Range Gain		Eight selectable gains (Table 3)		39 to 221		V/V
Minimum Differential Signal Gain			36	39	44	V/V
Differential Signal Path Temperature Coefficient		At any gain		±50		ppm/°C
Output Voltage Swing		5kΩ load to V_{SS} or V_{DD}, T_A = +25°C	V_{SS} + 0.25		V_{DD} - 0.25	V
		No load, T_A = T_{MIN} to T_{MAX}	V_{SS} + 0.05		V_{DD} - 0.05	
Output Current Range		V_{OUT} = (V_{SS} + 0.25V) to (V_{DD} - 0.25V), T_A = +25°C	-1.0 (sink)		1.0 (source)	mA
Output Noise		DC to 10Hz, gain = 39, sensor impedance = 5kΩ		500		$µV_{RMS}$

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V, V_{SS} = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT SOURCE						
Bridge Current Range	I_{BDRIVE}		0.1	0.5	2.0	mA
Bridge Voltage Swing	V_{BDRIVE}		V_{SS} + 1.3		V_{DD} - 1.3	V
Current-Source Gain	AA	$\Delta I_{BDRIVE}/\Delta I_{ISRC}$ (Figure 2)		13		µA/µA
Current-Source Input Voltage Range	V_{ISRC}		V_{SS} + 1.3		V_{DD}- 1.3	V
BUFFER (BBUF)						
Voltage Swing		No load	V_{SS} + 1.3		V_{DD} - 1.3	V
Current Drive		V_{BDRIVE} = 2.5V	-100		100	µA
Offset Voltage	V_{OFS}	(V_{BDRIVE} - V_{BBUF}) at V_{BDRIVE} = 2.5V, no load	-20		20	mV

Note 1: Contact factory for high-volume applications requiring less than 1.5mA.
Note 2: All electronics temperature errors are compensated together with the sensor errors.
Note 3: The sensor and the MAX1450 must always be at the same temperature during calibration and use.
Note 4: This is the maximum allowable sensor offset at minimum gain (39V/V).
Note 5: This is the sensor's sensitivity normalized to its drive voltage, assuming a desired full-span output (FSO) of 4V and a bridge voltage of 2.5V. Operating at lower bridge excitation voltages can accommodate higher sensitivities.

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Pin Description

PIN	NAME	FUNCTION
1	INP	Positive Sensor Input. Input impedance is typically 1MΩ. Rail-to-rail input range.
2, 3, 12, 16	I.C.	Internally connected. Leave unconnected.
4	SOTC	Offset TC Sign Bit Input. A logic low inverts V_{OFFTC} with respect to V_{SS}. This pin is internally pulled to V_{SS} via a 1MΩ (typical) resistor. Connect to V_{DD} to add V_{OFFTC} to the PGA output, or leave unconnected (or connect to V_{SS}) to subtract V_{OFFTC} from the PGA output.
5	SOFF	Offset Sign Bit Input. A logic low inverts V_{OFFSET} with respect to V_{SS}. This pin is internally pulled to V_{SS} via a 1MΩ (typical) resistor. Connect to V_{DD} to add V_{OFFSET} to the PGA output, or leave unconnected (or connect to V_{SS}) to subtract V_{OFFSET} from the PGA output.
6	A1	PGA Gain-Set Input. Internally pulled to V_{SS} via a 1MΩ (typical) resistor. Connect to V_{DD} for a logic high or V_{SS} for a logic low.
7	A0	PGA Gain-Set LSB Input. Internally pulled to V_{SS} via a 1MΩ (typical) resistor. Connect to V_{DD} for a logic high or V_{SS} for a logic low.
8	OFFTC	Offset TC Adjust. Analog input summed with PGA output and V_{OFFSET}. Input impedance is typically 1MΩ. Rail-to-rail input range.
9	OFFSET	Offset Adjust Input. Analog input summed with PGA output and V_{OFFTC}. Input impedance is typically 1MΩ. Rail-to-rail input range.
10	BBUF	Buffered Bridge-Voltage Output (the voltage at BDRIVE). Use with correction resistor R_{STC} to correct for FSO tempco.
11	FSOTRIM	Bridge Drive Current-Set Input. The voltage on this pin sets the nominal I_{ISRC}. See the *Bridge Drive* section.
13	A2	PGA Gain-Set MSB Input. Internally pulled to V_{SS} via a 11kΩ (typical) resistor. Connect to V_{DD} for a logic high or V_{SS} for a logic low.
14	OUT	PGA Output Voltage. Connect a 0.1µF capacitor from OUT to V_{SS}.
15	V_{DD}	Positive Supply Voltage Input. Connect a 0.1µF capacitor from V_{DD} to V_{SS}.
17	ISRC	Current-Source Reference. Connect a 50kΩ (typical) resistor from ISRC to V_{SS}.
18	BDRIVE	Sensor Excitation Current Output. This pin drives a nominal 0.5mA through the bridge.
19	V_{SS}	Negative Power-Supply Input.
20	INM	Negative Sensor Input. Input impedance is typically 1MΩ. Rail-to-rail input range.

Detailed Description

Analog Signal Path

The MAX1450's signal path is fully differential and combines the following three stages: a 3-bit PGA with selectable gains of 39, 65, 91, 117, 143, 169, 195, and 221; a summing junction; and a differential to single-ended output buffer (Figure 1).

Programmable-Gain Amplifier

The analog signal is first fed into a programmable-gain instrumentation amplifier with a CMRR of 90dB and a common-mode input range from V_{SS} to V_{DD}. Pins A0, A1, and A2 set the PGA gain anywhere from 39V/V to 221V/V (in steps of 26).

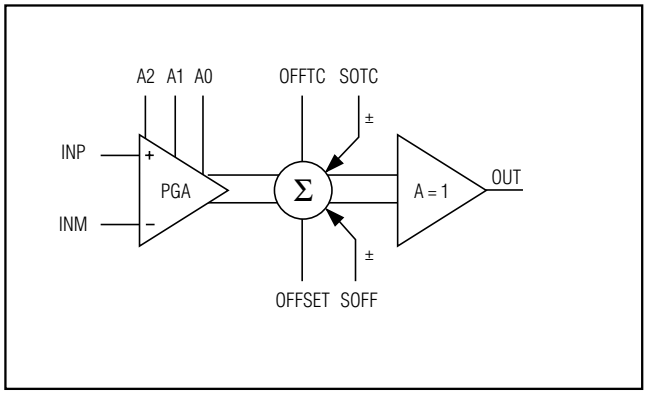

Figure 1. Signal-Path Functional Diagram

Summing Junction

The second stage in the analog signal path consists of a summing junction for offset, offset temperature compensation, and the PGA output. The offset voltage (V_{OFFSET}) and offset temperature-compensation voltage (V_{OFFTC}) add or subtract from the PGA output depending on their respective sign bits, offset sign (SOFF), and offset TC sign (SOTC). V_{OFFSET} and V_{OFFTC} can range in magnitude from V_{SS} to V_{DD}.

Output Buffer

The final stage in the analog signal path consists of a unity-gain buffer. This buffer is capable of swinging to within 250mV of V_{SS} and V_{DD} while sourcing/sinking up to 1.0mA, or within 50mV of the power supplies with no load.

Bridge Drive

Figure 2 shows the functional diagram of the on-chip current source. The voltage at FSOTRIM, in conjunction with R_{ISRC}, sets the nominal current, I_{ISRC} which sets the FSO (refer to Figure 3 for sensor terminology.) I_{ISRC} is additionally modulated by components from the external resistor R_{STC} and the optional resistor R_{LIN}. R_{STC} is used to feed back a portion of the buffered bridge-excitation voltage (V_{BBUF}), which compensates FSO TC errors by modulating the bridge-excitation current over temperature. To correct FSO linearity errors, feed back a portion of the output voltage to the current-source reference node via the optional R_{LIN} resistor.

Applications Information

Compensation Procedure

The following compensation procedure assumes a pressure transducer with a +5V supply and an output voltage that is ratiometric to the supply voltage (see *Ratiometric Output Configuration* section). The desired offset voltage (V_{OUT} at P_{MIN}) is 0.5V, and the desired FSO voltage ($V_{OUT}(P_{MAX})$ - $V_{OUT}(P_{MIN})$) is 4V; thus the FS output voltage (V_{OUT} at P_{MAX}) will be 4.5V. The procedure requires a minimum of two test pressures (e.g., zero and full scale) and two temperatures. A typical compensation procedure is as follows:

1) Perform Coefficient Initialization

2) Perform FSO Calibration

3) Perform FSO TC Compensation

4) Perform OFFSET TC Compensation

5) Perform OFFSET Calibration

6) Perform Linearity Calibration (Optional)

Coefficient Initialization

Select the resistor values and the PGA gain to prevent gross overload of the PGA and bridge current source. These values depend on sensor behavior and require some sensor characterization data. This data may be available from the sensor manufacturer. If not, it can be generated by performing a two-temperature, two-pres-

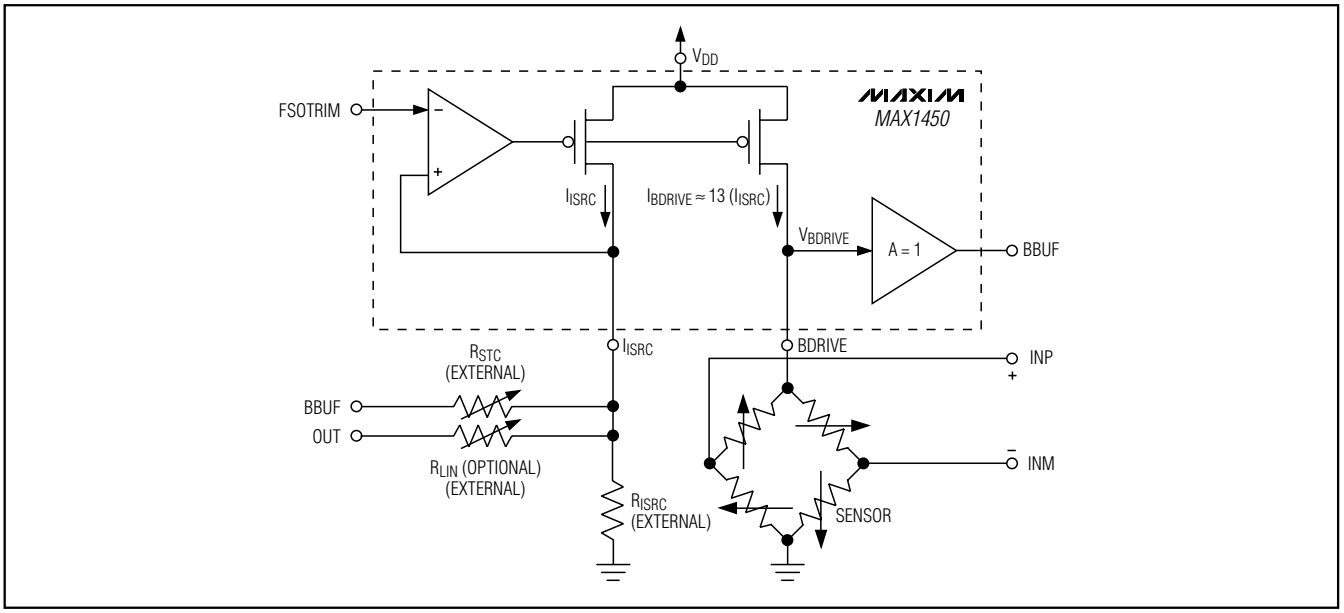

Figure 2. Bridge Drive Circuit

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sure sensor evaluation. Note that the resistor values and PGA gain obtained from this evaluation will represent a starting point. The final compensated transducer will likely use slightly different values. The required sensor information is shown in Table 1, and can be used to obtain the values for the parameters shown in Table 2.

Selecting R_{ISRC}

R_{ISRC} programs the nominal sensor excitation current and is placed between ISRC and V_{SS}. Use a variable resistor with a nominal starting value of:

$$R_{ISRC} \approx 13 \times Rb(T1)$$
$$\approx 13(5k\Omega) = 65k\Omega$$

where Rb(T1) is the sensor input impedance at temperature T1 (usually +25°C).

Selecting R_{STC}

R_{STC} compensates the FSO TC errors and is placed between BBUF and ISRC. Use a variable resistor with a nominal starting value of the following:

$$R_{STC} \approx \frac{R_{ISRC} \times 500ppm/°C}{TCR - |TCS|}$$
$$\approx \frac{65k\Omega \times 500ppm/°C}{2600ppm/°C - |-2100ppm/°C|} = 65k\Omega$$

This approximation works best for bulk, micromachined, silicon piezoresistive sensors (PRTs). Negative values for R_{STC} indicate unexpected sensor behavior that cannot be compensated by the MAX1450 without additional external circuitry.

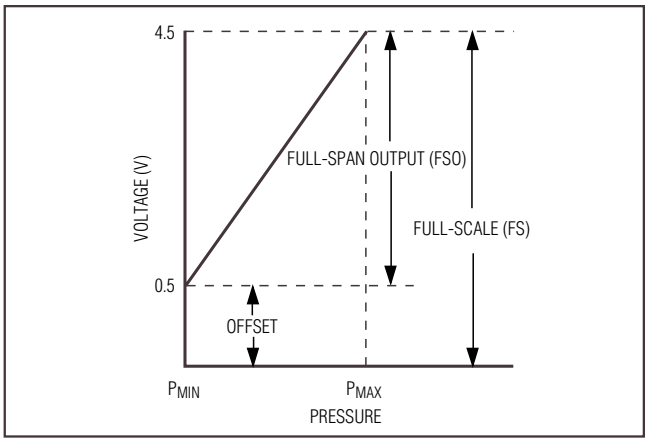

Figure 3. Typical Pressure-Sensor Output

Selecting PGA Gain Setting

Calculate the ideal gain using the following formula, and select the nearest gain setting from Table 3.

SensorFSO can be derived as follows:

$$SensorFSO = S \times V_{BDRIVE} \times \Delta P$$
$$= 1.5mV/V\ psi \times 2.5V \times 10\ psi$$
$$= 0.0375V$$

where S is the sensor sensitivity at T1, V_{BDRIVE} is the sensor excitation voltage (initially 2.5V), and ΔP is the maximum pressure differential.

Table 1. Sensor Information

PARAMETER	SENSOR DESCRIPTION	TYPICAL VALUE
Rb(T)	Input/Output Impedance	5kΩ at +25°C
TCR	Input/Output Impedance Tempco	2600ppm/°C
S(T)	Sensitivity	1.5mV/V psi at +25°C
TCS	Sensitivity Tempco	-2100ppm/°C
O(T)	Offset	12mV/V at +25°C
OTC	Offset Tempco	-1030 ppm-FSO/°C
S(p)	Sensitivity Linearity Error as % FSO BSLF (Best Straight-Line Fit)	0.1% FSO BSLF
P_{MIN}	Minimum Input Pressure	0 PSI
P_{MAX}	Maximum Input Pressure	10 PSI

Table 2. Compensation Components/Values

PARAMETER	DESCRIPTION
R_{ISRC}	Resistor that programs the nominal sensor excitation current
R_{STC}	Resistor that compensates FSO TC errors
A_{PGA}	Programmable-gain amplifier gain
OFFTC	Offset TC correction voltage, including its respective sign bit
R_{LIN}	Resistor that corrects FSO linearity errors (optional)

Table 3. PGA Gain Settings

PGA GAIN (V/V)	PGA VALUE	A2	A1	A0
39	0	0	0	0
65	1	0	0	1
91	2	0	1	0
117	3	0	1	1
143	4	1	0	0
169	5	1	0	1
195	6	1	1	0
221	7	1	1	1

$$A_{PGA} \approx \frac{OUTFSO}{SensorFSO} \approx \frac{4V}{0.0375V} = 106V/V$$

where OUTFSO is the desired calibrated transducer full-span output voltage, and SensorFSO is the sensor full-span output voltage at T1.

Determining OFFTC Initial Value

Generally, the OFFTC coefficient can be set to 0V, since the offset TC errors will be compensated in a later step. However, sensors with large offset TC errors may require an initial coarse offset TC adjustment to prevent the PGA from saturating as the temperature increases during the compensation procedure. An initial coarse offset TC adjustment would be required if the magnitude of the sensor offset TC error is more than about 10% of the FSO. If a coarse offset TC adjustment is required, use the following equation:

$$\text{OTC Correction} = \frac{\Delta V_{OUT(T)}}{\Delta V_{BDRIVE(T)} \times 1.15}$$

which can be approximated by:

$$\text{OTC Correction} \approx \frac{OTC \times FSO \times (\Delta T)}{TCS \times V_{BDRIVE} \times 1.15 \times (\Delta T)} \approx \frac{-1030ppm/°C \times 4V}{-2100 \times 2.5V \times 1.15} = 0.68$$

where OTC is the sensor offset TC error in ppm of FSO, ΔT is the operating temperature range in °C, and OTC Correction is the offset TC resistor-divider ratio. For positive values of OTC correction, connect SOTC to V_{DD}; for negative values, connect SOTC to V_{SS}.

Select the Offset TC resistor divider (R_{OTCA} and R_{OTCB}, Figure 4) using the following equation:

$$\text{OTC Correction} = \frac{R_{OTCA}}{R_{OTCA} + R_{OTCB}}$$

$$0.17 = \frac{R_{OTCA}}{R_{OTCA} + R_{OTCB}}$$

where $500k\Omega \geq (R_{OTCA} + R_{OTCB}) \geq 100k\Omega$. Choose $R_{OTCB} = 100k\Omega$ and $R_{OTCA} = 20k\Omega$.

Transfer Function

The following transfer function (linearity correction not included) is useful for data modeling or for developing compensative algorithms:

$$V_{OUT} = V_{BDRIVE} \times \left[V_S \times PGA + 1.15 \times \frac{V_{OFFTC}}{V_{DD}} \right] + 1.15 \times V_{OFFSET}$$

$$\text{where } V_{BDRIVE} = \frac{\frac{V_{DD}}{R_{ISRC}} + \frac{V_{DD}}{R_{STC}}}{\frac{1}{AA \times Rb(T)} + \frac{1}{R_{STC}}}$$

(AA = current source gain)

FSO Calibration

Perform FSO calibration at room temperature with a full-scale sensor excitation.

1) At +25°C (or T1), set $V_{FSOTRIM}$ to 2.5V. Adjust R_{ISRC} until V_{BBUF} = 2.5V.
2) Adjust V_{OFFSET} until the room temperature offset voltage is 0.5V (see *OFFSET Calibration* section).
3) Measure the full-span output (measuredV_{FSO}).
4) Calculate $V_{BIDEAL(25°C)}$ using the following equation:

$$V_{BIDEAL(25°C)} = V_{FSOTRIM}\left(1 + \frac{[\text{desired}V_{FSO}] - [\text{measured}V_{FSO}]}{[\text{measured}V_{FSO}]}\right)$$

Note: If $V_{BIDEAL(25°C)}$ is outside the allowable bridge voltage swing of (V_{SS} + 1.3V) to (V_{DD} - 1.3V), readjust the PGA gain setting. If $V_{BIDEAL(25°C)}$ is too low, decrease the PGA gain setting by one step and return to Step 1. If $V_{BIDEAL(25°C)}$ is too high, increase the PGA gain setting by one step and return to Step 1.

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5) Set $V_{FSOTRIM} = V_{BIDEAL(25°C)}$. Adjust R_{ISRC} until $V_{BBUF} = V_{BIDEAL(25°C)}$.

6) Readjust V_{OFFSET} until the offset voltage is 0.5V (see *OFFSET Calibration* section).

FSO TC Compensation

Correct linear span TC by connecting BBUF to ISRC through a resistor (R_{STC}). The value of R_{STC} depends on the required correction coefficient, which is sensor dependent, but typically around 100kΩ for most silicon PRTs. The following procedure results in FSO TC calibration:

1) Measure the full-span output at T2.

2) Use the equation from Step 4 of the *FSO Calibration* section to determine $V_{BIDEAL(T2)}$. While at T2, adjust R_{STC} until $V_{BBUF} = V_{BIDEAL(T2)}$.

3) Do not adjust V_{OFFSET} or V_{OFFTC}.

OFFSET TC Compensation

Connect OFFTC to a resistor divider between BBUF and V_{SS}. The divided-down V_{BBUF} is then fed into OFFTC and the appropriate polarity (designating whether V_{OFFTC} should be added or subtracted from the PGA output) is selected with SOTC.

1) At T2, remeasure the offset at V_{OUT}.

2) Use the following equation to determine the magnitude of $V_{OFFTC(T2)}$, and adjust R_{OTCA} accordingly. If V_{OFFTC} is negative, connect SOTC to V_{SS}. If V_{OFFTC} is positive, connect SOTC to V_{DD}. After OTC calibration, the output may be saturated; correct this condition during OFFSET calibration. In most cases Current OFFTC will be 0. However, if a coarse OFFTC adjustment was performed, the coefficient must be inserted in the equation below.

$$V_{OFFTC} = \frac{V_{OFFSET(T1)} - V_{OFFSET(T2)}}{\left(V_{BDRIVE(T1)} - V_{BDRIVE(T2)}\right)} \times 1.15 + \text{Current OFFTC}$$

where Current OFFTC is the voltage at pin OFFTC.

Note that the magnitude of V_{OFFTC} is directly proportional to the gain of the PGA. Therefore, if the PGA gain changes after performing the offset TC calibration, the offset TC must be recalibrated.

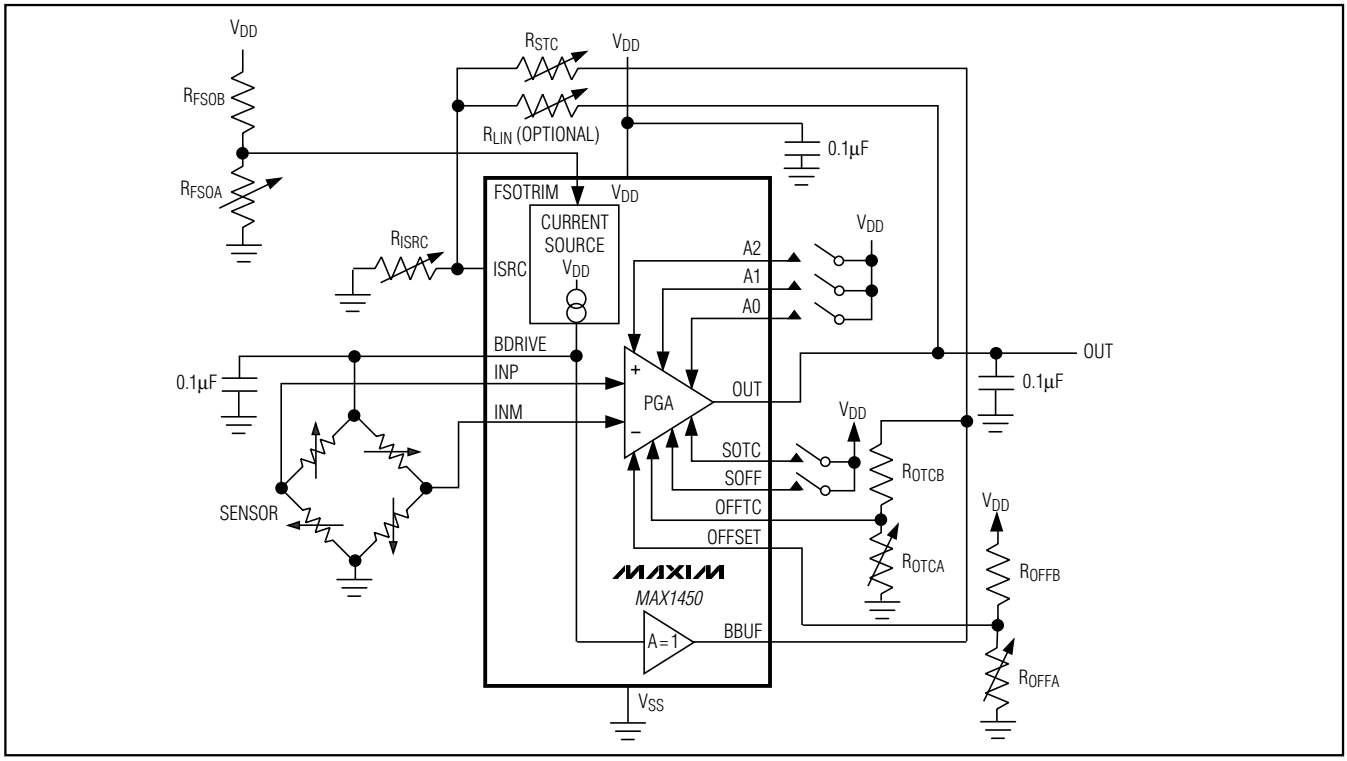

Figure 4. Basic Ratiometric Output Configuration

OFFSET Calibration

Accomplish offset calibration by applying a voltage to the OFFSET pin (SOFF determines the polarity of V_{OFFSET}). This voltage is generated by a resistor-divider between V_{DD} and V_{SS} (R_{OFFA} and R_{OFFB} in Figure 4). To calibrate the offset, set V_{OFFSET} to 0 and perform a minimum pressure input reading at room temperature. If the output voltage ($V_{OFFZERO}$) is greater than 0.5V, connect SOFF to V_{SS}; if $V_{OFFZERO}$ is less than 0.5V, connect SOFF to V_{DD}. Adjust V_{OFFSET} until V_{OUT} = 0.5V.

Note that the magnitude of V_{OFFSET} is directly proportional to the gain of the PGA. Therefore, if the PGA gain changes after performing the offset calibration, the offset must be recalibrated.

Linearity Calibration (optional)

Correct pressure linearity by using feedback from the output voltage (V_{OUT}) to ISRC to modulate the current source. If a bridge current is constant with applied pressure, sensor linearity remains unaffected. If, with a constant bridge current, the output voltage is nonlinear with applied pressure (e.g., increasing faster than the pressure), use pressure linearity correction to linearize the output.

Performing linearity corrections through the use of a transfer function is not practical, since a number of required system variables cannot easily be measured with a high enough degree of accuracy. Therefore, use a simple empirical approach. Figure 5 shows the uncompensated pressure linearity error of a silicon PRT. The magnitude of this error is usually well below 1% of span. Curves A, B, C, D, E, and F in Figure 5 represent increasing amounts of linearity error corrections, corresponding to decreasing values in the resistance of R_{LIN}. To correct pressure linearity errors, use the following equation to determine the appropriate range for R_{LIN}:

$$R_{LIN} \approx \frac{2\ R_{ISRC}\ x\ R_{STC}}{(R_{ISRC}\ +\ R_{STC})\ x\ S(p)}$$

where S(p) is the sensitivity linearity error as % best straight-line fit (BSLF). Ideally, this variable resistor should be disconnected during temperature error compensation. If this is not possible, set it to the maximum available value.

First measure the magnitude of the uncorrected error (R_{LIN} = maximum value), then choose an arbitrary value for R_{LIN} (approximately 50% of maximum value). Measuring the new linearity error establishes a linear relationship between the amount of linearity correction and the value of R_{LIN}.

Note that if pressure linearity correction is to be performed, it must occur after temperature compensation is completed. A minor readjustment to the FSO and OFFSET will be required after linearity correction is performed. If pressure linearity correction is not required, remove R_{LIN}.

Ratiometric Output Configuration

Ratiometric output configuration provides an output that is proportional to the power-supply voltage. When used with ratiometric A/D converters, this output provides digital pressure values independent of supply voltage. Most automotive and some industrial applications require ratiometric outputs.

The MAX1450 has been designed to provide a high-performance ratiometric output with a minimum number of external components (Figure 4).

Sensor Calibration and Compensation Example

Calibration and compensation requirements for a sensor involve conversion of a sensor-specific performance into a normalized output curve. Table 4 shows an example of the MAX1450's capabilities.

A repeatable piezoresistive sensor with an initial offset of 30mV and FSO of 37.5mV was converted into a compensated transducer (using the piezoresistive sensor with the MAX1450) with an offset of 0.5V and an FSO of 4.0V. The temperature errors, which were on the order of -17% for the offset TC and -35% for the FSO TC, were reduced to about ±1% FSO. The graphs of Figure 6 show the outputs of the uncompensated sensor and the compensated transducer.

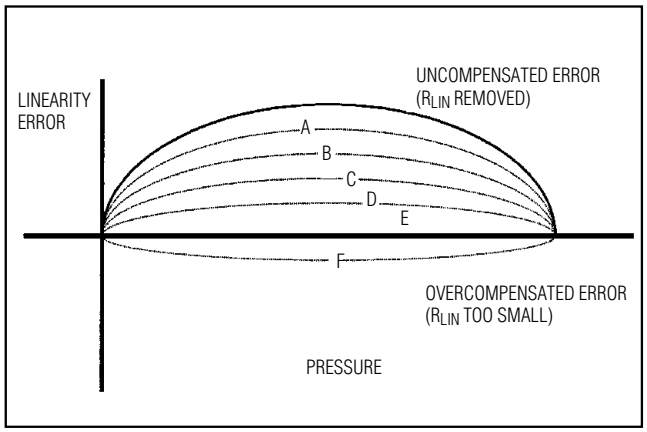

Figure 5. Effect of R_{LIN} on Linearity Corrections

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Table 4. MAX1450 Calibration and Compensation

Typical Uncompensated Input (Sensor)	Typical Compensated Transducer Output
Offset .....±80% FSO FSO .....15mV/V Offset TC .....-17% FSO Offset TC Nonlinearity .....1% FSO FSO TC.....-35% FSO FSO TC Nonlinearity.....1% FSO Temperature Range.....-40°C to +125°C	V_{OUT} .....Ratiometric to V_{DD} at 5.0V Offset at +25°C .....0.500V ±5mV FSO at +25°C .....4.000V ±5mV Offset Accuracy Over Temp. Range.....±60mV (1.5% FSO) FSO Accuracy Over Temp. Range .....±60mV (1.5% FSO)

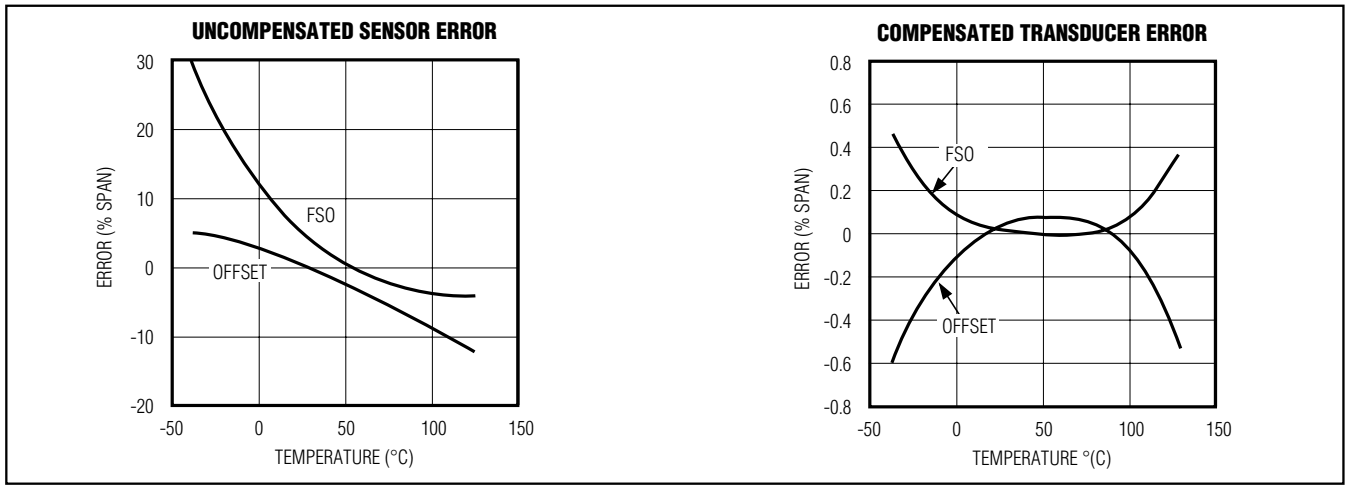


Figure 6. Comparison of an Uncalibrated Sensor and a Temperature-Compensated Transducer

Chip Information

TRANSISTOR COUNT: 1364

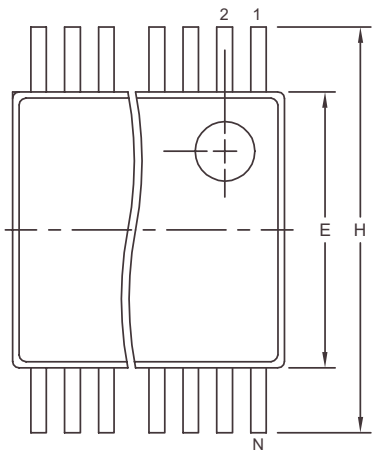
SUBSTRATE CONNECTED TO V_{SS}

Low-Cost, 1%-Accurate Signal Conditioner for Piezoresistive Sensors

Package Information

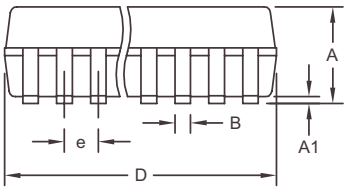
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

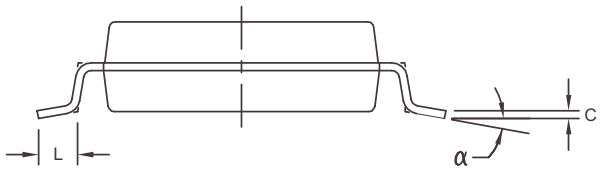
SSOP.EPS



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.004	0.008	0.09	0.20
D	SEE VARIATIONS			
E	0.205	0.212	5.20	5.38
e	0.0256 BSC		0.65 BSC	
H	0.301	0.311	7.65	7.90
L	0.025	0.037	0.63	0.95
α	0∞	8∞	0∞	8∞

	INCHES		MILLIMETERS		
	MIN	MAX	MIN	MAX	N
D	0.239	0.249	6.07	6.33	14L
D	0.239	0.249	6.07	6.33	16L
D	0.278	0.289	7.07	7.33	20L
D	0.317	0.328	8.07	8.33	24L
D	0.397	0.407	10.07	10.33	28L





NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15 MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO150.
5. LEADS TO BE COPLANAR WITHIN 0.10 MM.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, SSOP, 5.3 MM

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0056	C	1/1