The Future of Analog IC Technology

MP2223

18V, Dual-Channel 3A/2A, 540kHz, Synchronous, Step-Down Converter in 8-Pin TSOT23 Package

DESCRIPTION

The MP2223 is a dual-channel, synchronous, rectified, step-down, switch-mode converter with built-in, internal power MOSFETs. The MP2223 offers a very compact solution that achieves 3A/2A of continuous output current over a wide input supply range.

Two channels operate 180° out-of-phase to minimize the input capacitor and alleviate EMI. Current-mode operation provides fast transient response and eases loop stabilization. Full protection features include hiccup mode over-current protection (OCP) and thermal shutdown.

Other features include power-save mode (PSM) at light load and a separate enable control (EN) for power-sequence control.

The MP2223 requires a minimal number of readily available, standard, external components and is available in a space saving 8-pin TSOT23 package.

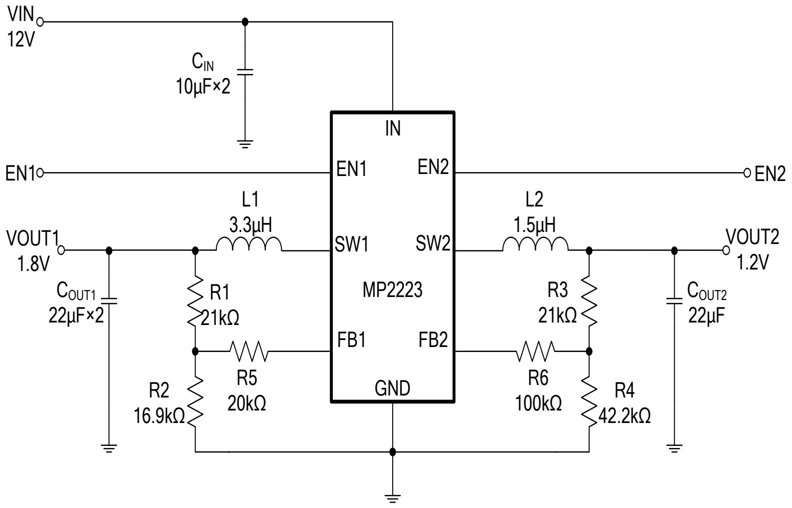
FEATURES

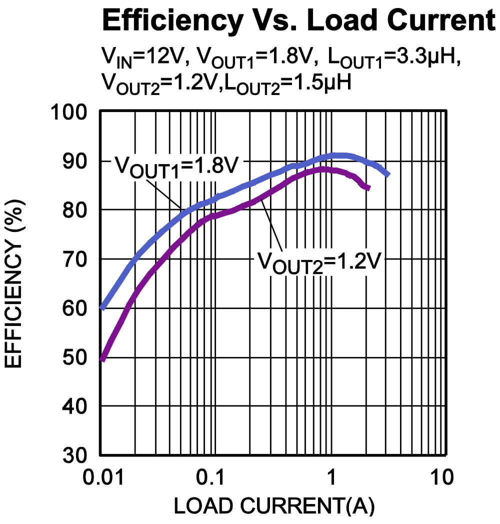
- Wide 4.5V to 18V Operating Input Range
- 70mΩ/50mΩ for Ch1, 100mΩ/60mΩ for Ch2, Low $R_{DS(ON)}$ Internal Power MOSFETs
- Up to 3A (Ch1) and 2A (Ch2) Maximum Continuous Output Current
- 180° Out-of-Phase Operation
- Power-Save Mode for Light Load
- 540kHz Fixed Switching Frequency
- Over-Current Protection (OCP) and Hiccup
- Over-Voltage Protection (OVP)
- Thermal Shutdown
- Both Channel Outputs Adjustable from 0.8V
- Available in a TSOT23-8 Package

APPLICATIONS

- Notebook Systems and I/O Power
- Digital Set-Top Boxes
- DSL Modems
- Flat-Panel Televisions and Monitors
- Distributed Power Systems

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2223GJ	TSOT23-8	*See Below*

* For Tape & Reel, add suffix –Z (e.g.: MP2223GJ–Z).

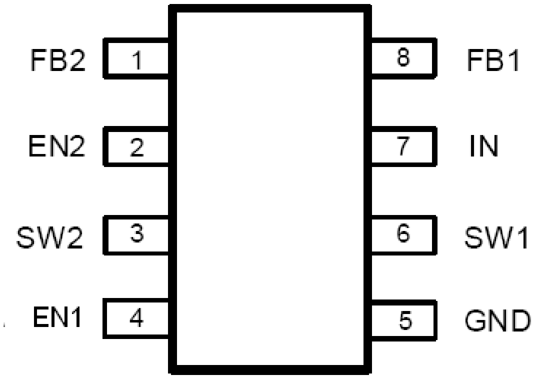
TOP MARKING

|ARAY

ARA: Product code of MP2223GJ
Y: Year code

PACKAGE REFERENCE

TOP VIEW



TSOT23-8

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} .... -0.3V to 20V
V_{SW1}, V_{SW2} .... -0.3V (-5V for <10ns)
to V_{IN} + 0.7V (24V for <10ns)
V_{EN1}, V_{EN2} .... -0.3V to 20V
All other pins .... -0.3V to 5V
Continuous power dissipation (T_A = +25°C) (2)
.... 1.25W
Junction temperature .... 150°C
Lead temperature .... 260°C
Storage temperature .... -65°C to 150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .... 4.5V to 18V
Output voltage (V_{OUT1}) .... 0.8V to V_{IN} * D_{MAX} V
Output voltage (V_{OUT2}) .... 0.8V to V_{IN} * D_{MAX} V
Operating junction temp. (T_J) ... -40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
TSOT23-8	100	55	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, f_{SW} = 500kHz, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{IN}	$V_{EN1} = V_{EN2} = 0V$			10	μA
Supply current (no switching quiescent)	I_Q	$V_{EN1} = V_{EN2} = 2V$, $V_{FB1} = V_{FB2} = 1V$		1		mA
Ch1 HS switch on resistance	$HS1_{RDS(ON)}$			70		mΩ
Ch1 LS switch on resistance	$LS1_{RDS(ON)}$			50		mΩ
Ch2 HS switch on resistance	$HS2_{RDS(ON)}$			100		mΩ
Ch2 LS switch on resistance	$LS1_{RDS(ON)}$			60		mΩ
Switch leakage	SW_{LKG}	$V_{EN} = 0V$, $V_{SW} = 12V$			1	μA
Ch1 current limit	$I_{LIMIT-CH1}$	Duty = 40%	3.5	5.4		A
Ch2 current limit	$I_{LIMIT-CH2}$	Duty = 40%	2.5	4.4		A
Zero-crossing current limit	I_{ZCD}			-50		mA
Oscillator frequency	f_{SW}		420	540	660	KHz
Maximum duty cycle	D_{MAX}	V_{FB} = 700mV		89		%
Minimum on time (5)	$T_{ON\ MIN}$			110		ns
Feedback voltage	V_{FB}	T_A = 25°C	-1.5%	800	+1.5%	mV
EN rising threshold	$V_{EN\ RISING}$		1.09	1.25	1.41	V
EN falling threshold	$V_{EN\ FALLING}$		0.95	1.08	1.21	V
V_{IN} UVLO rising			3.9	4.1	4.3	V
UVLO hysteresis				250		mV
Output OVP threshold	V_{OVP}			123%		V_{REF}
OVP threshold hysteresis	$V_{OVP\ HYS}$			15%		V_{REF}
Ch1 soft-start time	I_{SS1}			0.8		ms
Ch2 soft-start time	I_{SS2}			0.8		ms
Thermal shutdown (6)	T_{SD}			150		°C
Thermal hysteresis (6)	$T_{SD\ HYS}$			20		°C

NOTES:

5) Guaranteed by characterization.

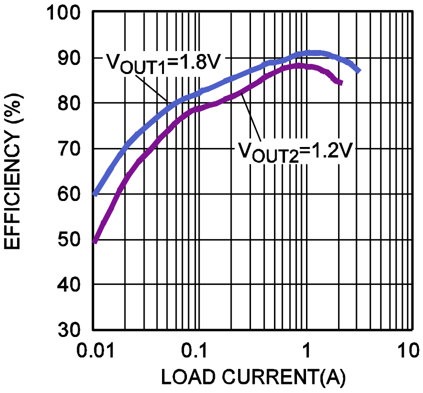
6) Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L_{OUT1} = 3.3µH, L_{OUT2} = 1.5µH, T_A = 25°C, unless otherwise noted.

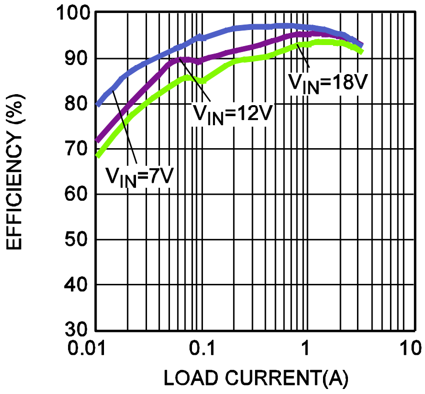
Efficiency Vs. Load Current

V_{IN}=12V, V_{OUT1}=1.8V, L_{OUT1}=3.3µH, V_{OUT2}=1.2V, L_{OUT2}=1.5µH



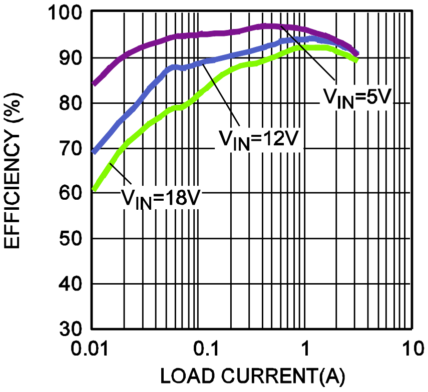
Efficiency Vs. Load Current

CH1, V_{OUT1}=5V, L_{OUT1}=6.5µH, DCR=21.5mohm



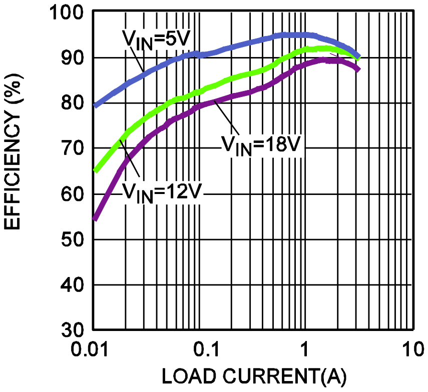
EfficiencyVs. Load Current

CH1, V_{OUT1}=3.3V, L_{OUT1}=6.5µH, DCR=21.5mohm



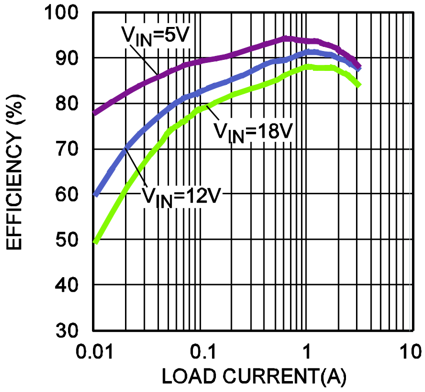
Efficiency Vs. Load Current

CH1, V_{OUT1}2.5V, L_{OUT1}=3.3µH, DCR=9mohm



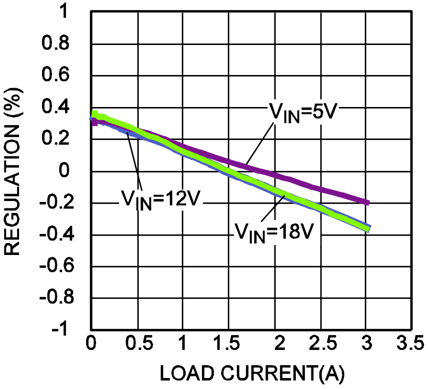
Efficiency Vs. Load Current

CH1, V_{OUT1}=1.8V, L_{OUT1}=3.3µH, DCR=9mohm



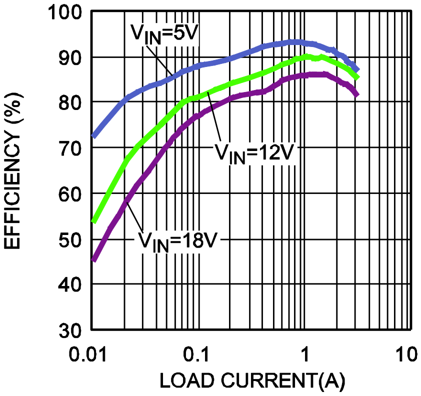
Load Regulation

CH1, V_{IN}=5V to 18V, V_{OUT}=1.8V, I_{OUT}=0A to 3A



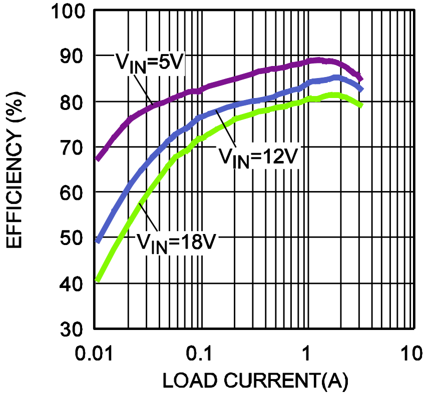
Efficiency Vs. Load Current

CH1, V_{OUT1}=1.5V, L_{OUT1}=3.3µH, DCR=9mohm



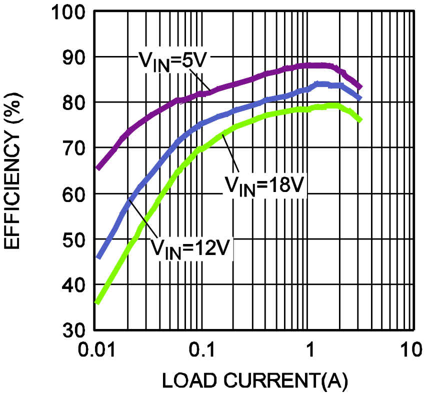
Efficiency Vs. Load Current

CH1, V_{OUT1}=1.2V, L_{OUT1}=1.0µH, DCR=4.6mohm



Efficiency Vs. Load Current

CH1, V_{OUT1}=1.0V, L_{OUT1}=1.0µH, DCR=4.6mohm

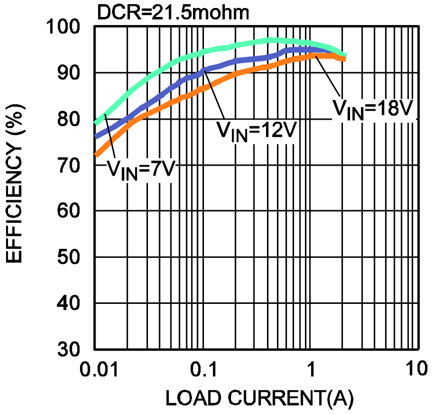


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L_{OUT1} = 3.3μH, L_{OUT2} = 1.5μH, T_A = 25°C, unless otherwise noted.

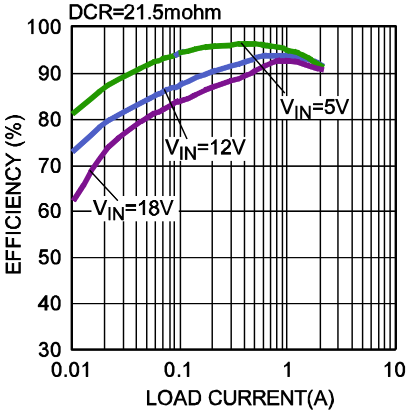
Efficiency Vs. Load Current

CH2, V_{OUT2}=5V, L_{OUT2}=6.5μH, DCR=21.5mohm



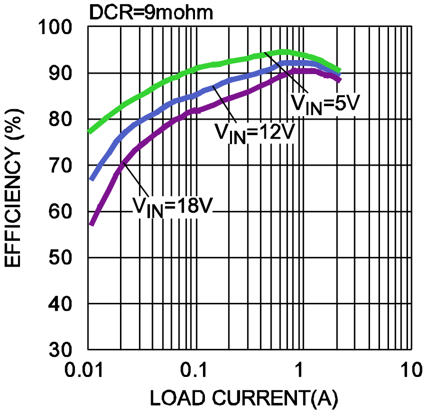
Efficiency Vs. Load Current

CH2, V_{OUT2}=3.3V, L_{OUT2}=6.5μH, DCR=21.5mohm



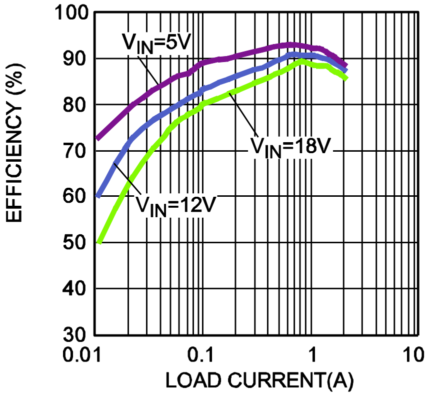
Efficiency Vs. Load Current

CH2, V_{OUT2}=2.5V, L_{OUT2}=3.3μH, DCR=9mohm



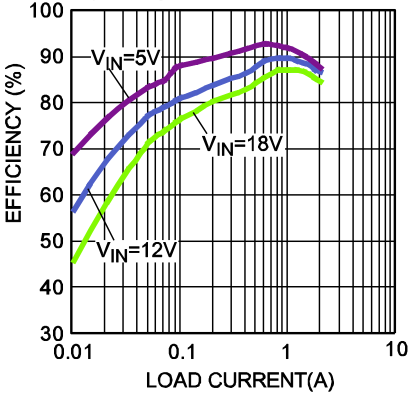
Efficiency Vs. Load Current

CH2, V_{OUT2}=1.8V, L_{OUT2}=3.3μH, DCR=9mohm



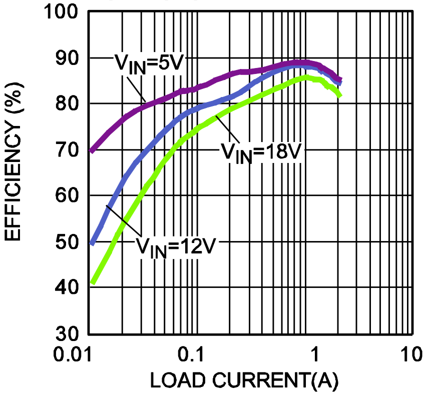
Efficiency Vs. Load Current

CH2, V_{OUT2}=1.5V, L_{OUT2}=3.3μH, DCR=9mohm



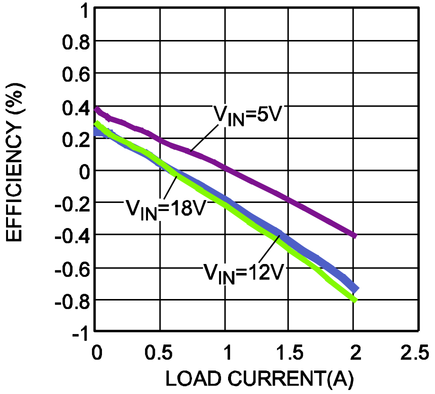
Efficiency Vs. Load Current

CH2, V_{OUT2}=1.2V, L_{OUT2}=1.5μH, DCR=4.3mohm



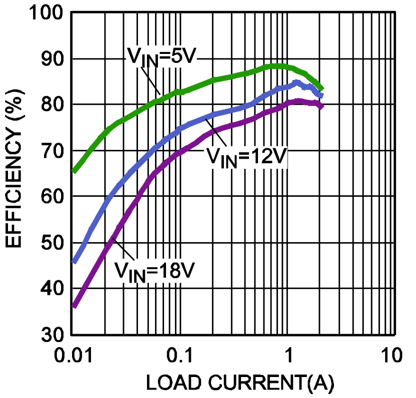
Load Regulation

CH2, V_{IN}=5V to 18V, V_{OUT}=1.2V, I_{OUT}=0A to 2A



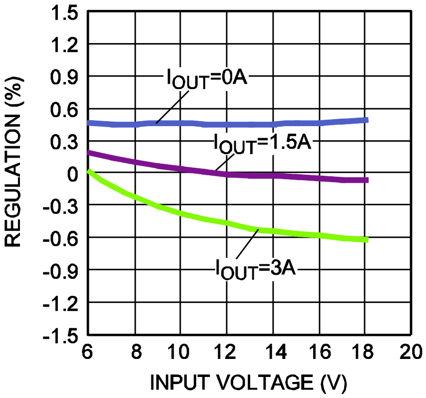
Efficiency Vs. Load Current

CH2, V_{OUT2}=1.0V, L_{OUT2}=1.5μH, DCR=4.3mohm



Line Regulation

CH1, V_{OUT1}=3.3V,V_{IN}=6V to 18V

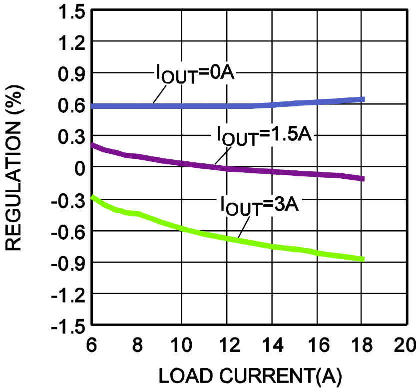


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

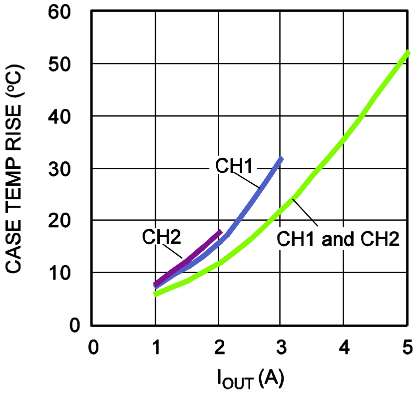
V_{IN} = 12V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L_{OUT1} = 3.3µH, L_{OUT2} = 1.5µH, T_A = 25°C, unless otherwise noted.

Line Regulation

CH2, V_{OUT2}=3.3V,V_{IN}=6V to 18V

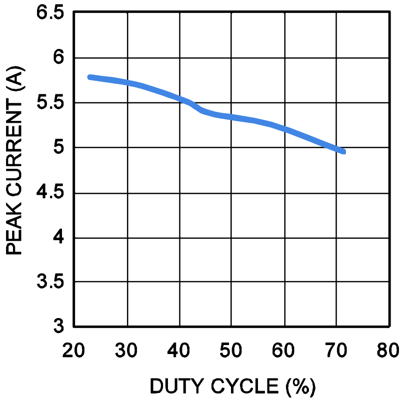


Case Temp Rise



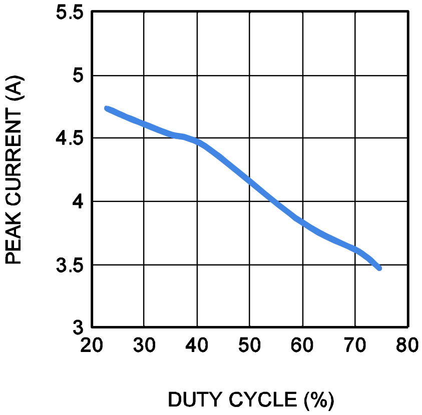
Peak Current Vs. Duty Cycle

CH1, V_{OUT1}=5V



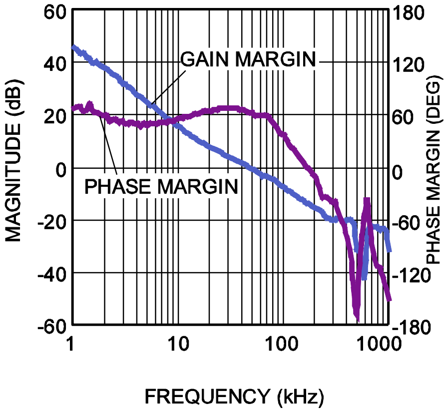
Peak Current Vs. Duty Cycle

CH2, V_{OUT2}=5V



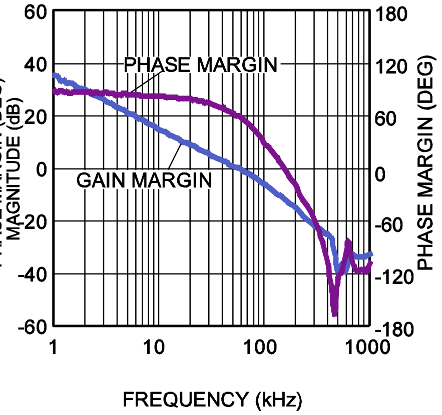
Bode Plot

CH1, V_{OUT1}=1.8V



Bode Plot

CH1, V_{OUT1}=1.2V

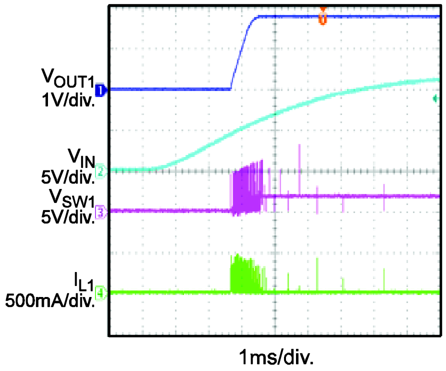


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L_{OUT1} = 3.3µH, L_{OUT2} = 1.5µH, T_A = 25°C, unless otherwise noted.

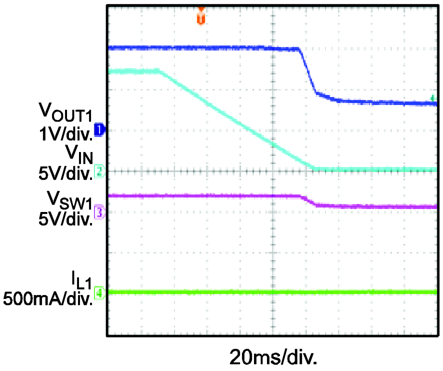
Startup through Input Voltage (CH1)

I_{OUT} = 0A



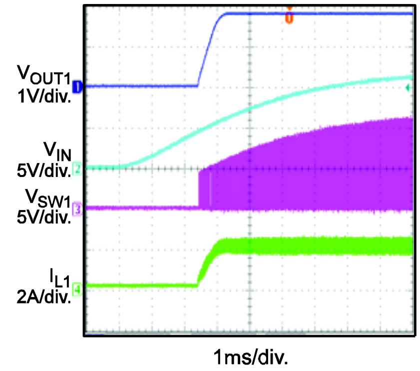
Shutdown through Input Voltage (CH1)

I_{OUT} = 0A



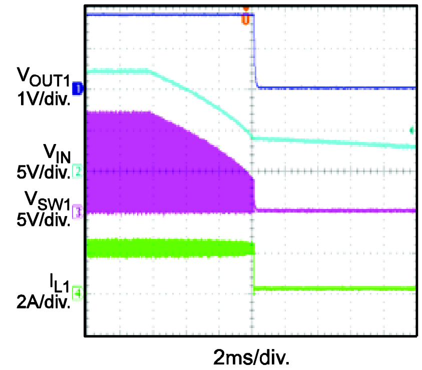
Startup through Input Voltage (CH1)

I_{OUT} = 3A



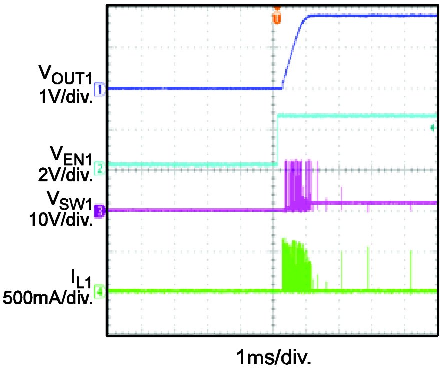
Shutdown through Input Voltage (CH1)

I_{OUT} = 3A



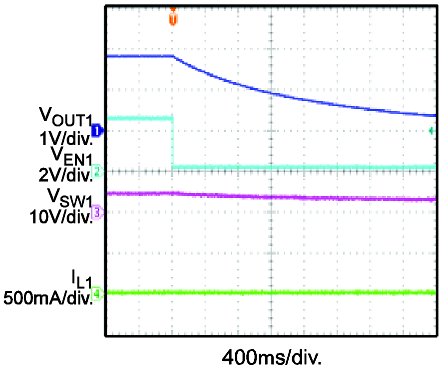
Startup through Enable (CH1)

I_{OUT} = 0A



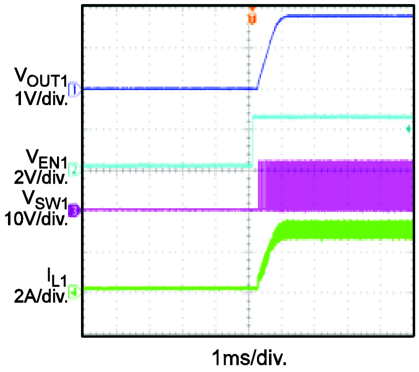
Shutdown through Enable (CH1)

I_{OUT} = 0A



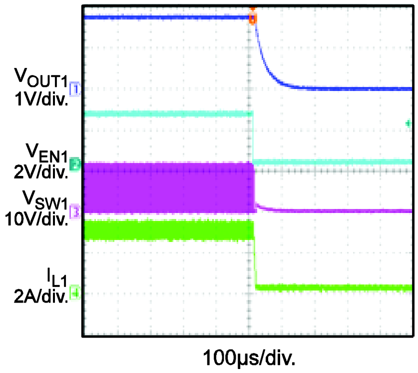
Startup through Enable (CH1)

I_{OUT} = 3A



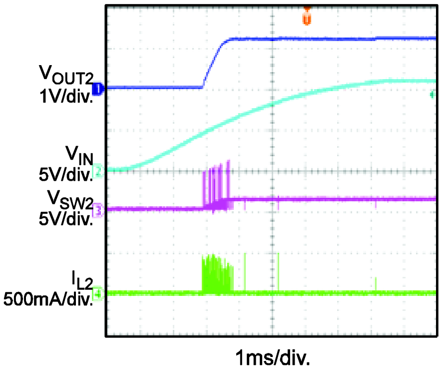
Shutdown through Enable (CH1)

I_{OUT} = 3A



Startup through Input Voltage (CH2)

I_{OUT} = 0A

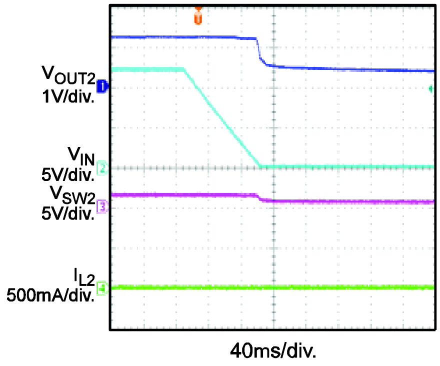


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L_{OUT1} = 3.3µH, L_{OUT2} = 1.5µH, T_A = 25°C, unless otherwise noted.

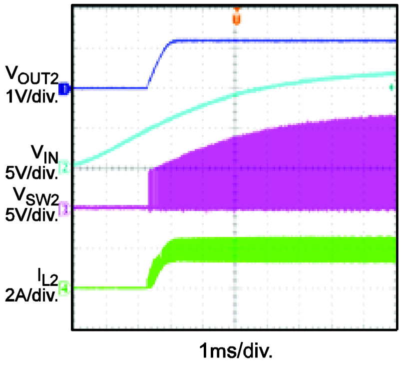
Shutdown through Input Voltage (CH2)

I_{OUT} = 0A



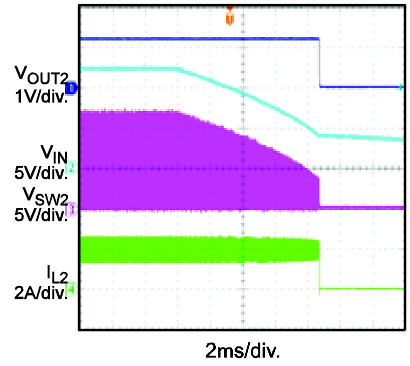
Startup through Input Voltage (CH2)

I_{OUT} = 2A



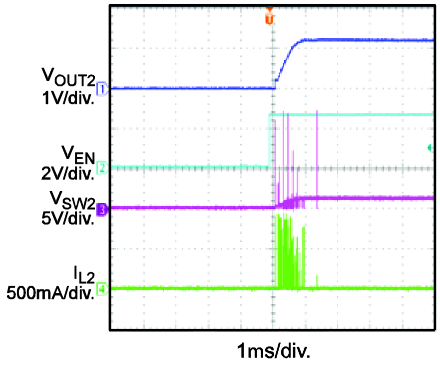
Shutdown through Input Voltage (CH2)

I_{OUT} = 2A



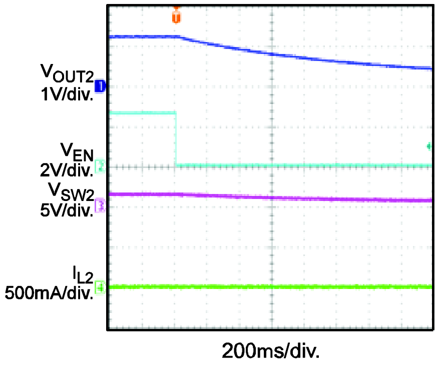
Startup through Enable (CH2)

I_{OUT} = 0A



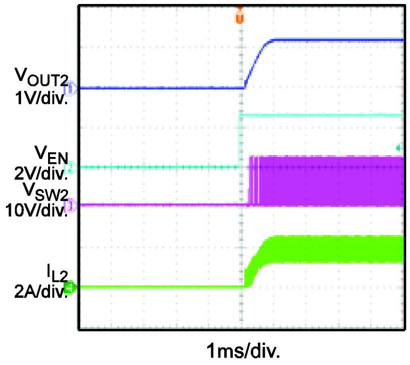
Shutdown through Enable (CH2)

I_{OUT} = 0A



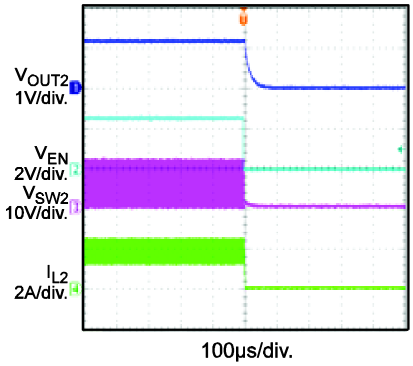
Startup through Enable (CH2)

I_{OUT} = 2A



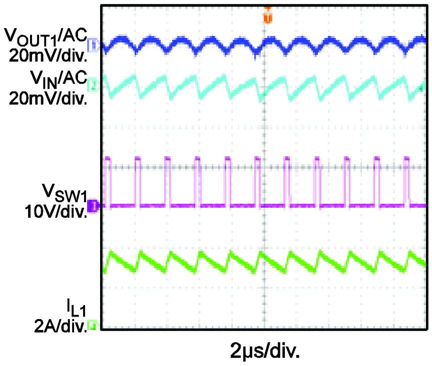
Shutdown through Enable (CH2)

I_{OUT} = 2A



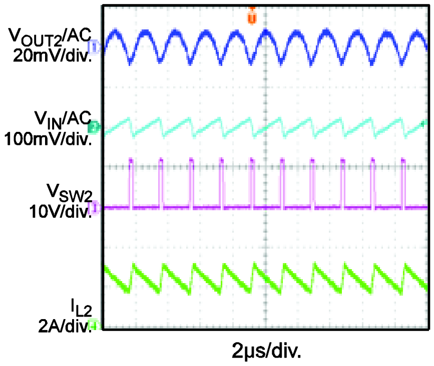
Input/Output Ripple (CH1)

I_{OUT} = 3A



Input/Output Ripple (CH2)

I_{OUT} = 2A

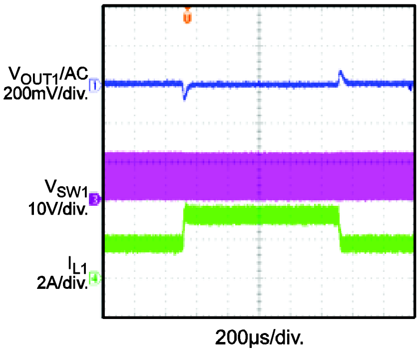


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L_{OUT1} = 3.3µH, L_{OUT2} = 1.5µH, T_A = 25°C, unless otherwise noted.

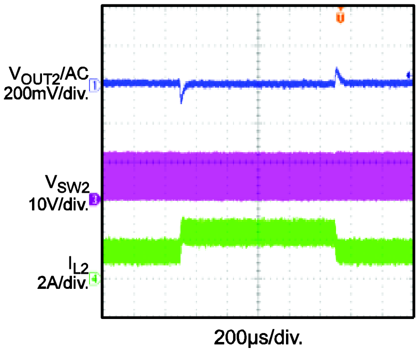
Transient Response (CH1)

I_{OUT} = 1.5A to 3A, 2.5A/µs



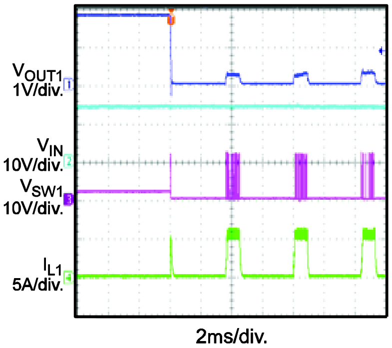
Transient Response (CH2)

I_{OUT} = 1A to 2A, 2.5A/µs



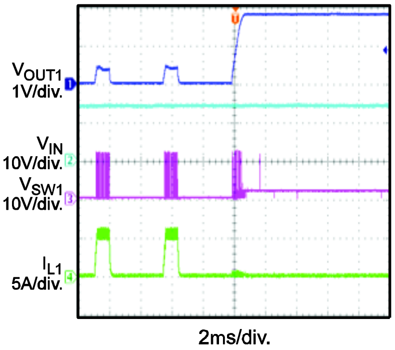
Short Circuits Entry (CH1)

I_{OUT} = 0A



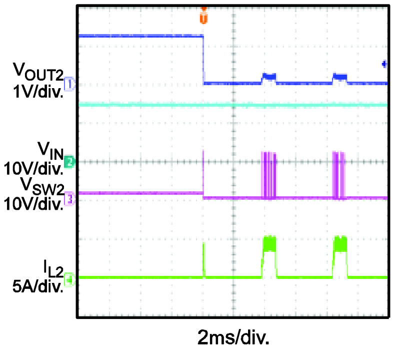
Short Circuits Recovery (CH1)

I_{OUT} = 0A



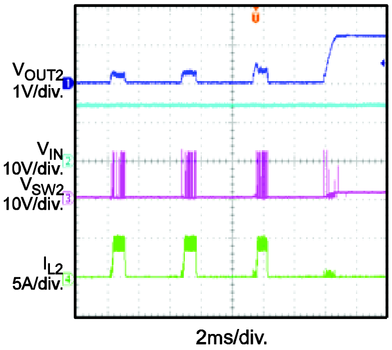
Short Circuits Entry (CH2)

I_{OUT} = 0A



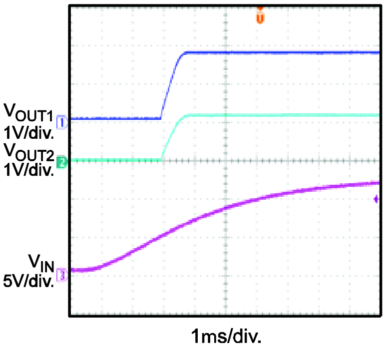
Short Circuits Recovery (CH2)

I_{OUT} = 0A



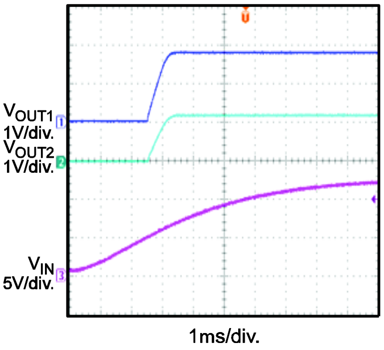
Startup through Input Voltage (Both CH1 and CH2 On)

I_{OUT1} = 0A and I_{OUT2} = 0A



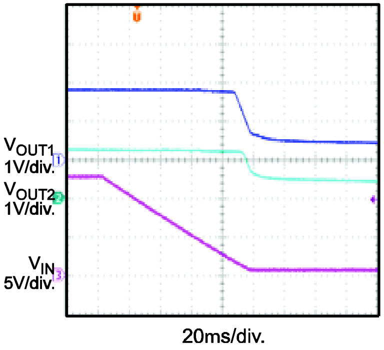
Startup through Input Voltage (Both CH1 and CH2 On)

I_{OUT1} = 3A and I_{OUT2} = 2A



Shutdown through Input Voltage (Both CH1 and CH2 On)

I_{OUT1} = 0A and I_{OUT2} = 0A

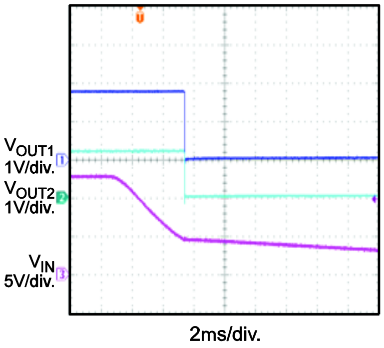


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L_{OUT1} = 3.3µH, L_{OUT2} = 1.5µH, T_A = 25°C, unless otherwise noted.

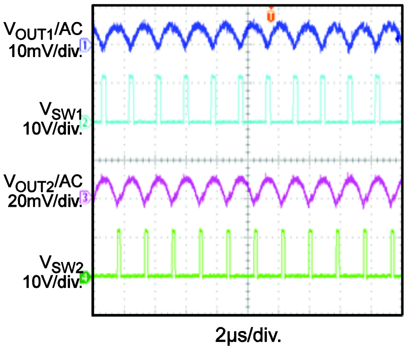
Shutdown through Input Voltage (Both CH1 and CH2 On)

I_{OUT1} = 3A and I_{OUT2} = 2A



Input/Output Ripple (Both CH1 and CH2 On)

I_{OUT1} = 3A and I_{OUT2} = 2A



PIN FUNCTIONS

Package Pin #	Name	Description
1	FB2	**Feedback for buck 2.** Connect FB2 to the tap of an external resistor divider from the output to GND to set the output voltage. The comparator lowers the oscillator frequency when the FB voltage drops below 400mV to prevent current-limit runaway during a short-circuit fault.
2	EN2	**Enable input for buck 2.** Drive EN2 high to enable the MP2223. Drive EN2 low to disable the MP2223. Do not float EN2.
3	SW2	**Switch output for buck 2.** Connect SW2 using a wide PCB trace.
4	EN1	**Enable input for buck 1.** Drive EN1 high to enable the MP2223. Drive EN1 low to disable the MP2223. Do not float EN1.
5	GND	**Power ground.**
6	SW1	**Switch output for buck 1.** Connect SW1 using a wide PCB trace.
7	IN	**Supply voltage.** Use a 22µF ceramic capacitor to decouple the input rail. Connect IN using a wide PCB trace.
8	FB1	**Feedback for buck 1.** Connect FB1 to the tap of an external resistor divider from the output to GND to set the output voltage. The comparator lowers the oscillator frequency when the FB voltage drops below 400mV to prevent current-limit runaway during a short-circuit fault.

BLOCK DIAGRAM

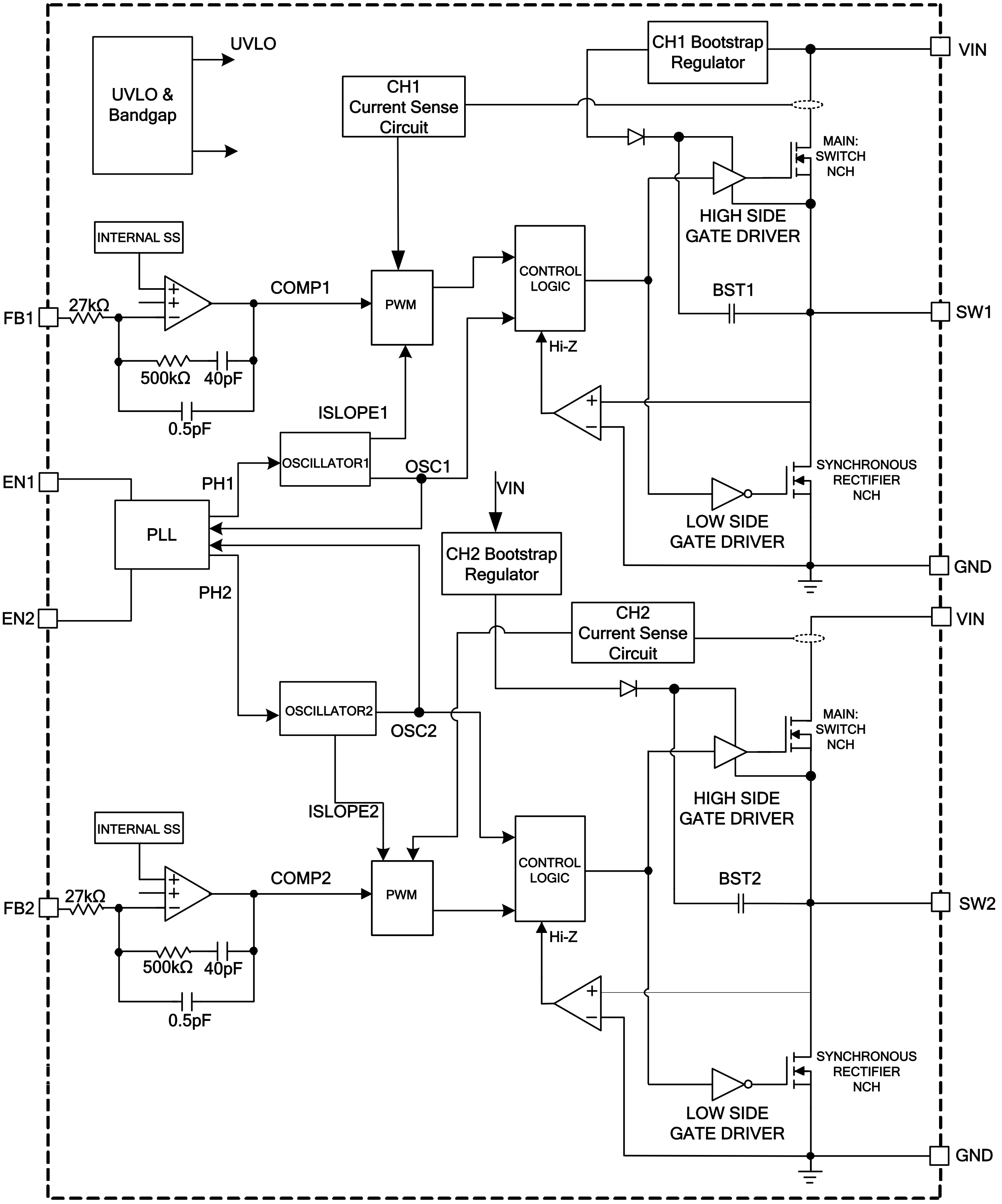


Figure 1: Functional Block Diagram

OPERATION

The MP2223 is a high-frequency, synchronous, rectified, step-down, switch-mode converter with built-in power MOSFETs. The MP2223 offers a very compact solution that achieves 2A and 3A of continuous output current with excellent load and line regulation over a wide input supply range.

The MP2223 has three working modes: advanced asynchronous mode (AAM), discontinuous conduction mode (DCM), and continuous conduction mode (CCM). The device switches from AAM to DCM to CCM as the load current increases. In some particular specs, the device may enter CCM directly from AAM without entering DCM.

AAM Control Operation

In the light-load condition, the MP2223 works in AAM (see Figure 2). The AAM voltage (V_{AAM}) is an internal, fixed voltage when the input and output voltages are fixed. The COMP voltage (V_{COMP}) is the error amplifier output, which represents the peak inductor current information. When V_{COMP} is lower than V_{AAM}, the internal clock is blocked, so the MP2223 skips some pulses and achieves light-load power saving. Refer to the application note AN032 “Advanced Asynchronous Modulation Application Note” for more detail.

The internal clock resets whenever V_{COMP} is higher than V_{AAM}. Simultaneously, the high-side MOSFET (HS-FET) turns on and remains on until $V_{ILsense}$ reaches the value set by V_{COMP}.

The light-load feature in this device is optimized for 12V input applications.

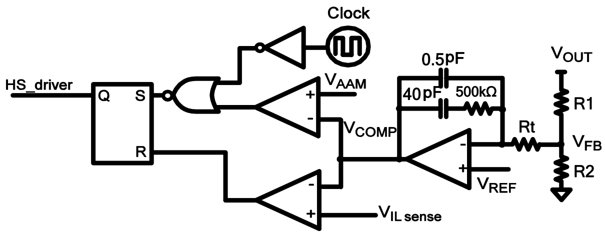


Figure 2: Simplified AAM Control Logic

DCM Control Operation

V_{COMP} ramps up as the output current increases. When its minimum value exceeds V_{AAM}, the device enters DCM (see Figure 3). In this mode, the internal 500kHz clock initiates the pulse-width modulation (PWM) cycle, the HS-FET turns on and remains on until $V_{ILsense}$ reaches the value set by V_{COMP}. After a dead-time period, the low-side MOSFET (LS-FET) turns on and remain on until the inductor current value decreases to zero. The device repeat this operation during every clock cycle to regulate the output voltage.

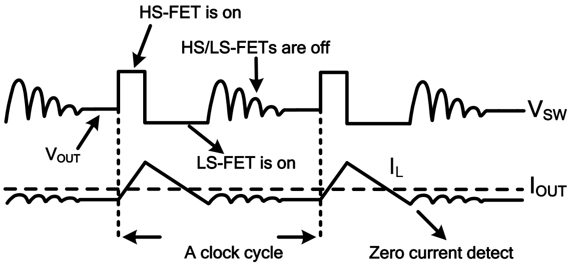


Figure 3: DCM Control Operation

CCM Control Operation

When the inductor current no longer drops to zero in a clock cycle, the device enters CCM from DCM. In CCM, the internal 500kHz clock initiates the PWM cycle, the HS-FET turns on and remains on until $V_{ILsense}$ reaches the value set by V_{COMP} (after a dead-time period), and the LS-FET turn on and remains on until the next clock cycle begins. The device repeats this operation during every clock cycle to regulate the output voltage.

If $V_{ILsense}$ does not reach the value set by V_{COMP} within 89% of one PWM period, the HS-FET is forced off.

180° Phase Shift

When both channels work in CCM, the MP2223’s two channels operate at a 180° phase-shift to reduce the input current ripple. The smaller current ripple allows for a smaller input bypass capacitor. In CCM, two internal clocks control the switching. The high-side MOSFET turns on at the corresponding CLK’s rising edge (see Figure 4).

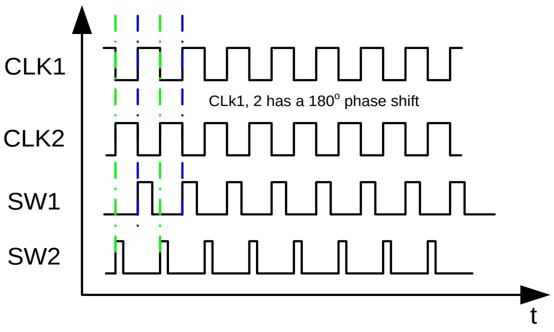


Figure 4: Clock/Switching Timing

However, when one or both channels work in AAM, its frequency drops below the internal clock, and the two channels will not work in 180° phase shift.

Error Amplifier (EA)

The error amplifier compares the FB voltage (V_{FB}) against the internal 0.8V reference (V_{REF}) and outputs a V_{COMP} value, which controls the power MOSFET current. The optimized internal compensation network minimizes the external component count and simplifies the control loop design.

Enable (EN1/2)

EN1/2 is a digital control pin that turns the regulator on and off. Drive EN1/2 high to turn on the regulator. Drive EN1/2 low to turn off the regulator. EN1/2 can operate with an 18V input voltage, which allows EN1/2 to be connected to V_{IN} directly for automatic start-up. EN1/2 cannot be floated. EN1 and EN2 are used to control Ch1 and Ch2 on/off respectively.

Over-Voltage Protection (OVP)

The MP2223 monitors the resistor-divided feedback voltage to detect an over-voltage (OV) condition when the feedback voltage rises above 123% of the target voltage. The LS-FET remains on until the low-side current drops to the negative current-limit threshold. This discharges the output and keeps it within the normal range. The device exits this regulation period when V_{FB} drops below 108% of V_{REF}.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MP2223 UVLO comparator monitors the output voltage of the internal regulator (VCC). The UVLO rising threshold is about 4.1V, and its falling threshold is 3.9V.

Soft Start (SS)

Soft start prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a soft-start voltage (SS) that ramps up from 0V to 1.2V. When SS is lower than REF, the error amplifier uses SS as the reference. When SS is higher than REF, the error amplifier uses REF as the reference.

Pre-Bias Start-Up

The MPM2223 is designed for monotonic start-up into a pre-biased output voltage. If the output is pre-biased to a certain voltage during start-up, the voltage on the soft-start capacitor is charged. When the soft-start capacitor's voltage exceeds the sensed output voltage at FB, the part turns on the high-side and low-side power switches sequentially. The output voltage starts to ramp up following the soft-start slew rate.

Over-Current Protection (OCP) and Hiccup

The MP2223 implements a cycle-by-cycle over-current (OC) limit when the inductor current peak value exceeds the set current-limit threshold. Meanwhile, the output voltage drops until FB is below the under-voltage (UV) threshold (typically 50% below the reference). Once UV is triggered, the MP2223 enters hiccup mode to restart the part periodically. This protection mode is especially useful when the output is dead-shorted to ground. The average short-circuit current is reduced greatly to alleviate thermal issues and protect the regulator. The MP2223 exits hiccup mode once the over-current condition is removed.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperatures exceeds 150°C, the entire chip shuts down. When the temperature is below its lower threshold (typically 130°C), the chip is enabled again.

Start-Up and Shutdown

If both V_{IN} and EN exceed their respective thresholds, the chip starts up. The reference block starts first, generating a stable reference voltage and current, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Three events can shut down the chip: EN low, V_{IN} low, and thermal shutdown. In the shutdown procedure, the signaling path is blocked first to avoid any fault triggering. V_{COMP} and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets the output voltage. The feedback resistors R1 and R3 set the feedback loop bandwidth with the internal compensation capacitor. R2 and R4 can then be calculated with Equation (1):

$$R2(R4)=\frac{R1(R3)}{\frac{V_{OUT1}(V_{OUT2})}{0.8V}-1} \qquad (1)$$

The feedback network shown in Figure 5 is highly recommended when V_{OUT} is low.

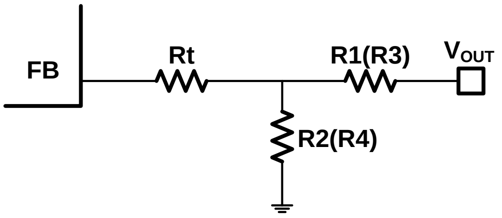


Figure 5: Feedback Network

Table 1 lists the recommended feedback resistor values for common output voltages.

Table 1: Resistor Selection for Common Output Voltages (7)

	V_{OUT1} (V)	R1 (kΩ)	R2 (kΩ)	Rt (kΩ)	L_{OUT} (µH)	C_{OUT} (µF)
Ch1	1.0	21	84.5	40.2	1.0	44
	1.2	21	42.2	40.2	1.0	44
	1.5	21	24	20	3.3	44
	1.8	21	16.9	20	3.3	44
	2.5	40.2	19.1	7.5	3.3	44
	3.3	40.2	13	7.5	6.5	44
	5	40.2	7.68	7.5	6.5	44
	V_{OUT2} (V)	**R3 (kΩ)**	**R4 (kΩ)**	**Rt (kΩ)**	**L_{OUT} (µH)**	**C_{OUT} (µF)**
Ch2	1.0	21	84.5	150	1.5	22
	1.2	21	42.2	100	1.5	22
	1.5	21	24	100	3.3	22
	1.8	40.2	32.4	100	3.3	22
	2.5	40.2	19.1	7.5	3.3	22
	3.3	40.2	13	7.5	6.5	22
	5	40.2	7.68	7.5	6.5	22

NOTE:

7) Rt must larger than 7kΩ.

Selecting the Inductor

For most applications, use a 1 - 10µH inductor with a DC current rating at least 25% higher than the maximum load current. For the highest efficiency, use an inductor with a DC resistance less than 15mΩ. For most designs, the inductance value can be derived from Equation (2):

$$L_1=\frac{V_{OUT}\times(V_{IN}-V_{OUT})}{V_{IN}\times\Delta I_L\times f_s} \qquad (2)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (3):

$$I_{L(MAX)}=I_{LOAD}+\frac{\Delta I_L}{2} \qquad (3)$$

Use a larger inductor for improved efficiency under light-load conditions (below 100mA).

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are recommended for their low ESR and small temperature coefficients. For most applications, a 22µF capacitor is sufficient.

Since C_{IN} absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (4):

$$I_{C_{IN}}=I_{LOAD}\times\sqrt{\frac{V_{OUT}}{V_{IN}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)} \qquad (4)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (5):

$$I_{C_{IN}}=\frac{I_{LOAD}}{2} \qquad (5)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, place a small, high-quality ceramic capacitor (e.g.: 0.1μF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at the input. For single channels, the input voltage ripple caused by the capacitance can be estimated with Equation (6):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_s \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \qquad (6)$$

Selecting the Output Capacitor

The output capacitor (C_{OUT}) maintains the DC output voltage. Ceramic, tantalum, or low-ESR electrolytic capacitors are recommended. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_s \times C_{OUT}}\right) \qquad (7)$$

Where L_1 is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and the capacitance causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_s^2 \times L_1 \times C_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \qquad (8)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \qquad (9)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MP2223 can be optimized for a wide range of capacitance and ESR values.

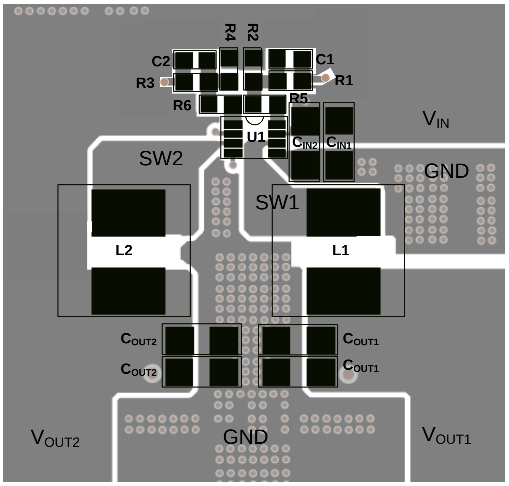
PCB Layout Guidelines [8]

Efficient PCB layout is critical for stable operation. For best results, refer to Figure 6 and follow the guidelines below.

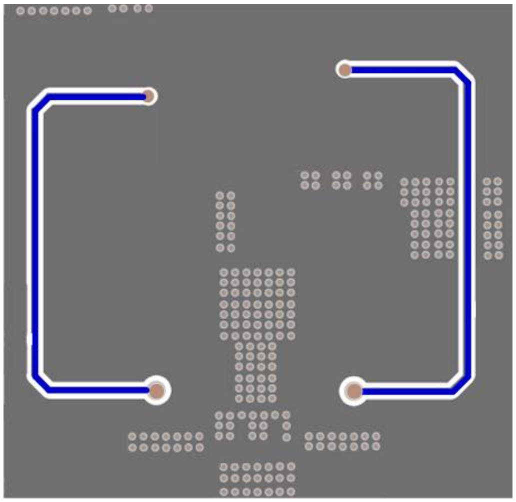
1. Connect the input ground to IN and GND using the shortest and widest trace possible.
2. Ensure that all feedback connections are short and direct.
3. Place the feedback resistors and compensation components as close to the chip as possible.
4. Route SW away from sensitive analog areas such as FB.

NOTES:

8) The recommended layout is based on the Typical Application circuit in Figure 7.



Top Layer



Bottom Layer

Figure 6: Recommended PCB Layout

Design Example

Table 2 shows a design example following the application guidelines for the specifications below.

Table 2: Design Example

V_{IN}	12V
V_{OUT1}	1.8V
I_{O1}	3A
V_{OUT2}	1.2V
I_{O2}	2A

The detailed application schematic is shown in Figure 7. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section. For more device applications, please refer to the related evaluation board datasheets.

TYPICAL APPLICATION CIRCUIT

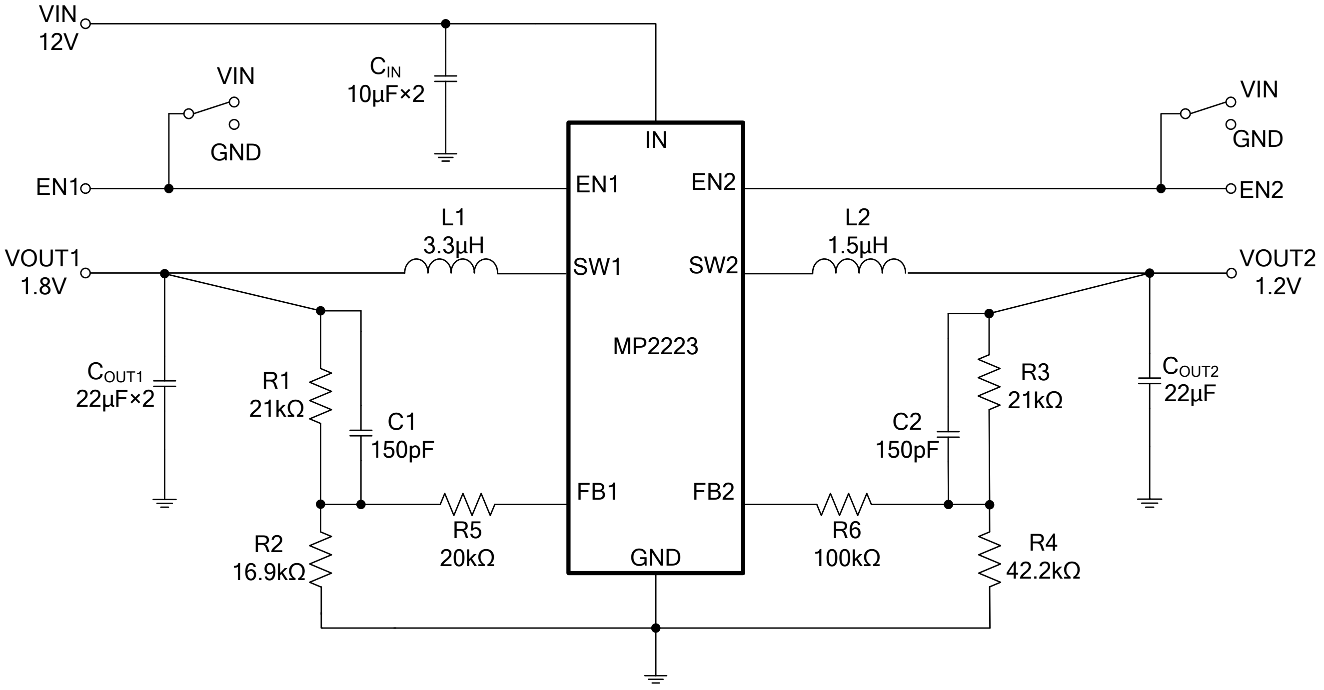
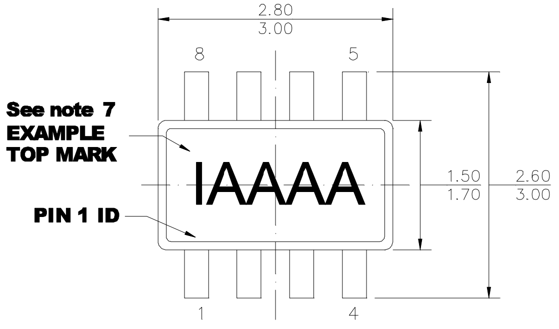


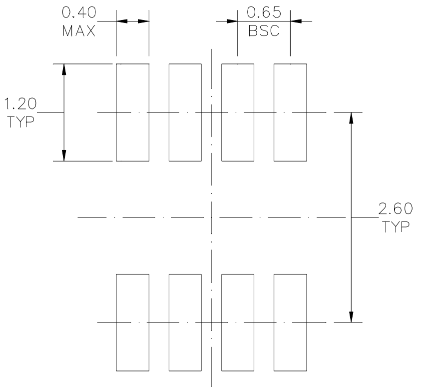
Figure 7: 12V V_{IN}, 1.8V/3A, 1.2V/2A

PACKAGE INFORMATION

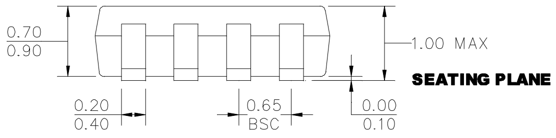
TSOT23-8



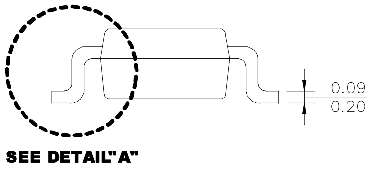
TOP VIEW



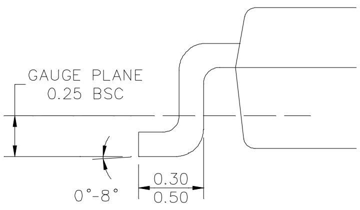
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION
4) LEAD COPLANARITY(BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO193, VARIATION BA
6) DRAWING IS NOT TO SCALE
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)