CAT93C46 (Die Rev. H)

1K-Bit Microwire Serial EEPROM

CAT93C46 Die Revision H not recommended for new designs. See CAT93HC46 data sheet.

FEATURES

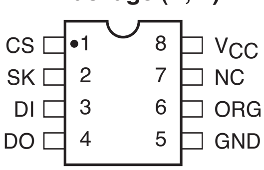
- High speed operation: 1MHz
- Low power CMOS technology
- 1.8 to 6.0 volt operation
- Selectable x8 or x16 memory organization
- Self-timed write cycle with auto-clear
- Hardware and software write protection
- Power-up inadvertant write protection
- 1,000,000 Program/erase cycles
- 100 year data retention
- Commercial, industrial and automotive temperature ranges
- “Green” package option available

DESCRIPTION

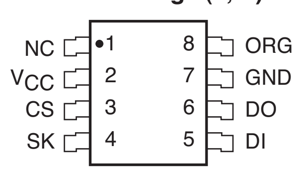
The CAT93C46 is a 1K-bit Serial EEPROM memory device which is configured as either registers of 16 bits (ORG pin at V_{CC}) or 8 bits (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The CAT93C46 is manufactured using Catalyst’s advanced CMOS EEPROM floating gate technology. The device is designed to endure 1,000,000 program/erase cycles and has a data retention of 100 years. The device is available in 8-pin DIP, 8-pin SOIC, 8-pin TSSOP and 8-pad TDFN packages.

PIN CONFIGURATION

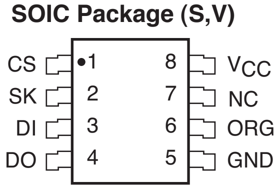
DIP Package (P, L)



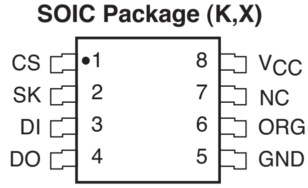
SOIC Package (J,W)



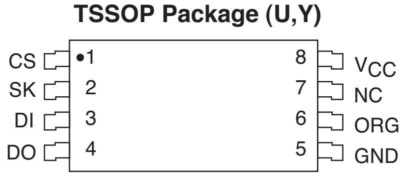
SOIC Package (S,V)



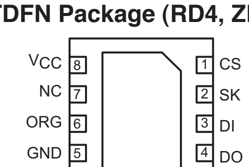
SOIC Package (K,X)



TSSOP Package (U,Y)

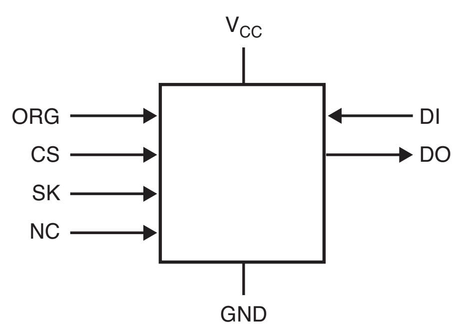


TDFN Package (RD4, ZD4)



Bottom View

FUNCTIONAL SYMBOL



PIN FUNCTIONS

Pin Name	Function
CS	Chip Select
SK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	+1.8 to 6.0V Power Supply
GND	Ground
ORG	Memory Organization
NC	No Connection

Note: When the ORG pin is connected to VCC, the x16 organization is selected. When it is connected to ground, the x8 pin is selected. If the ORG pin is left unconnected, then an internal pullup device will select the x16 organization.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .... -55°C to +125°C

Storage Temperature .... -65°C to +150°C

Voltage on any Pin with
Respect to Ground(1) .... -2.0V to $+V_{CC}$ +2.0V

V_{CC} with Respect to Ground .... -2.0V to +7.0V

Package Power Dissipation
Capability (T_A = 25°C) 1.0W

Lead Soldering Temperature (10 secs) .... 300°C

Output Short Circuit Current(2) .... 100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Reference Test Method	Min	Typ	Max	Units
N_{END}(3)	Endurance	MIL-STD-883, Test Method 1033	1,000,000			Cycles/Byte
T_{DR}(3)	Data Retention	MIL-STD-883, Test Method 1008	100			Years
V_{ZAP}(3)	ESD Susceptibility	MIL-STD-883, Test Method 3015	2000			Volts
I_{LTH}(3)(4)	Latch-Up	JEDEC Standard 17	100			mA

D.C. OPERATING CHARACTERISTICS

V_{CC} = +1.8V to +6.0V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I_{CC1}	Power Supply Current (Write)	f_{SK} = 1MHz V_{CC} = 5.0V			3	mA
I_{CC2}	Power Supply Current (Read)	f_{SK} = 1MHz V_{CC} = 5.0V			500	μA
I_{SB1}	Power Supply Current (Standby) (x8 Mode)	CS = 0V ORG=GND			10	μA
I_{SB2}	Power Supply Current (Standby) (x16Mode)	CS=0V ORG=Float or V_{CC}		0	10	μA
I_{LI}	Input Leakage Current	V_{IN} = 0V to V_{CC}			1	μA
I_{LO}	Output Leakage Current (Including ORG pin)	V_{OUT} = 0V to V_{CC}, CS = 0V			1	μA
V_{IL1}	Input Low Voltage	$4.5V \le V_{CC} < 5.5V$	-0.1		0.8	V
V_{IH1}	Input High Voltage	$4.5V \le V_{CC} < 5.5V$	2		V_{CC} + 1	V
V_{IL2}	Input Low Voltage	$1.8V \le V_{CC} < 4.5V$	0		V_{CC} x 0.2	V
V_{IH2}	Input High Voltage	$1.8V \le V_{CC} < 4.5V$	V_{CC} x 0.7		V_{CC}+1	V
V_{OL1}	Output Low Voltage	$4.5V \le V_{CC} < 5.5V$ I_{OL} = 2.1mA			0.4	V
V_{OH1}	Output High Voltage	$4.5V \le V_{CC} < 5.5V$ I_{OH} = -400μA	2.4			V
V_{OL2}	Output Low Voltage	$1.8V \le V_{CC} < 4.5V$ I_{OL} = 1mA			0.2	V
V_{OH2}	Output High Voltage	$1.8V \le V_{CC} < 4.5V$ I_{OH} = -100μA	V_{CC} - 0.2			V

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.

PIN CAPACITANCE

Symbol	Test	Conditions	Min	Typ	Max	Units
C_{OUT}(1)	Output Capacitance (DO)	V_{OUT}=0V			5	pF
C_{IN}(1)	Input Capacitance (CS, SK, DI, ORG)	V_{IN}=0V			5	pF

INSTRUCTION SET

Instruction	Start Bit	Opcode	Address		Data		Comments
			x8	x16	x8	x16	
READ	1	10	A6-A0	A5-A0			Read Address AN– A0
ERASE	1	11	A6-A0	A5-A0			Clear Address AN– A0
WRITE	1	01	A6-A0	A5-A0	D7-D0	D15-D0	Write Address AN– A0
EWEN	1	00	11XXXXX	11XXXX			Write Enable
EWDS	1	00	00XXXXX	00XXXX			Write Disable
ERAL	1	00	10XXXXX	10XXXX			Clear All Addresses
WRAL	1	00	01XXXXX	01XXXX	D7-D0	D15-D0	Write All Addresses

A.C. CHARACTERISTICS

Symbol	Parameter	Test Conditions	Limits						Units
			V_{CC} = 1.8V-6V		V_{CC} = 2.5V-6V		V_{CC} = 4.5V-5.5V		
			Min	Max	Min	Max	Min	Max	
t_{CSS}	CS Setup Time	C_L = 100pF (3)	200		100		50		ns
t_{CSH}	CS Hold Time		0		0		0		ns
t_{DIS}	DI Setup Time		400		200		100		ns
t_{DIH}	DI Hold Time		400		200		100		ns
t_{PD1}	Output Delay to 1			1		0.5		0.25	µs
t_{PD0}	Output Delay to 0			1		0.5		0.25	µs
t_{HZ}(1)	Output Delay to High-Z			400		200		100	ns
t_{EW}	Program/Erase Pulse Width			10		10		10	ms
t_{CSMIN}	Minimum CS Low Time		1		0.5		0.25		µs
t_{SKHI}	Minimum SK High Time		1		0.5		0.25		µs
t_{SKLOW}	Minimum SK Low Time		1		0.5		0.25		µs
t_{SV}	Output Delay to Status Valid			1		0.5		0.25	µs
SK_{MAX}	Maximum Clock Frequency		DC	250	DC	500	DC	1000	kHz

POWER-UP TIMING (1)(2)

Symbol	Parameter	Max	Units
t_{PUR}	Power-up to Read Operation	1	ms
t_{PUW}	Power-up to Write Operation	1	ms

A.C. TEST CONDITIONS

Input Rise and Fall Times	≤ 50ns	
Input Pulse Voltages	0.4V to 2.4V	$4.5V \leq V_{CC} \leq 5.5V$
Timing Reference Voltages	0.8V, 2.0V	$4.5V \leq V_{CC} \leq 5.5V$
Input Pulse Voltages	$0.2V_{CC}$ to $0.7V_{CC}$	$1.8V \leq V_{CC} \leq 4.5V$
Timing Reference Voltages	$0.5V_{CC}$	$1.8V \leq V_{CC} \leq 4.5V$

NOTE:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.
(3) The input levels and timing reference points are shown in “AC Test Conditions” table.

DEVICE OPERATION

The CAT93C46 is a 1024-bit nonvolatile memory intended for use with industry standard microprocessors. The CAT93C46 can be organized as either registers of 16 bits or 8 bits. When organized as X16, seven 9-bit instructions control the reading, writing and erase operations of the device. When organized as X8, seven 10-bit instructions control the reading, writing and erase operations of the device. The CAT93C46 operates on a single power supply and will generate on chip, the high voltage required during any write operation.

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a write operation.

The ready/busy status can be determined after the start of a write operation by selecting the device (CS high) and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy “1” into the DI pin. The DO pin will enter the high impedance state on the falling edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin.

The format for all instructions sent to the device is a logical "1" start bit, a 2-bit (or 4-bit) opcode, 6-bit address (an additional bit when organized X8) and for write operations a 16-bit data field (8-bit for X8 organizations).

Read

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT93C46 will come out of the high impedance state and, after sending an initial dummy zero bit, will begin shifting out the data addressed (MSB first). The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay (t_{PD0} or t_{PD1}).

Write

After receiving a WRITE command, address and the data, the CS (Chip Select) pin must be deselected for a minimum of t_{CSMIN}. The falling edge of CS will start the self clocking clear and data store cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46 can be determined by selecting the device and polling the DO pin. Since this device features Auto-Clear before write, it is NOT necessary to erase a memory location before it is written into.

Figure 1. Sychronous Data Timing

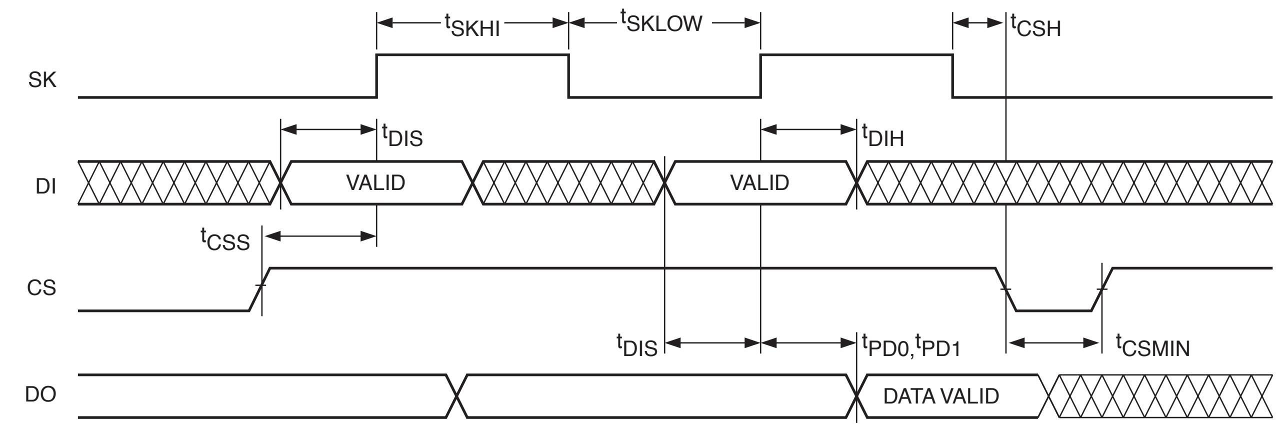


Figure 2. Read Instruction Timing

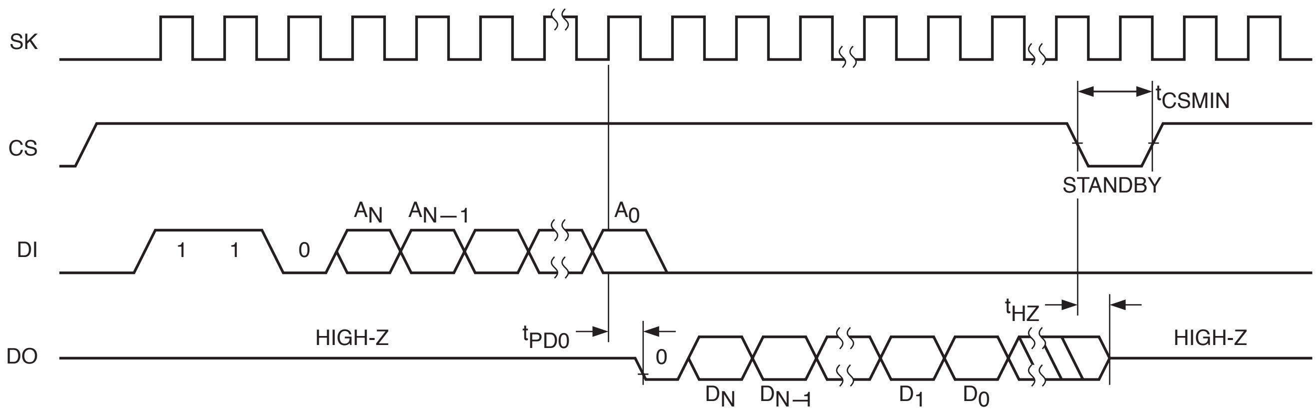
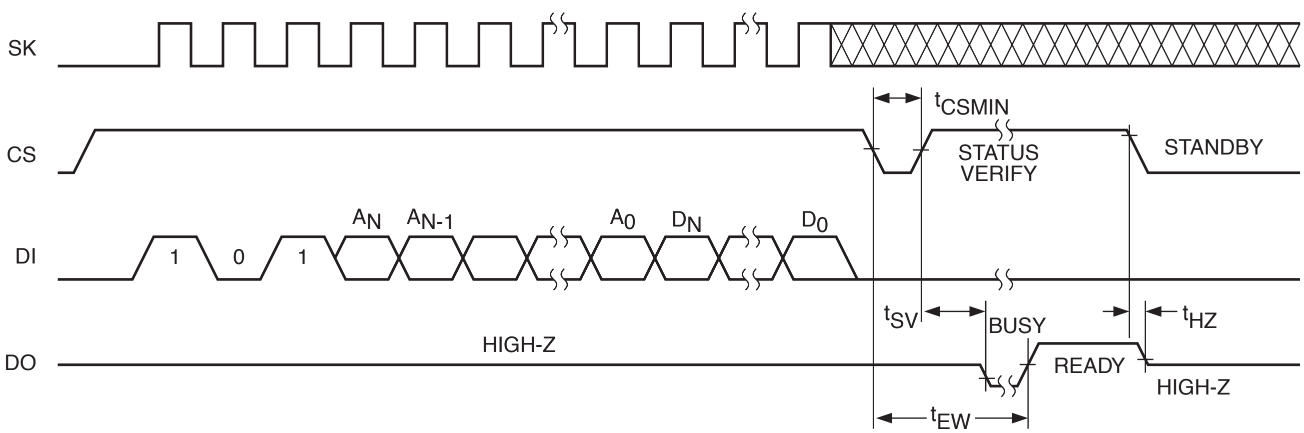


Figure 3. Write Instruction Timing



Erase

Upon receiving an ERASE command and address, the CS (Chip Select) pin must be deasserted for a minimum of t_{CSMIN}. The falling edge of CS will start the self clocking clear cycle of the selected memory location. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46 can be determined by selecting the device and polling the DO pin. Once cleared, the content of a cleared location returns to a logical "1" state.

Erase/Write Enable and Disable

The CAT93C46 powers up in the write disable state. Any writing after power-up or after an EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT93C46 write and clear instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status.

Erase All

Upon receiving an ERAL command, the CS (Chip Select) pin must be deselected for a minimum of t_{CSMIN}. The falling edge of CS will start the self clocking clear cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46 can be determined by selecting the device and polling the DO pin. Once cleared, the contents of all memory bits return to a logical "1" state.

Write All

Upon receiving a WRAL command and data, the CS (Chip Select) pin must be deselected for a minimum of t_{CSMIN}. The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. *(Note 1.)* The ready/ busy status of the CAT93C46 can be determined by selecting the device and polling the DO pin. It is not necessary for all memory locations to be cleared before the WRAL command is executed.

Note:
(1) With CAT93C46 Die revision H, after the last data bit has been sampled, Chip Select (CS) must be brought Low before the next rising edge of the clock(SK) in order to start the slef-timed high voltage cycle. This is important because if the CS is brought low before or after this specific frame window, the addressed location will not be programmed or erased.

Figure 4. Erase Instruction Timing

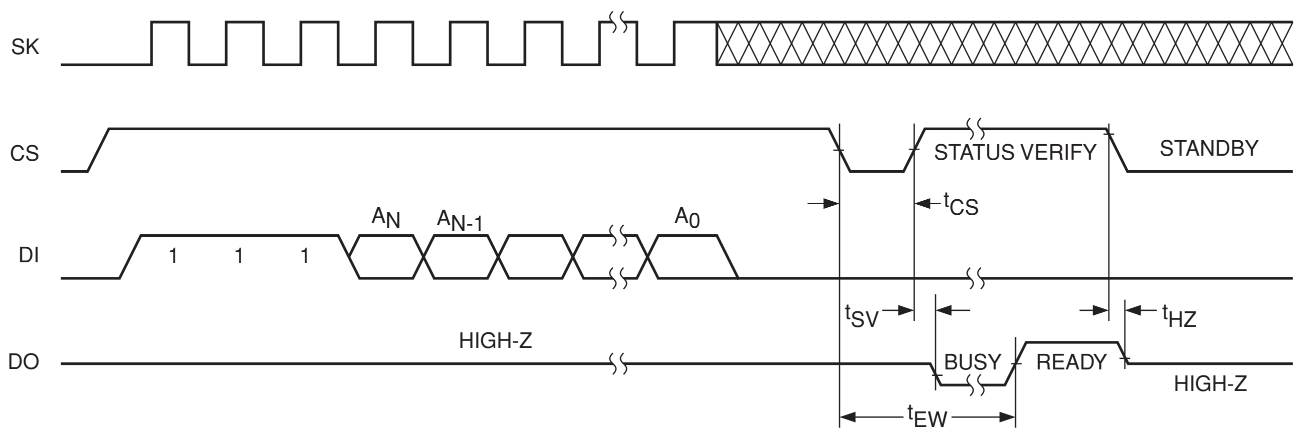


Figure 5. EWEN/EWDS Instruction Timing

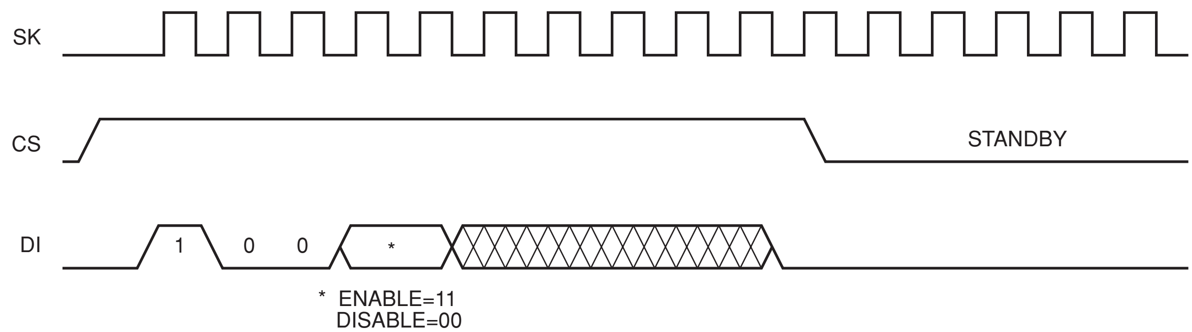


Figure 6. ERAL Instruction Timing

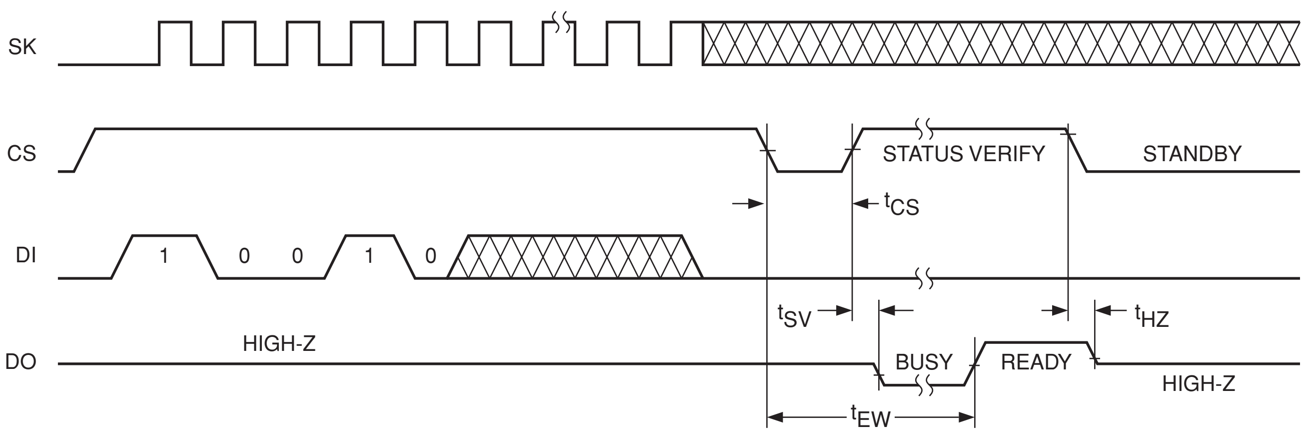
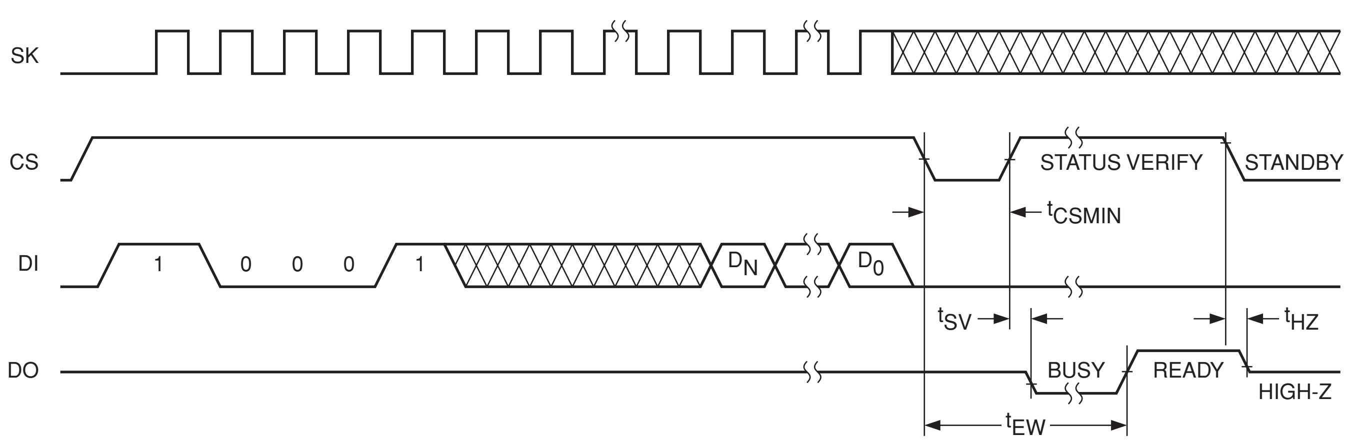


Figure 7. WRAL Instruction Timing



ORDERING INFORMATION

Prefix	Device #	Suffix				
CAT	93C46	S	I	-1.8	TE13	Rev H[2]
Optional Company ID	Product Number	Package	Temperature Range	Operating Voltage	Tape & Reel	Die Revision

Temperature Range
Blank = Commercial (0°C - 70°C)
I = Industrial (-40°C - 85°C)
A = Automotive (-40°C - 105°C)
E = Extended (-40°C to + 125°C)

Package
P = PDIP
S = SOIC (JEDEC)
J = SOIC (JEDEC)
K = SOIC (EIAJ)
U = TSSOP
RD4 = TDFN (3x3mm)
ZD4 = TDFN (3x3mm, Lead free, Halogen free)
L = PDIP (Lead free, Halogen free)
V = SOIC, JEDEC (Lead free, Halogen free)
W= SOIC, JEDEC (Lead free, Halogen free)
X = SOIC, EIAJ (Lead free, Halogen free)
Y = TSSOP (Lead free, Halogen free)

Operating Voltage
Blank (V_{CC}=2.5 to 6.0V)
1.8 (V_{CC}=1.8 to 6.0V)

Notes:
(1) The device used in the above example is a 93C46SI-1.8TE13 (SOIC, Industrial Temperature, 1.8 Volt to 6 Volt Operating Voltage, Tape & Reel)
(2) Product die revision letter is marked on top of the package as a suffix to the production data code (e.g., AYWW**H**.) For additional information, please contact your Catalyst sales office.

REVISION HISTORY

Date	Revision	Comments
05/14/04	L	New Data Sheet Created From CAT93C46/56/57/66/86. Parts CAT93C56, CAT93C56, CAT93C57, CAT93C66, CAT93C76 and CAT93C86 have been separtated into single data sheets Add Die Revision ID Letter Update Features Update Description Update Pin Condition Add Functional Diagram Update Pin Function Update D.C. Operating Characteristics Update Pin Capacitance Update Instruction Set Update Device Operation Update Ordering Information Update Revision History Update Rev Number

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