MP4321

36V, 1A, Configurable-Frequency, Low-I_Q, Ultra-Compact, Synchronous Step-Down Converter with 42V Load Dump Tolerance

DESCRIPTION

The MP4321 is a configurable-frequency (350kHz to 2.5MHz), synchronous, step-down switching converter with integrated internal high-side and low-side power MOSFETs (HS-FET and LS-FET, respectively). The device provides up to 1A of highly efficient output current (I_{OUT}) with peak current control mode.

The wide 3.3V to 36V input voltage (V_{IN}) range and 42V load dump tolerance accommodates a variety of step-down applications in automotive input environments. The 1µA shutdown current (I_{SD}) allows the converter to be used in battery-powered applications.

High power conversion efficiency across the entire load range is achieved by scaling down the switching frequency (f_{SW}) under light-load conditions to reduce switching and gate driver losses.

An open drain power good (PG) signal indicates whether the output is within 94.5% to 105.5% of its nominal voltage.

Frequency foldback prevents inductor current (I_L) runaway during start-up. Thermal shutdown provides reliable, fault-tolerant operation.

A high duty cycle and low-dropout (LDO) mode are provided for automotive cold crank conditions.

The MP4321 is available in a QFN-12 (2mmx3mm) package with wettable flanks.

FEATURES

- Designed for Aftermarket Automotive Applications:
  - 42V Load Dump Tolerance
  - Supports 3.1V for Cold Crank Conditions
  - Up to 1A of Continuous Output Current
  - Wide 3.3V to 36V Operating Input Voltage (V_{IN}) Range
  - -40°C to +125°C Operating Junction Temperature (T_J) Range
- Increases Battery Life:
  - 1µA Shutdown Current (I_{SD})
  - 20µA Sleep Mode Quiescent Current
  - Advanced Asynchronous Modulation (AAM) Mode for Increased Efficiency under Light Load Conditions
- High Performance for Improved Thermals:
  - 70mΩ/50mΩ Integrated MOSFETs
  - 65ns Minimum On Time (t_{ON_MIN})
  - 50ns Minimum Off Time (t_{OFF_MIN})
- Optimized for EMC/EMI Reduction:
  - Frequency Spread Spectrum (FSS) Modulation
  - Symmetric VIN Pinout
  - CISPR25 Class 5 Compliant
  - 350kHz to 2.5MHz Configurable Switching Frequency (f_{SW})
  - MeshConnect™ Flip-Chip Package
- Additional Features:
  - Power Good (PG) Output
  - Over-Current Protection (OCP) with Hiccup Mode
  - Available in a QFN-12 (2mmx3mm) Package
  - Available in a Wettable Flank Package

APPLICATIONS

- USB Chargers
- Aftermarket Automotive Applications
- Battery-Powered Systems
- General Consumer Applications

TYPICAL APPLICATION

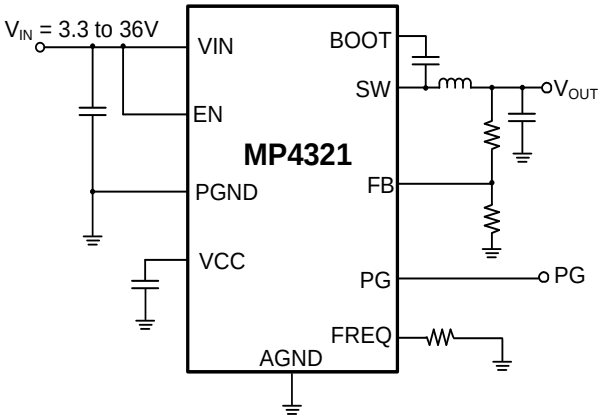
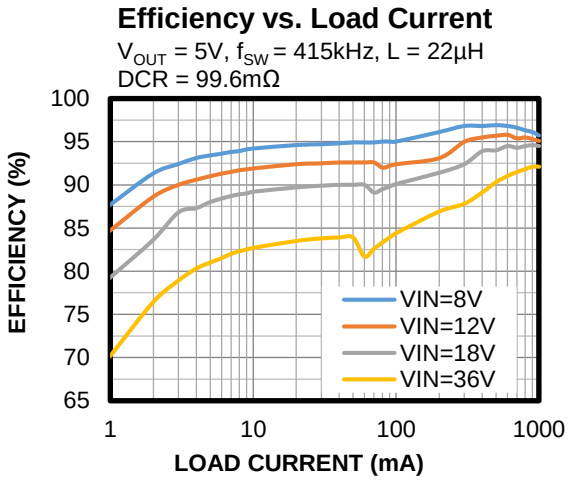


Figure 1: Typical Application (Adjustable Output)



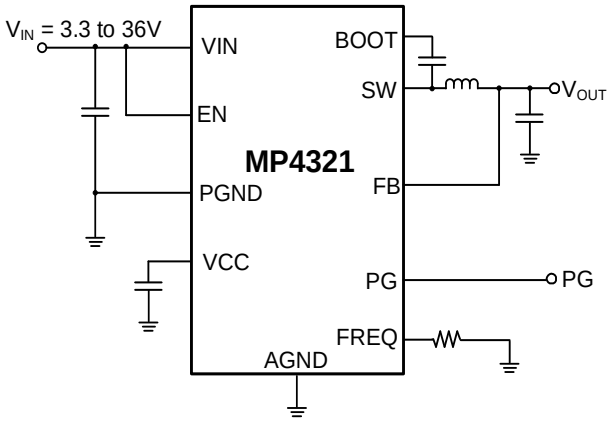


Figure 2: Typical Application (Fixed Output)

ORDERING INFORMATION

Part Number* (1)	Package	Top Marking	MSL Rating**
MP4321GDE***	QFN-12 (2mmx3mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MP4321GDE-Z).
**Moisture Sensitivity Level Rating
***Wettable Flank

Note:

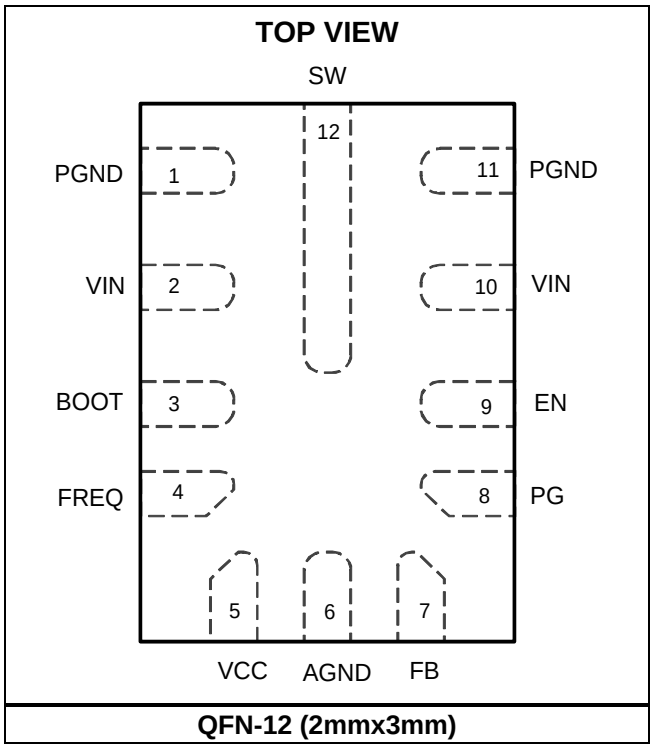
1) Contact MPS for details regarding the fixed output versions.

TOP MARKING (MP4321GDE)

BRJ
YWW
LLLL

BRJ: Production code of MP4321GDE
Y: Year code
WW: Week code
LLLL: Lot number

PACKAGE REFERENCE



QFN-12 (2mmx3mm)

PIN FUNCTIONS

Pin #	Name	Description
1, 11	PGND	**Power ground.**
2, 10	VIN	**Input supply.** The VIN pin supplies power to the internal control circuitry and the high-side MOSFET (HS-FET) connected to the SW pin. The two VIN pins are connected internally. Place a decoupling capacitor between each VIN pin and PGND. Place the capacitor as close to each VIN pin as possible to minimize switching spikes.
3	BOOT	**Bootstrap.** The BOOT pin is the positive power supply for the HS-FET driver connected to SW. Connect a bypass capacitor between the BOOT and SW pins.
4	FREQ	**Switching frequency.** Connect a resistor between the FREQ pin and AGND to set the switching frequency (f_{SW}).
5	VCC	**Bias supply.** The VCC pin is the output of the internal regulator that supplies power to the internal control circuitry and gate drivers. Place a >1μF decoupling capacitor between VCC and AGND. Place this capacitor close to VCC.
6	AGND	**Analog ground.**
7	FB	**Feedback input.** The FB pin is the negative input of the error amplifier (EA) (typically 0.8V). For the fixed output versions, connect FB to the output. For the adjustable output version, connect FB to the middle point of the external feedback divider between the output and the AGND pin to set the output voltage (V_{OUT}).
8	PG	**Power good output.** The PG pin is an open-drain output. If PG is used, connect PG to a power source via a pull-up resistor. If V_{OUT} is within 94.5% and 105.5% of the nominal voltage, then PG goes high. If V_{OUT} exceeds 107% or drops below 93% of the nominal voltage, then PG goes low. Float PG if not used.
9	EN	**Enable.** Pull EN above the 1.02V to turn the converter on; pull the EN pin below 0.85V to turn it off. EN does not require an internal pull-up or pull-down resistor. Do not float EN.
12	SW	**Switch node.** The SW pin is the source of the HS-FET and the drain of the low-side MOSFET (LS-FET).

ABSOLUTE MAXIMUM RATINGS (2)

V_{IN}, V_{EN} ……..42V for automotive load dump (3)
V_{IN}, V_{EN} …… -0.3V to +40V
V_{SW} …… -0.3V to $V_{IN(MAX)}$ + 0.3V
V_{BOOT} ……..V_{SW} + 5.5V
V_{FREQ}, V_{CC} ……..….5.5V
All other pins ..……-0.3V to +6V
Continuous power dissipation (T_A = 25°C) (4)
QFN-12 (2mmx3mm) …… 3.5W (9)
Operating junction temperature …… 150°C
Lead temperature ……260°C
Storage temperature …….. -65°C to +150°C

ESD Ratings

Human body model (HBM) ……..……..Class 2 (5)
Charged device model (CDM) .....Class C2b (6)

Recommended Operating Conditions

Input voltage (V_{IN}) ..……3.3V to 36V
Minimum start-up V_{IN} …..……3.9V
Minimum V_{IN} after start-up ……..…….....3.1V
Output voltage (V_{OUT}) …….....0.8V to 0.95 x V_{IN}
Operating junction temp (T_J)..-40°C to +125°C (7)

Thermal Resistance θ_{JA} θ_{JC}

QFN-12 (2mmx3mm)		
JESD51-7…..…….60…...7.3...	°C/W (8)	
EVQ4321-D-00A…….....35.5.....3.5...	°C/W (9)	

Notes:

2) The absolute maximum ratings are rated at room temperature, unless otherwise noted. Exceeding these ratings may damage the device.
3) Refer to ISO16750.
4) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the device may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
5) Per ANSI/ESDA/JEDEC JS-001.
6) Per ANSI/ESDA/JEDEC JS-002.
7) The device may be able to operate at junction temperatures above 125°C. Contact an MPS FAE for more details.
8) Measured on a JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application. The value of θ_{JC} shows the thermal resistance from junction-to-case bottom.
9) Measured on the EVQ4321-D-00A: 8.3cmx8.3cm, 2oz copper thickness, 4-layer PCB. The value of θ_{JC} shows the thermal resistance from junction-to-case top.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +125°C (10), typical values are at T_J= 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Supply						
V_{IN} under-voltage lockout (UVLO) rising threshold	$V_{IN\_UVLO\_RISING}$		3.4	3.65	3.9	V
V_{IN} UVLO falling threshold	$V_{IN\_UVLO\_FALLING}$		2.6	2.9	3.1	V
V_{IN} UVLO hysteresis	$V_{IN\_UVLO\_HYS}$			750		mV
Quiescent current	I_Q	V_{FB} = 0.85V, T_J = 25°C, no load		20	28	µA
		V_{FB} = 0.85V, T_J = -40°C to +125°C (11), no load			34	µA
Quiescent current (switching) (11)	$I_{Q\_SWITCHING}$	Switching, R_{FB1} = 1MΩ, R_{FB2} = 191kΩ, no load		25		µA
Shutdown current	I_{SD}	V_{EN} = 0V		1	10	µA
V_{IN} over-voltage protection (OVP) rising threshold	$V_{IN\_OVP\_RISING}$		35.5	37.5	40	V
V_{IN} OVP falling threshold	$V_{IN\_OVP\_FALLING}$		34.5	36.5	39	V
V_{IN} OVP hysteresis	$V_{IN\_OVP\_HYS}$			1		V
MOSFETs and Frequency						
Switching frequency	f_{SW}	R_{FREQ} = 86.6kΩ	332	415	498	kHz
		R_{FREQ} = 34.8kΩ	900	1000	1100	kHz
		R_{FREQ} = 15kΩ	1980	2200	2420	kHz
Frequency spread spectrum (FSS)				±10		%
FSS modulation frequency				15		kHz
Minimum on time (11)	t_{ON_MIN}			65	80	ns
Minimum off time (11)	t_{OFF_MIN}			50	70	ns
Maximum duty cycle	D_{MAX}		98	99.5		%
Switch leakage current	I_{SW_LKG}	V_{SW} = V_{BOOT} = 0V or V_{IN}, V_{EN} = 0V, T_J = 25°C)		0.01	1	µA
		V_{SW} = V_{BOOT} = 0V or V_{IN}, V_{EN} = 0V, T_J = -40°C to +125°C		0.01	5	µA
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)\_HS}$	V_{BOOT} - V_{SW} = 5V		70	130	mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)\_LS}$	V_{CC} = 5V		50	90	mΩ
Output and Regulation						
Feedback (FB) voltage	V_{FB}	T_J = 25°C, adjustable output version	0.794	0.8	0.806	V
		Adjustable output version, T_J = -40°C to +125°C	0.79	0.8	0.81	V
FB current	I_{FB}	Adjustable output version		0	100	nA
V_{OUT} discharge current	$I_{DISCHARGE}$	V_{EN} = 0V, V_{OUT} = 0.3V	2	4		mA

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +125°C (10), typical values are at T_J= 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Bootstrap (BOOT)						
BOOT to SW refresh rising threshold	V_{BOOT_RISING}			2.5	2.9	V
BOOT to SW refresh falling threshold	$V_{BOOT\_FALLING}$			2.3	2.7	V
BOOT to SW refresh hysteresis	V_{BOOT_HYS}			0.2		V
Enable (EN)						
EN rising threshold	V_{EN_RISING}		0.97	1.02	1.07	V
EN falling threshold	$V_{EN\_FALLING}$		0.8	0.85	0.9	V
EN threshold hysteresis	V_{EN_HYS}			170		mV
Soft Start (SS) and VCC						
Soft-start time	t_{SS}	EN high to SS complete	3	5	7	ms
VCC voltage	V_{CC}	I_{VCC} = 0A	4.7	5	5.3	V
VCC regulation		I_{VCC} = 30mA		1		%
VCC current Limit	I_{LIMIT_VCC}	V_{CC} = 4V	50	70		mA
Power Good (PG)						
PG rising threshold	V_{PG_RISING}	V_{FB} / V_{REF}, V_{OUT} rising	93	94.5	96	% of V_{REF}
		V_{FB} / V_{REF}, V_{OUT} falling	104	105.5	107	
PG falling threshold	$V_{PG\_FALLING}$	V_{FB} / V_{REF}, V_{OUT} falling	91.5	93	94.5	% of V_{REF}
		V_{FB} / V_{REF}, V_{OUT} rising	105.5	107	108.5	
PG threshold hysteresis	V_{PG_HYS}	V_{FB} / V_{REF}		1.5		% of V_{REF}
PG output voltage (V_{OUT}) low	V_{PG_LOW}	I_{SINK} = 1mA		0.1	0.3	V
PG rising deglitch time	t_{PG_RISING}			70		µs
PG falling deglitch time	$t_{PG\_FALLING}$			60		µs
Protections						
HS-FET peak current limit	I_{LIMIT_HS}	20% duty cycle	1.5	2	2.6	A
LS-FET valley current limit	I_{LIMIT_LS}		1	1.5	2	A
Zero-current detection (ZCD) current	I_{ZCD}		-0.05	0.05	+0.15	A
Thermal shutdown (11)	T_{SD}		160	175	185	°C
Thermal shutdown hysteresis (11)	T_{SD_HYS}			20		°C

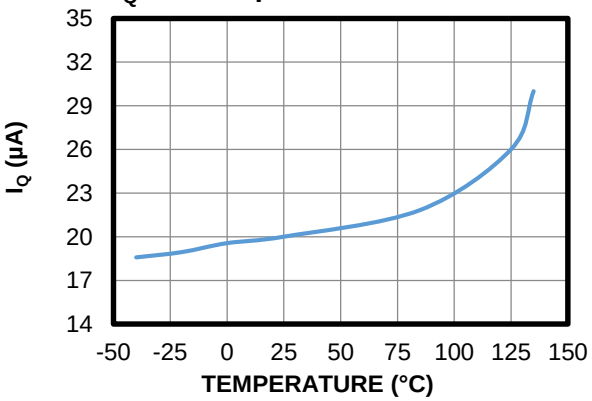
Notes:

10) Guaranteed by over temperature correlation. Not tested in production.
11) Guaranteed by design and characterization. Not tested in production.

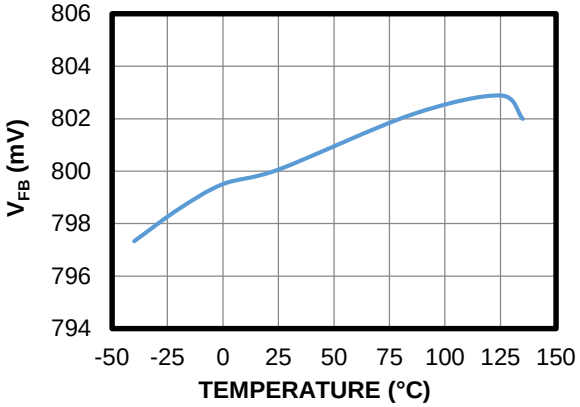
TYPICAL CHARACTERISTICS

V_{IN} = 12V, unless otherwise noted.

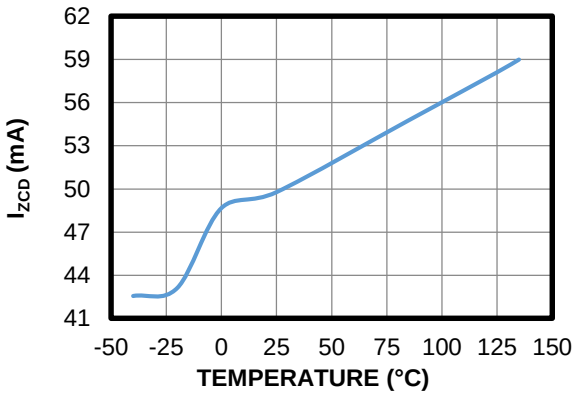
I_Q vs. Temperature



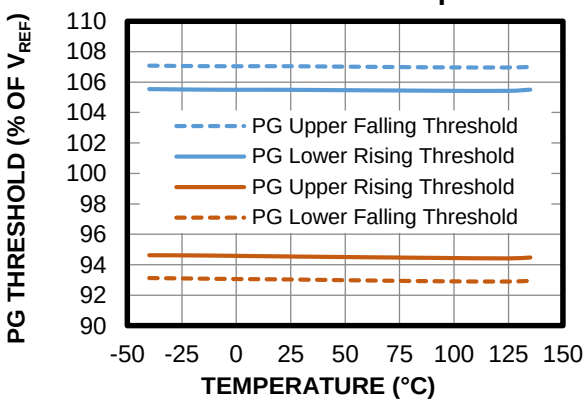
V_{FB} vs. Temperature



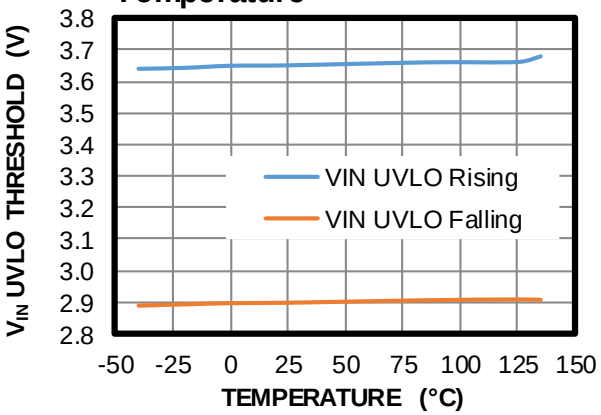
I_{ZCD} vs. Temperature



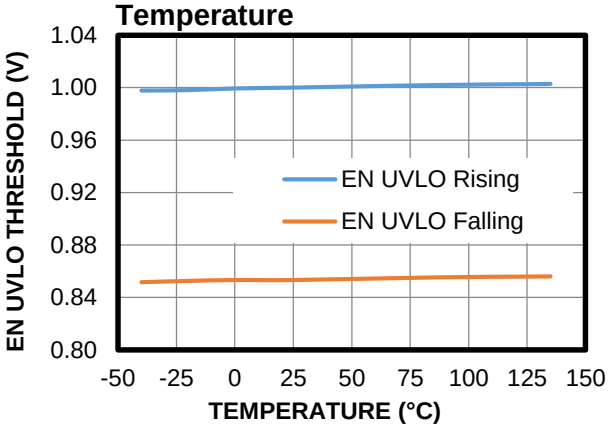
PG Threshold vs. Temperature



V_{IN} UVLO Threshold vs. Temperature



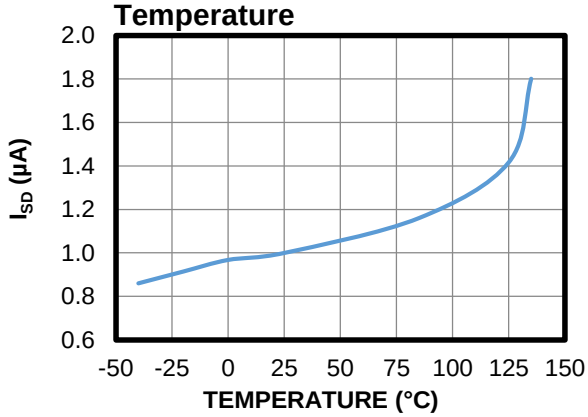
EN UVLO Threshold vs. Temperature



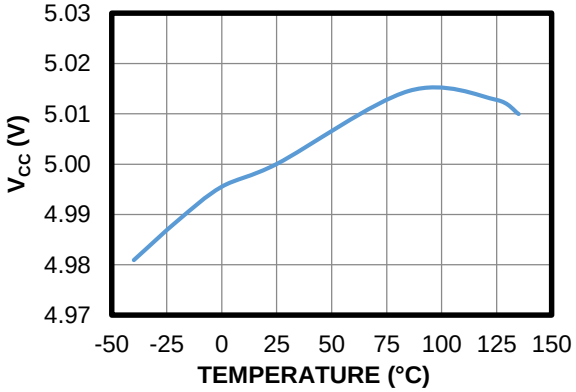
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, unless otherwise noted.

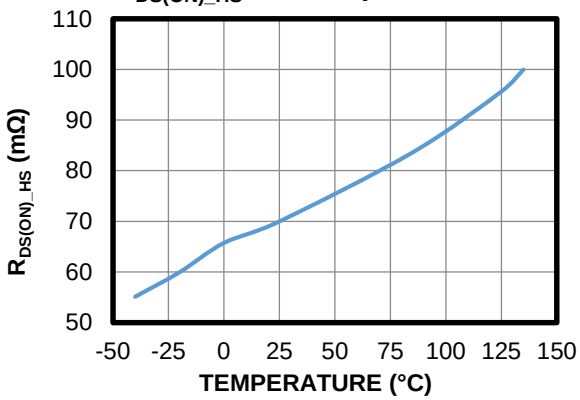
Shutdown Current vs. Temperature



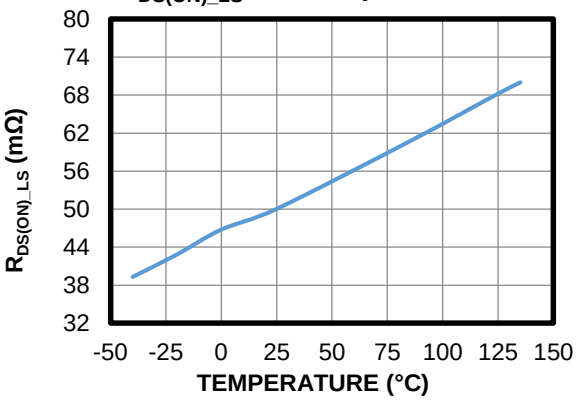
V_{CC} vs. Temperature



$R_{DS(ON)\_HS}$ vs. Temperature

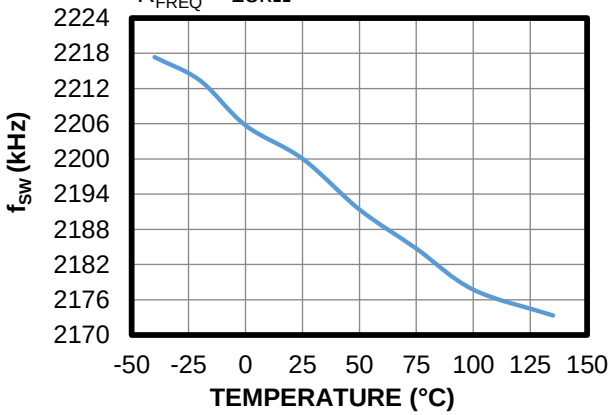


$R_{DS(ON)\_LS}$ vs. Temperature



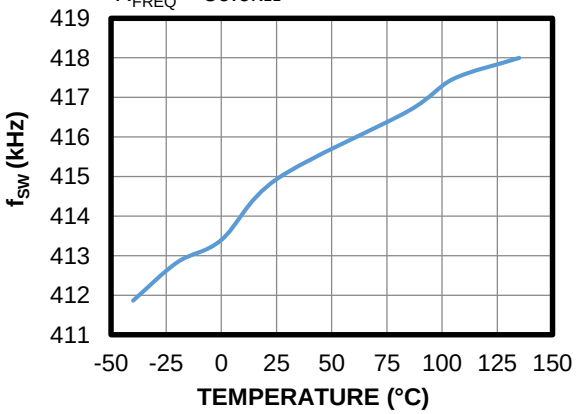
f_{SW} vs. Temperature

R_{FREQ} = 15kΩ



f_{SW} vs. Temperature

R_{FREQ} = 86.6kΩ

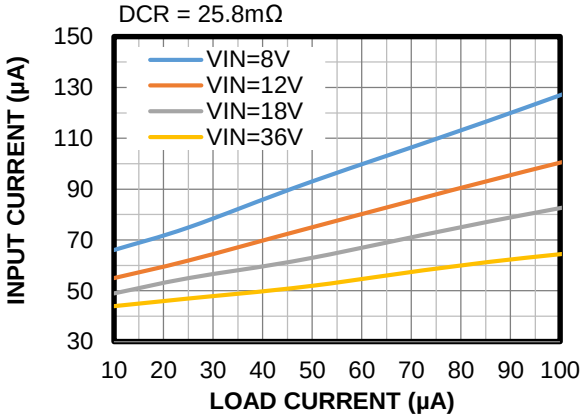


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 5.6µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

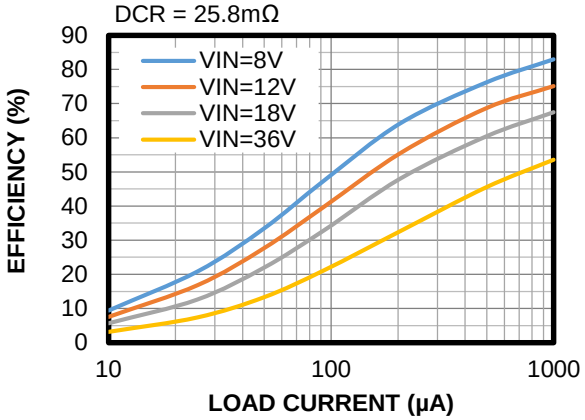
Input Current vs. Load Current

R_{FB1} = 100kΩ, R_{FB2} = 19.1kΩ,
DCR = 25.8mΩ



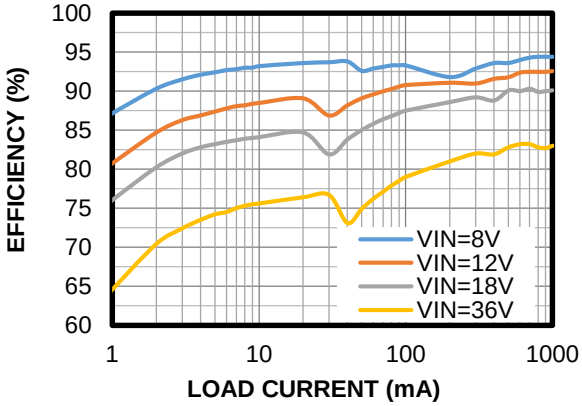
Efficiency vs. Load Current

R_{FB1} = 100kΩ, R_{FB2} = 19.1kΩ,
DCR = 25.8mΩ



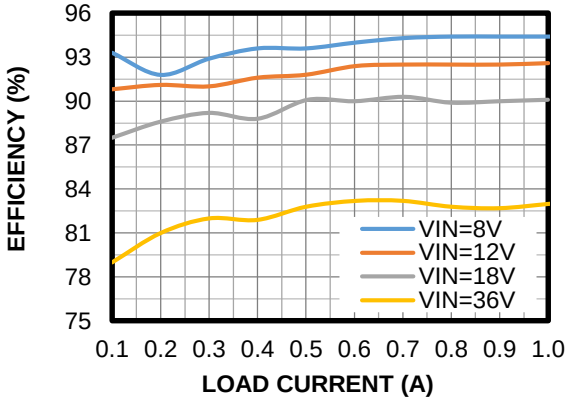
Efficiency vs. Load Current

DCR = 25.8mΩ



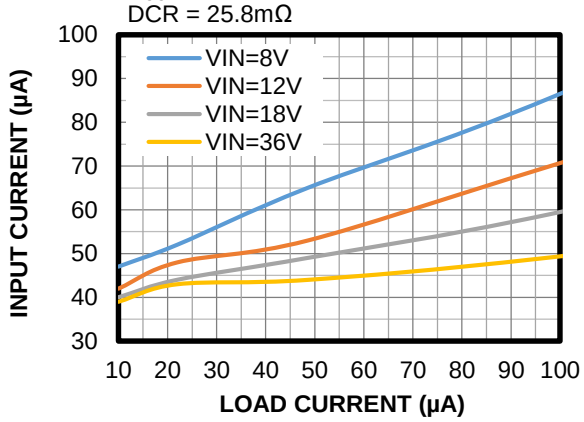
Efficiency vs. Load Current

DCR = 25.8mΩ



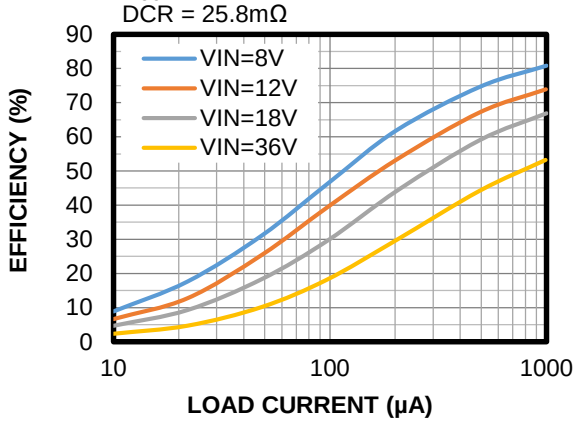
Input Current vs. Load Current

V_{OUT} = 3.3V, R_{FB1} = 100kΩ, R_{FB2} = 31.6kΩ
DCR = 25.8mΩ



Efficiency vs. Load Current

V_{OUT} = 3.3V, R_{FB1} = 100kΩ, R_{FB2} = 31.6kΩ
DCR = 25.8mΩ

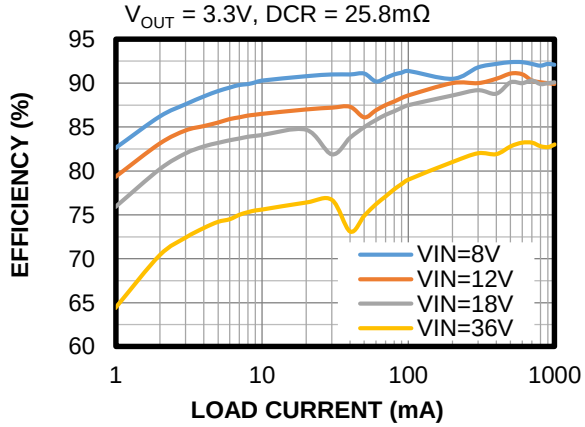


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 5.6µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

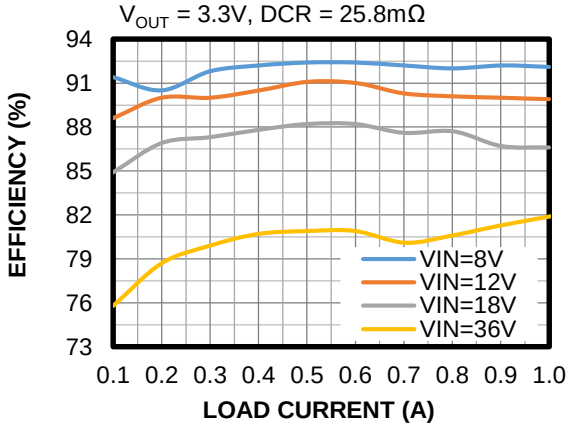
Efficiency vs. Load Current

V_{OUT} = 3.3V, DCR = 25.8mΩ



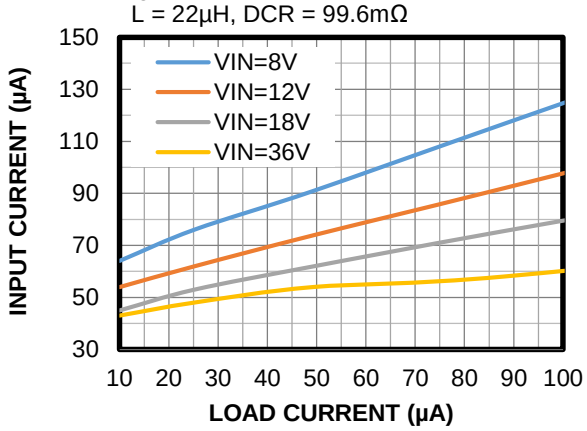
Efficiency vs. Load Current

V_{OUT} = 3.3V, DCR = 25.8mΩ



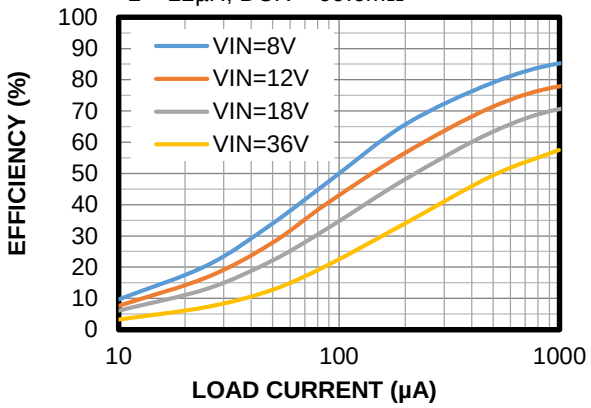
Input Current vs. Load Current

f_{SW} = 415kHz, R_{FB1} = 100kΩ, R_{FB2} = 19.1kΩ
L = 22µH, DCR = 99.6mΩ



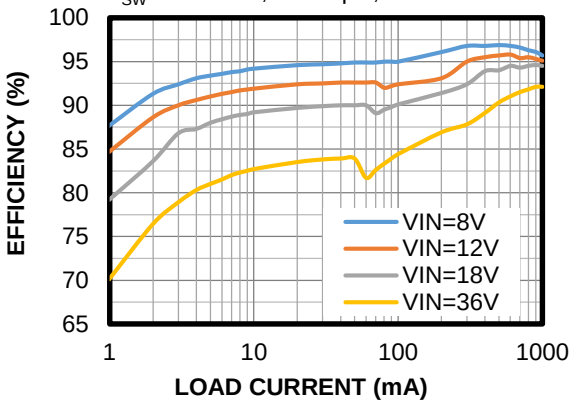
Efficiency vs. Load Current

f_{SW} = 415kHz, R_{FB1} = 100kΩ, R_{FB2} = 19.1kΩ
L = 22µH, DCR = 99.6mΩ



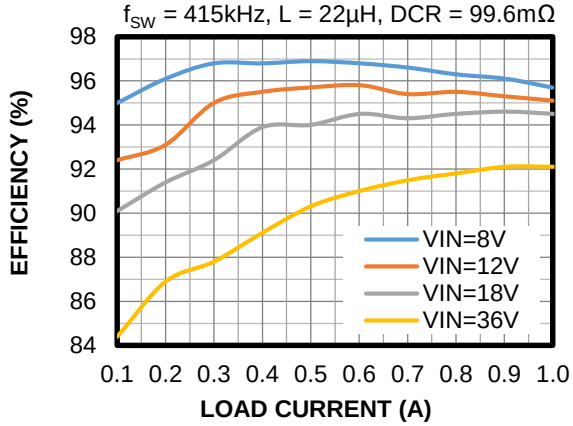
Efficiency vs. Load Current

f_{SW} = 415kHz, L = 22µH, DCR = 99.6mΩ



Efficiency vs. Load Current

f_{SW} = 415kHz, L = 22µH, DCR = 99.6mΩ

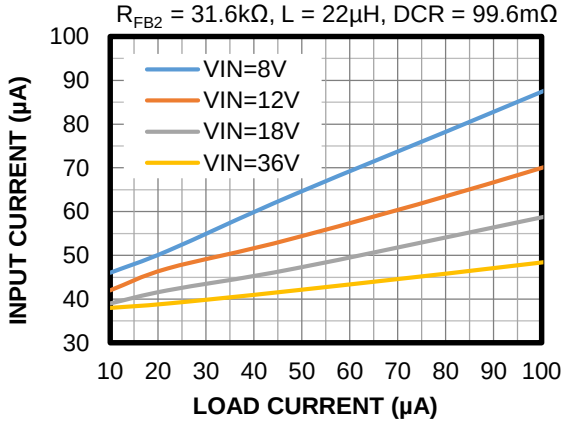


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 5.6µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

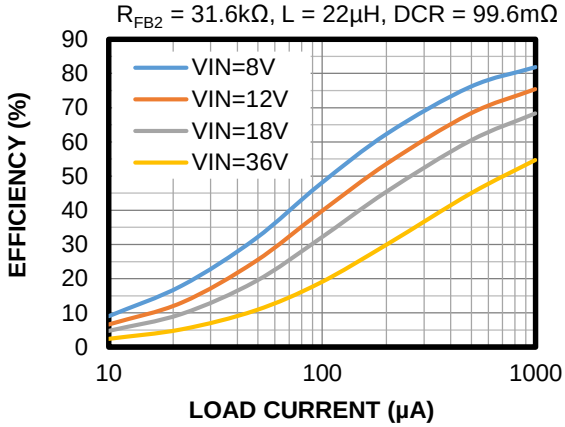
Input Current vs. Load Current

V_{OUT} = 3.3V, f_{SW} = 415kHz, R_{FB1} = 100kΩ
R_{FB2} = 31.6kΩ, L = 22µH, DCR = 99.6mΩ



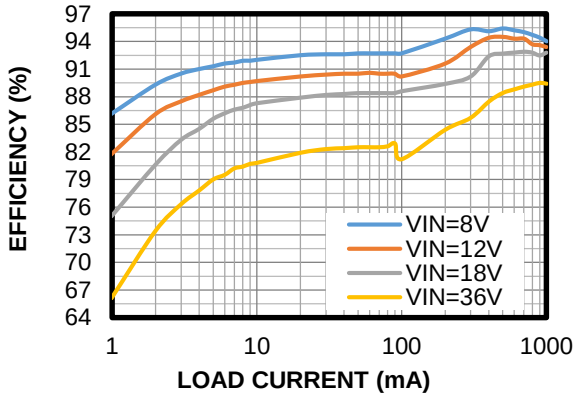
Efficiency vs. Load Current

V_{OUT} = 3.3V, f_{SW} = 415kHz, R_{FB1} = 100kΩ
R_{FB2} = 31.6kΩ, L = 22µH, DCR = 99.6mΩ



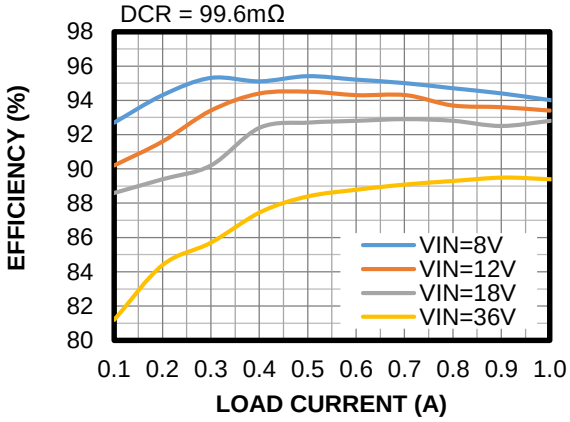
Efficiency vs. Load Current

V_{OUT} = 3.3V, f_{SW} = 415kHz, L = 22µH
DCR = 99.6mΩ



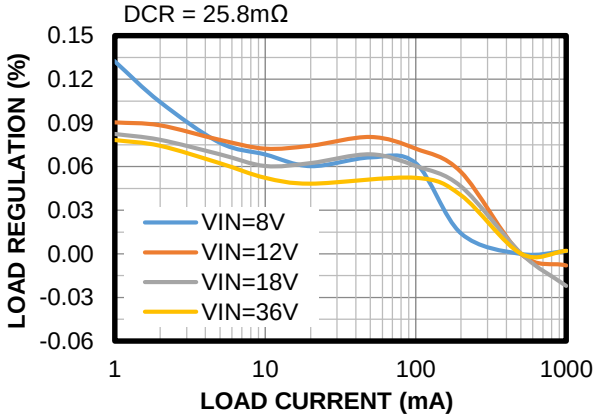
Efficiency vs. Load Current

V_{OUT} = 3.3V, f_{SW} = 415kHz, L = 22µH
DCR = 99.6mΩ



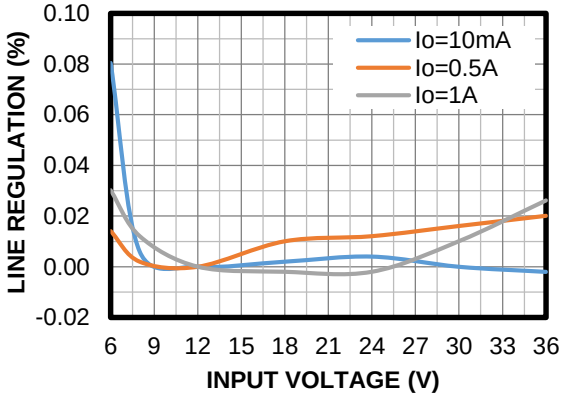
Load Regulation

DCR = 25.8mΩ



Line Regulation

DCR = 25.8mΩ

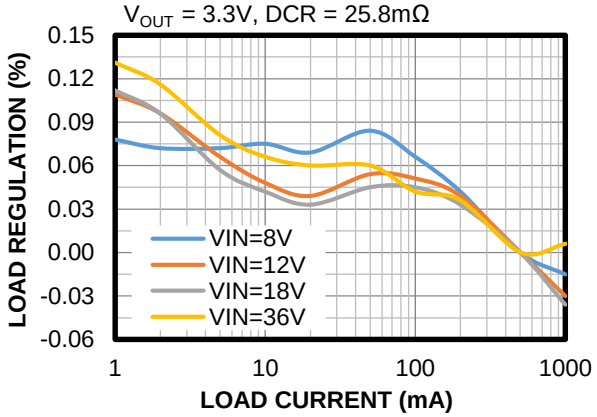


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 5.6µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

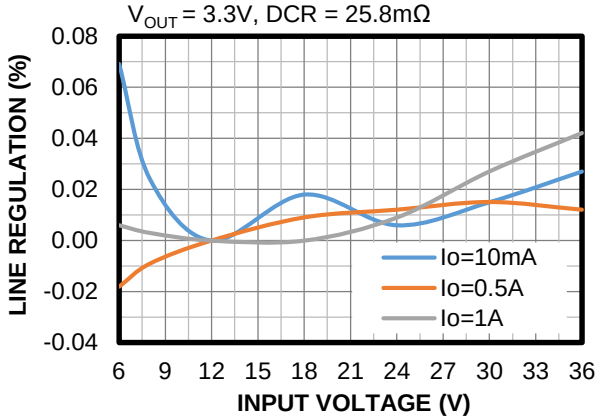
Load Regulation

V_{OUT} = 3.3V, DCR = 25.8mΩ



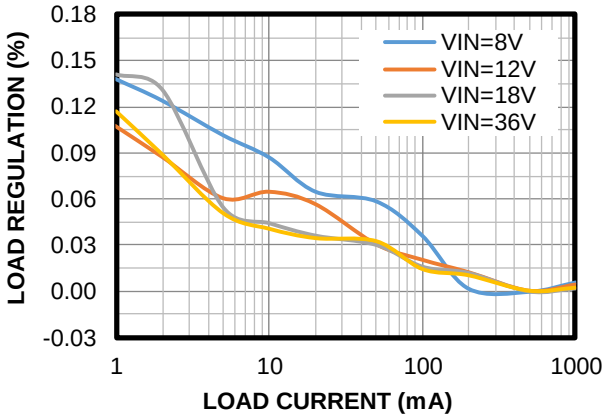
Line Regulation

V_{OUT} = 3.3V, DCR = 25.8mΩ



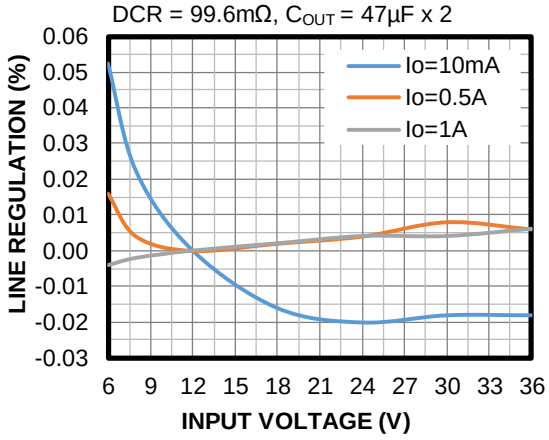
Load Regulation

f_{SW} = 415kHz, L = 22µH,
DCR = 99.6mΩ, C_{OUT} = 47µF x 2



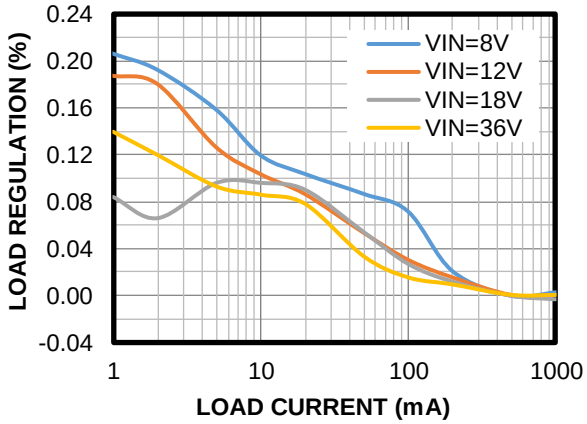
Line Regulation

f_{SW} = 415kHz, L = 22µH,
DCR = 99.6mΩ, C_{OUT} = 47µF x 2



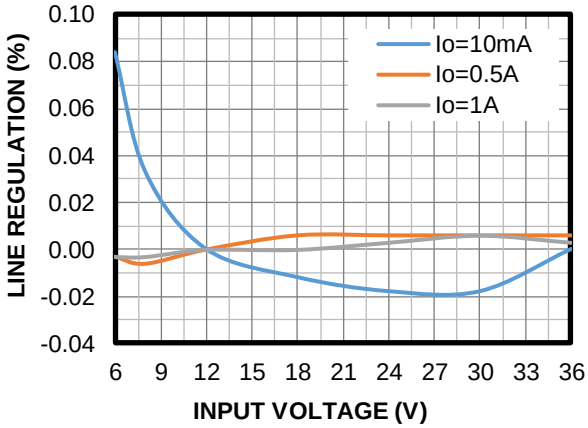
Load Regulation

V_{OUT} = 3.3V, f_{SW} = 415kHz, L = 22µH,
DCR = 99.6mΩ, C_{OUT} = 47µF x 2



Line Regulation

V_{OUT} = 3.3V, f_{SW} = 415kHz, L = 22µH,
DCR = 99.6mΩ, C_{OUT} = 47µF x 2

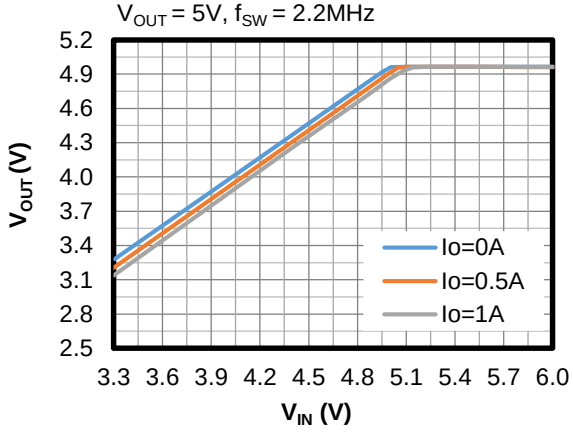


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 5.6µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

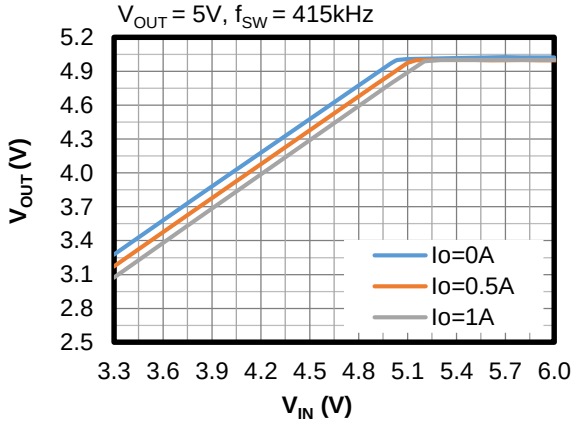
Low-Dropout Mode

V_{OUT} = 5V, f_{SW} = 2.2MHz



Low-Dropout Mode

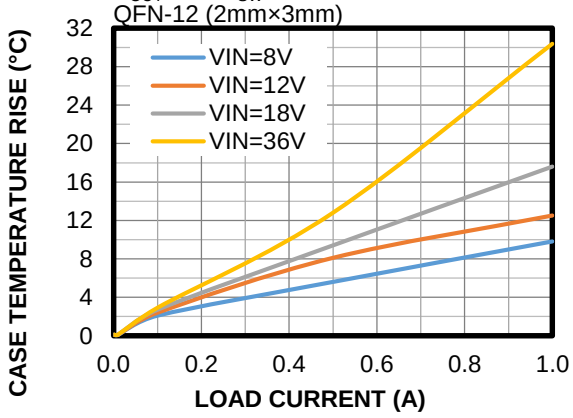
V_{OUT} = 5V, f_{SW} = 415kHz



Case Temperature Rise

V_{OUT} = 5V, f_{SW} = 2.2MHz

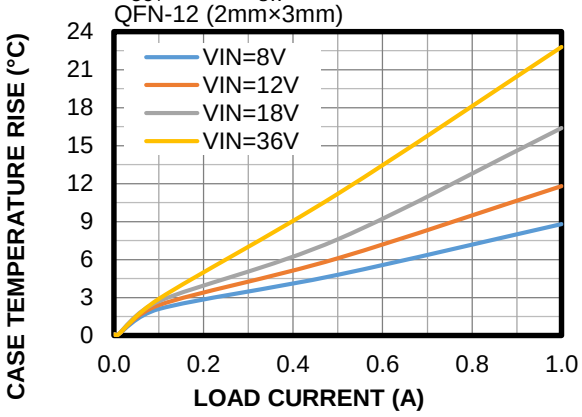
QFN-12 (2mm×3mm)



Case Temperature Rise

V_{OUT} = 3.3V, f_{SW} = 2.2MHz

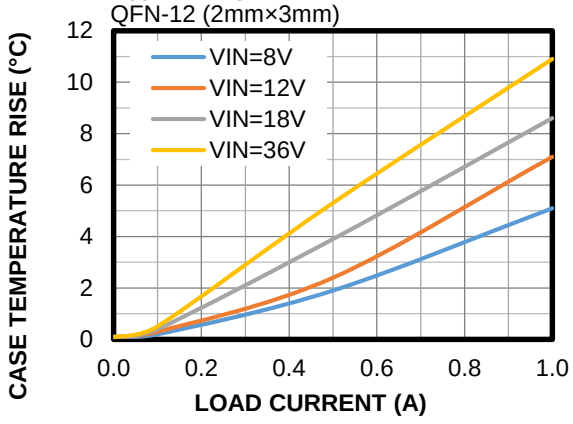
QFN-12 (2mm×3mm)



Case Temperature Rise

V_{OUT} = 5V, f_{SW} = 415kHz

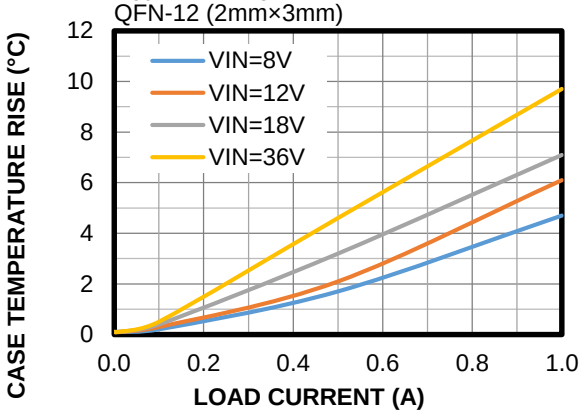
QFN-12 (2mm×3mm)



Case Temperature Rise

V_{OUT} = 3.3V, f_{SW} = 415kHz

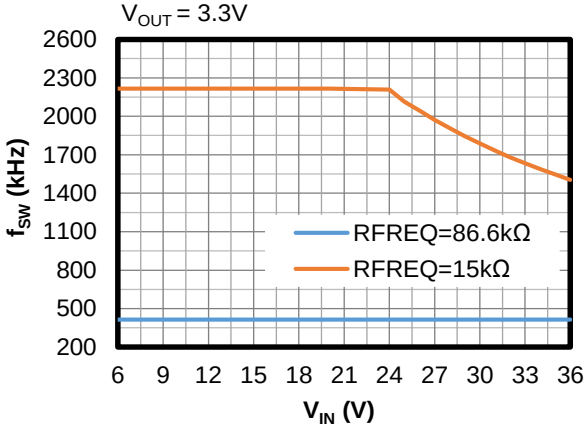
QFN-12 (2mm×3mm)



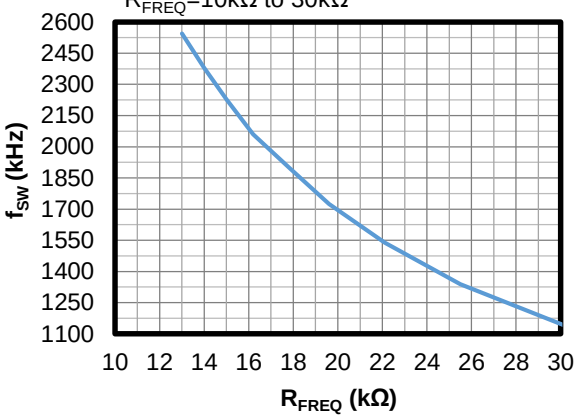
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 5.6µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

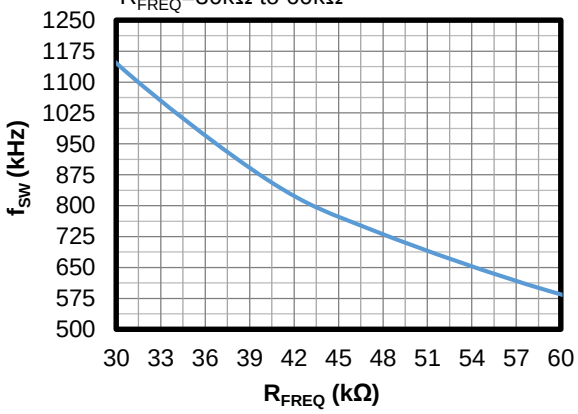
f_{SW} vs. V_{IN}
V_{OUT} = 3.3V



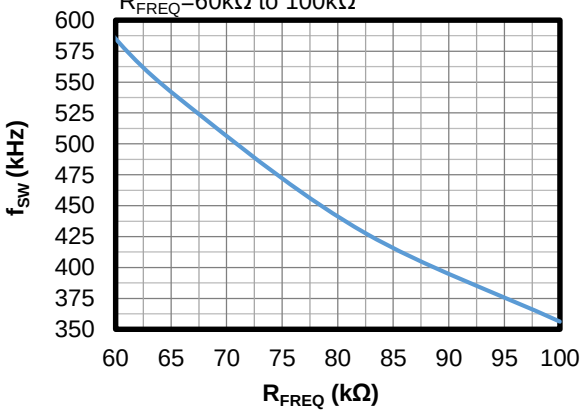
f_{SW} vs. R_{FREQ}
R_{FREQ}=10kΩ to 30kΩ



f_{SW} vs. R_{FREQ}
R_{FREQ}=30kΩ to 60kΩ



f_{SW} vs. R_{FREQ}
R_{FREQ}=60kΩ to 100kΩ

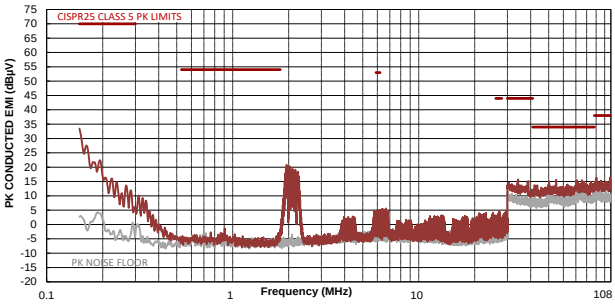


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)* (12)

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 5.6µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

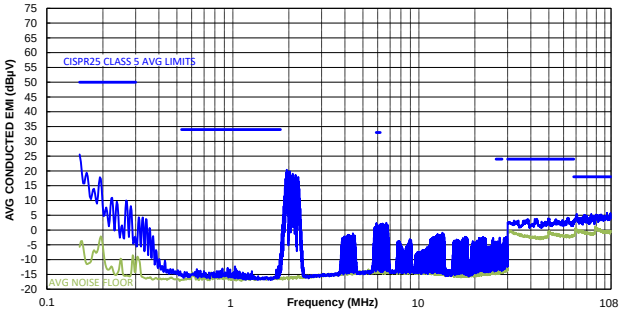
CISPR25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



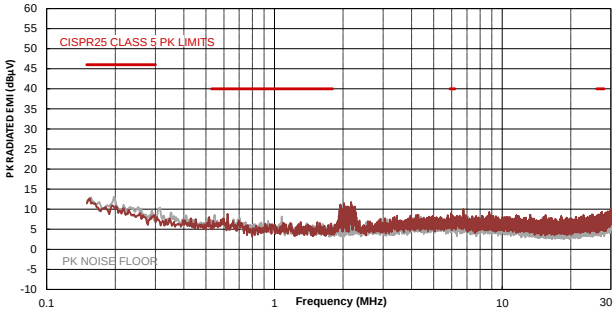
CISPR25 Class 5 Average Conducted Emissions

150kHz to 108MHz



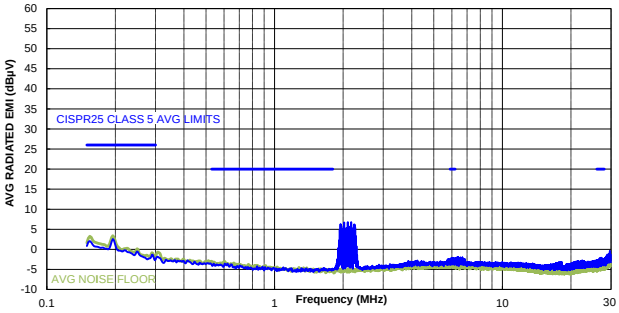
CISPR25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



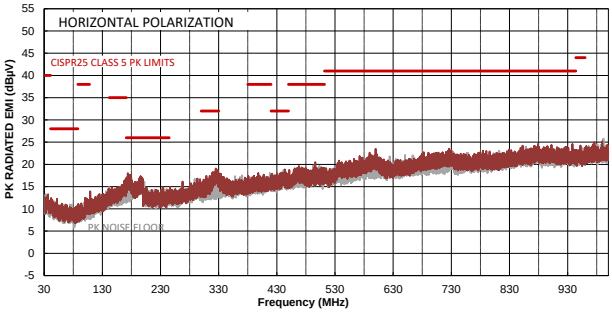
CISPR25 Class 5 Average Radiated Emissions

150kHz to 30MHz



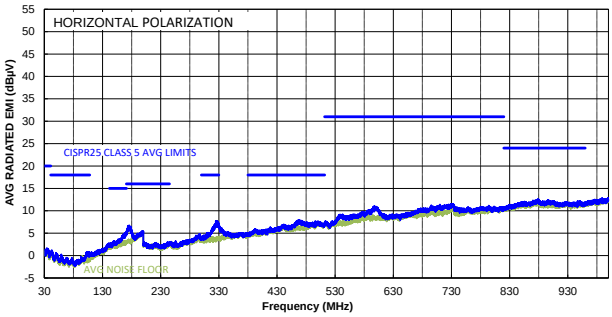
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 1GHz

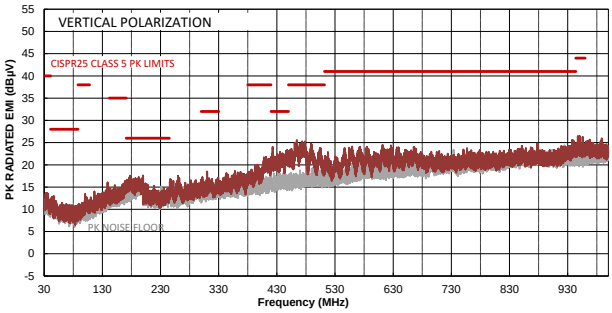


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)* (12)

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 5.6µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

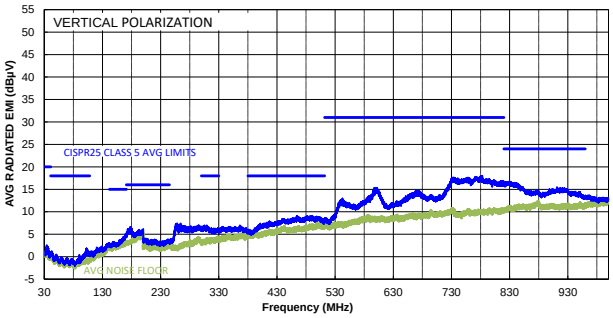
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 1GHz



Note:

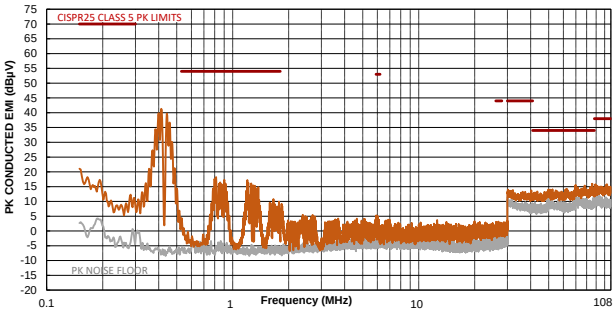
12) The EMC test results are based on the typical application circuit with EMI filters (see Figure 16 on page 38).

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)* (13)

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 415kHz, L = 22µH, C_{OUT} = 47µF x 2, T_A = 25°C, unless otherwise noted.

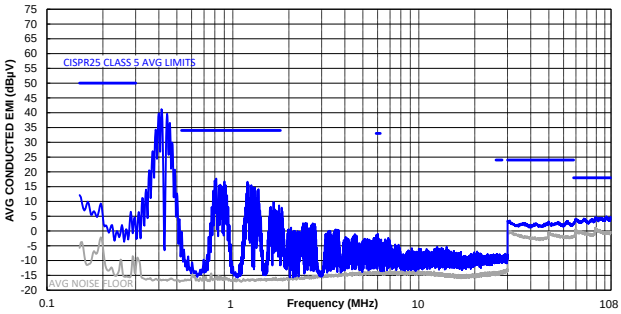
CISPR25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



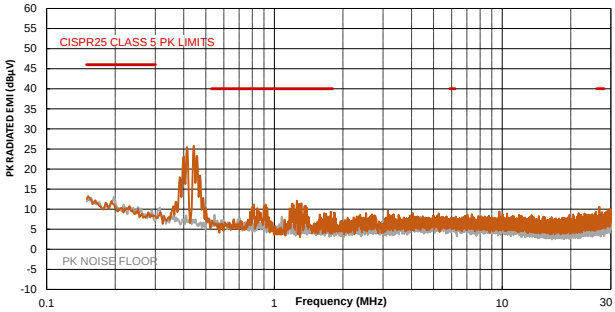
CISPR25 Class 5 Average Conducted Emissions

150kHz to 108MHz



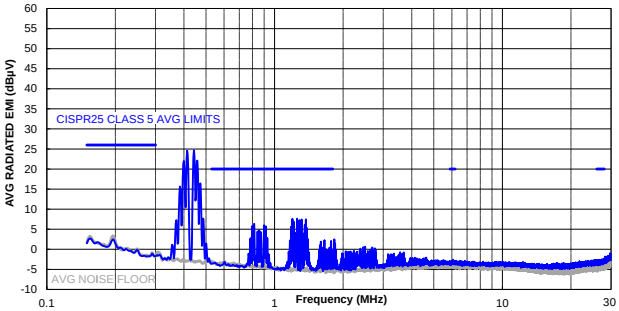
CISPR25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



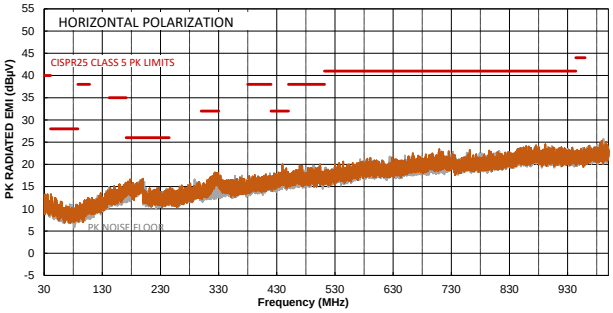
CISPR25 Class 5 Average Radiated Emissions

150kHz to 30MHz



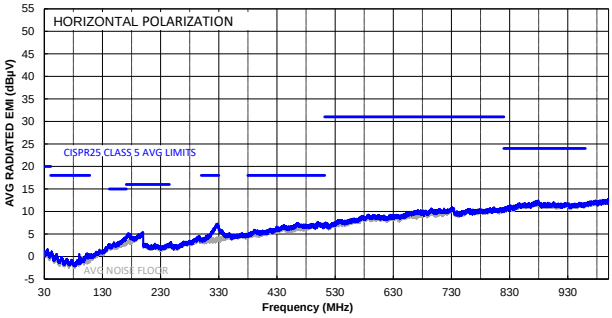
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 1GHz

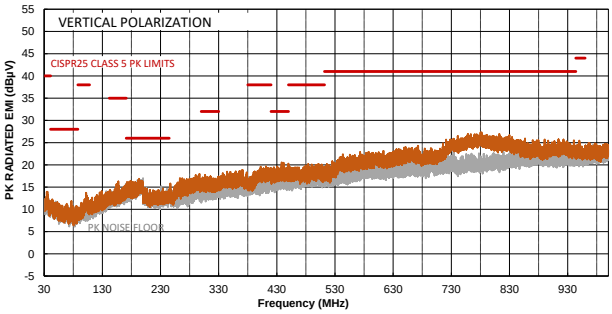


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)* (13)

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 415kHz, L = 22µH, C_{OUT} = 47µF x 2, T_A = 25°C, unless otherwise noted.

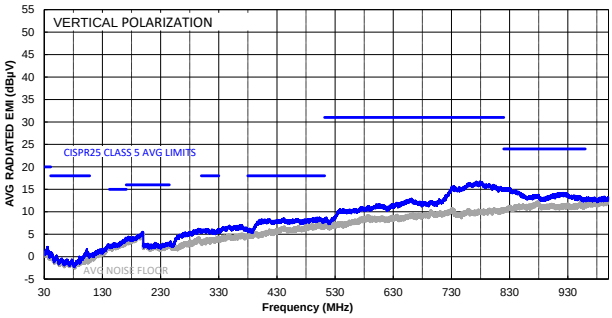
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 1GHz



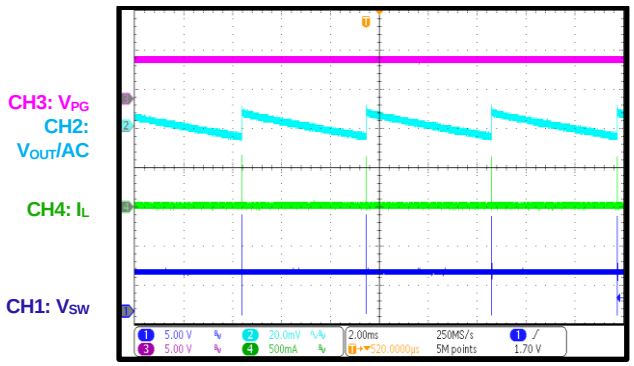
Note:

13) The EMC test results are based on the typical application circuit with EMI filters (see Figure 17 on page 39).

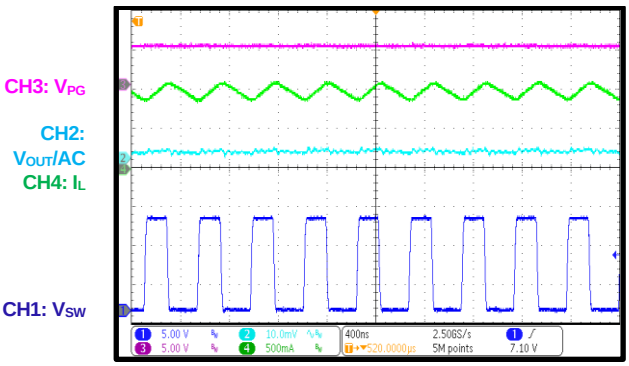
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 5.6µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

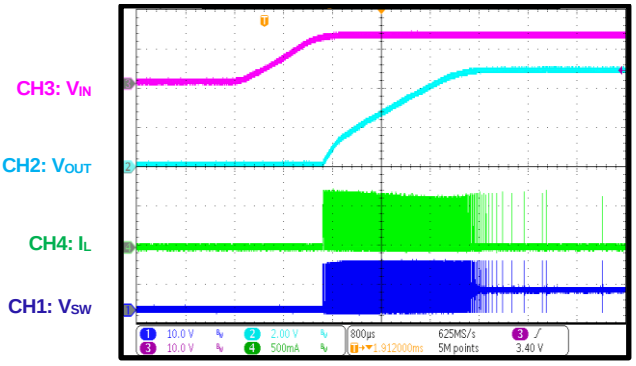
Steady State
I_{OUT} = 0A



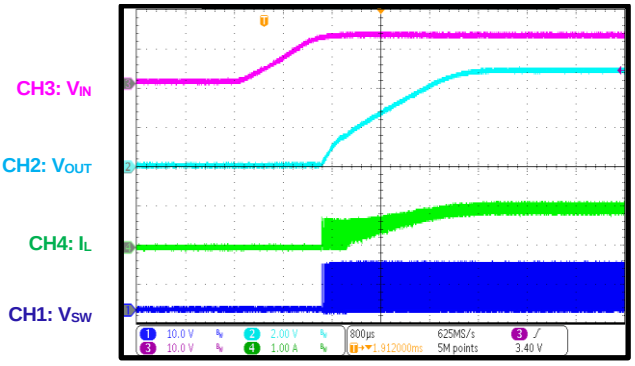
Steady State
I_{OUT} = 1A



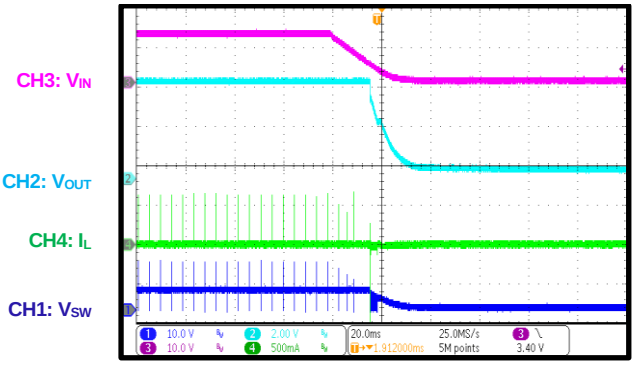
Start-Up through VIN
I_{OUT} = 0A



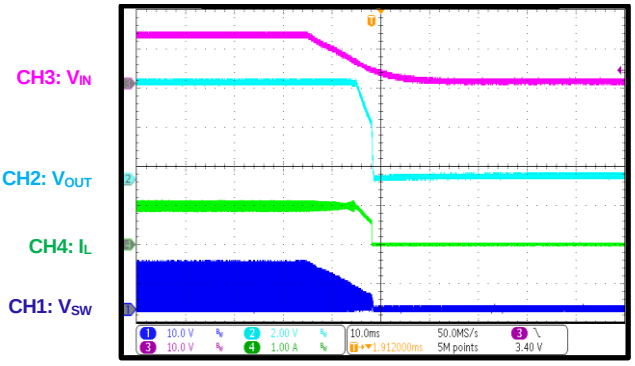
Start-Up through VIN
I_{OUT} = 1A



Shutdown through VIN
I_{OUT} = 0A



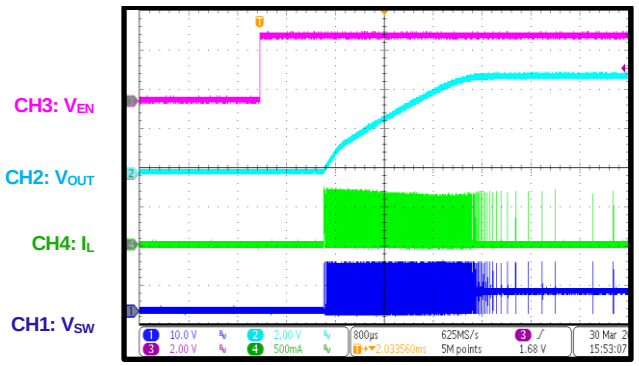
Shutdown through VIN
I_{OUT} = 1A



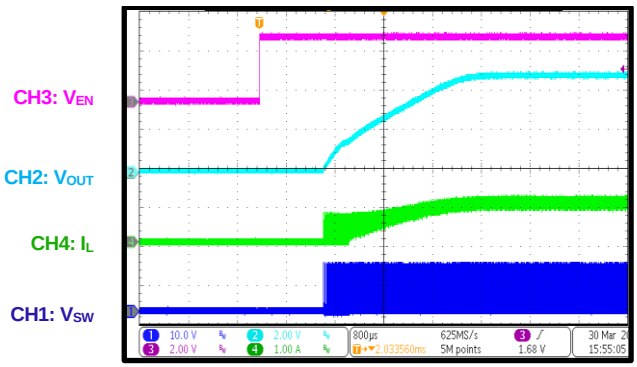
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 5.6µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

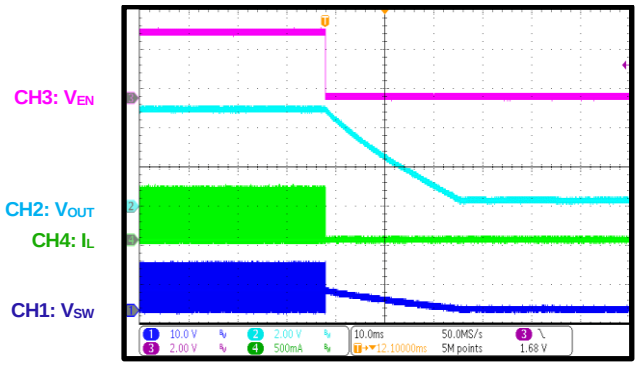
Start-Up through EN
I_{OUT} = 0A



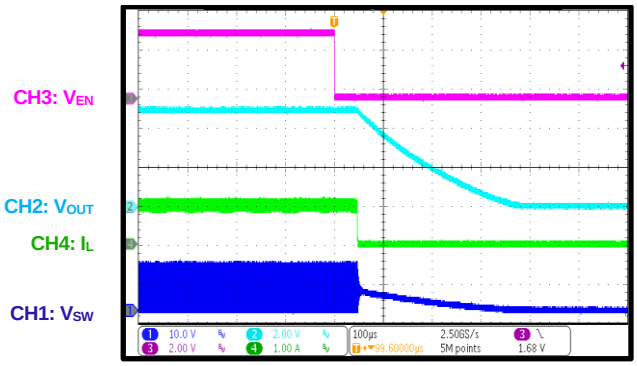
Start-Up through EN
I_{OUT} = 1A



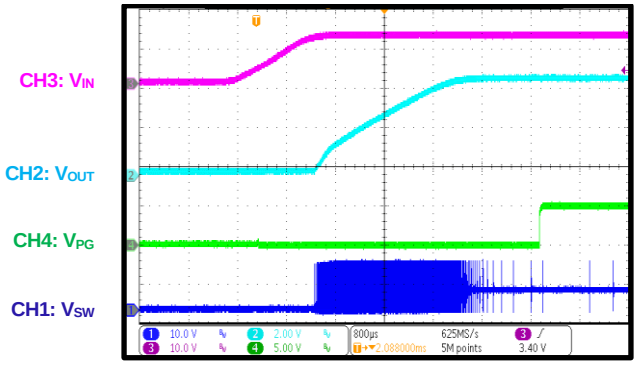
Shutdown through EN
I_{OUT} = 0A



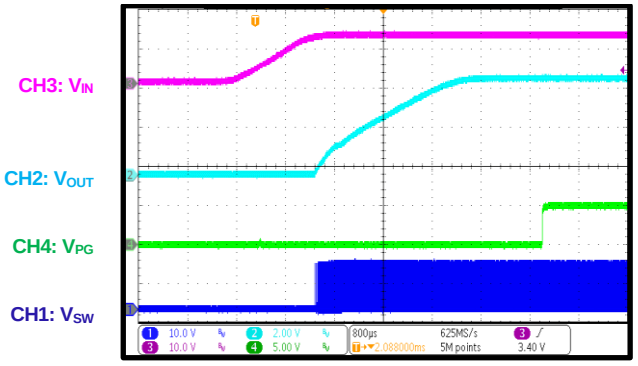
Shutdown through EN
I_{OUT} = 1A



PG Start-Up through VIN
I_{OUT} = 0A



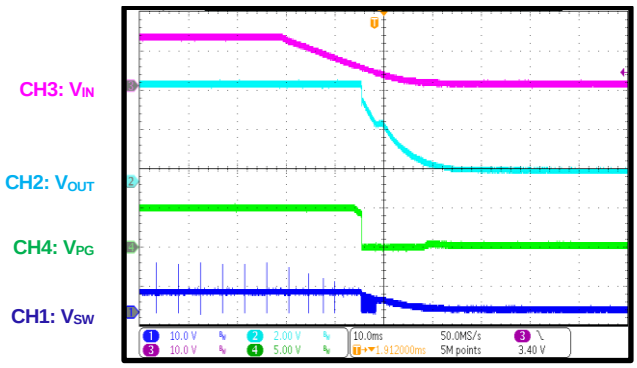
PG Start-Up through VIN
I_{OUT} = 1A



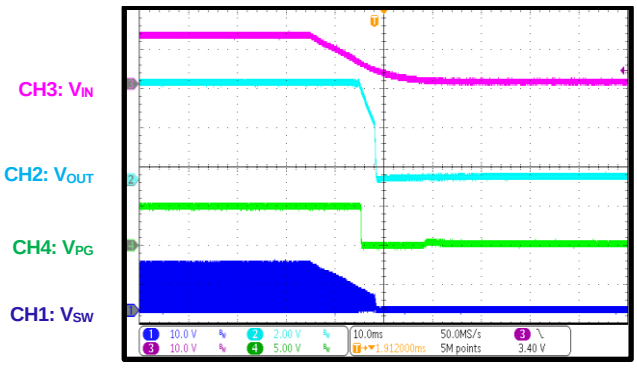
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 5.6µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

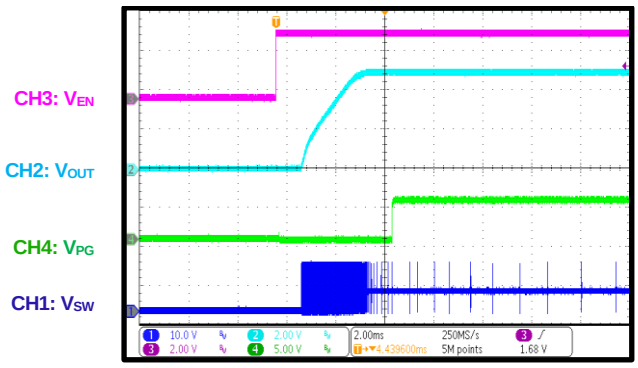
PG Shutdown through VIN
I_{OUT} = 0A



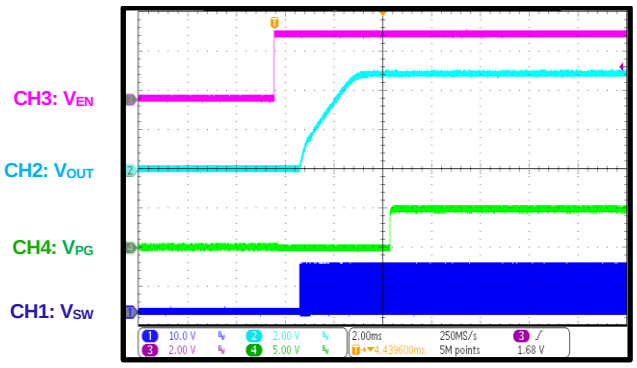
PG Shutdown through VIN
I_{OUT} = 1A



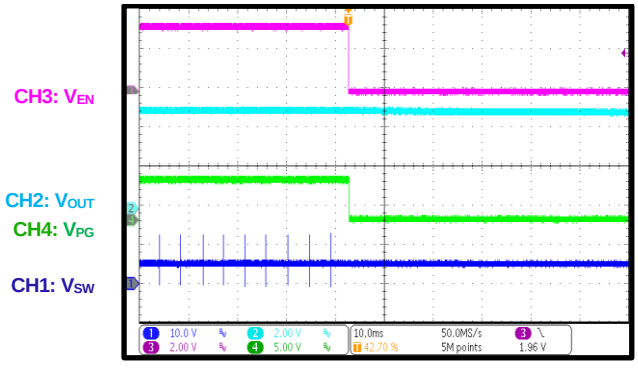
PG Start-Up through EN
I_{OUT} = 0A



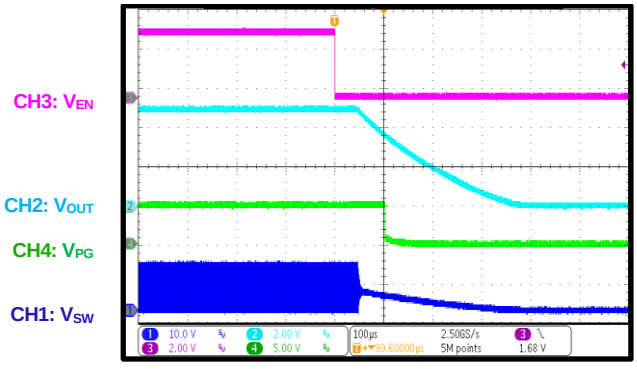
PG Start-Up through EN
I_{OUT} = 1A



PG in Shutdown through EN
I_{OUT} = 0A



PG in Shutdown through EN
I_{OUT} = 1A

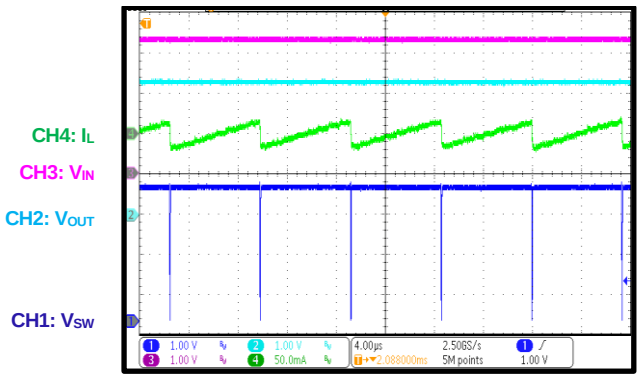


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 5.6µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

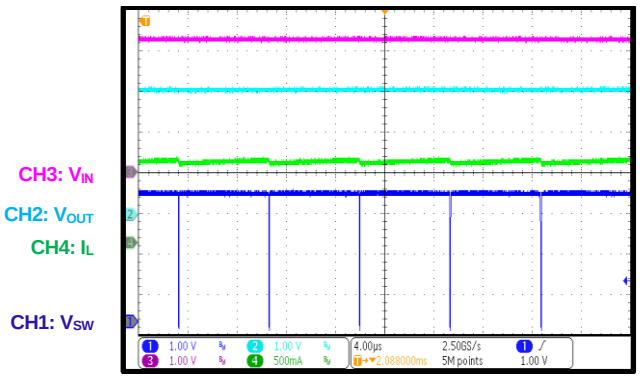
Low-Dropout Mode

I_{OUT} = 0A, V_{IN} = 3.3V



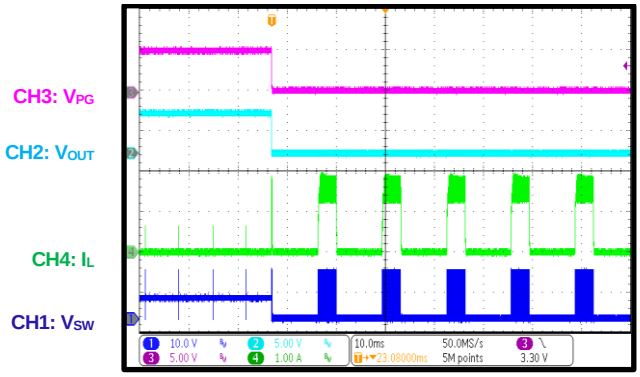
Low-Dropout Mode

I_{OUT} = 1A, V_{IN} = 3.3V



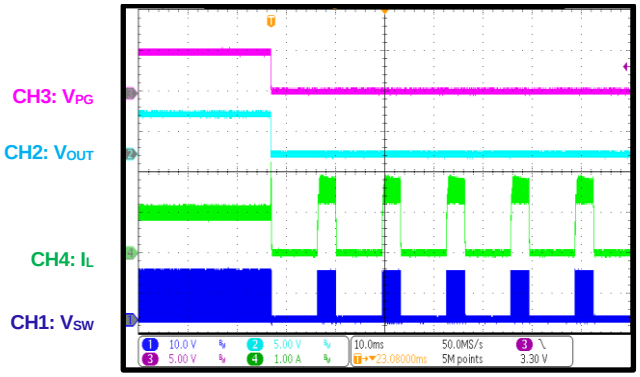
SCP Entry

I_{OUT} = 0A



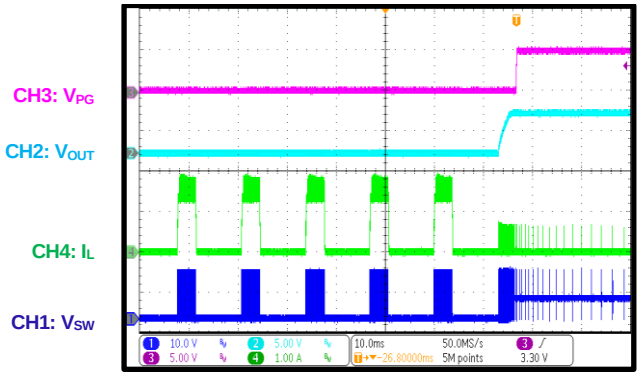
SCP Entry

I_{OUT} = 1A



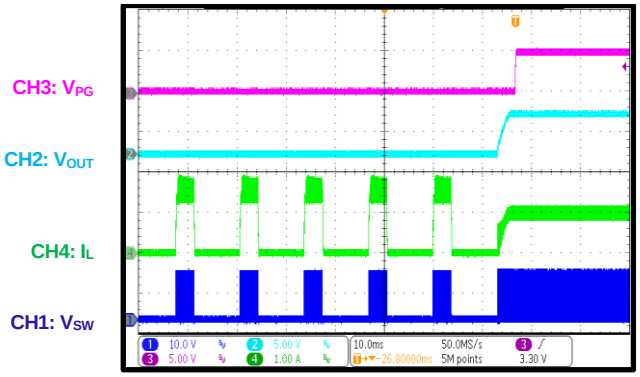
SCP Recovery

I_{OUT} = 0A



SCP Recovery

I_{OUT} = 1A

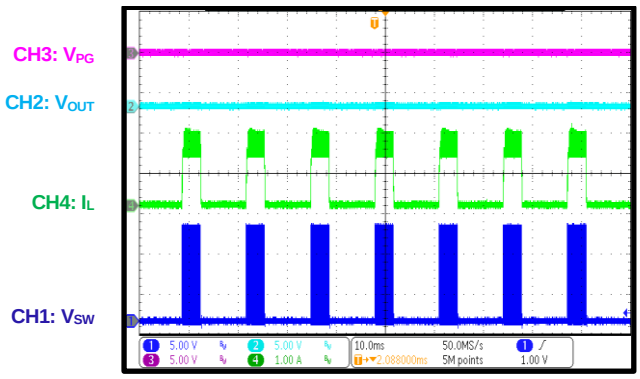


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 5.6µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

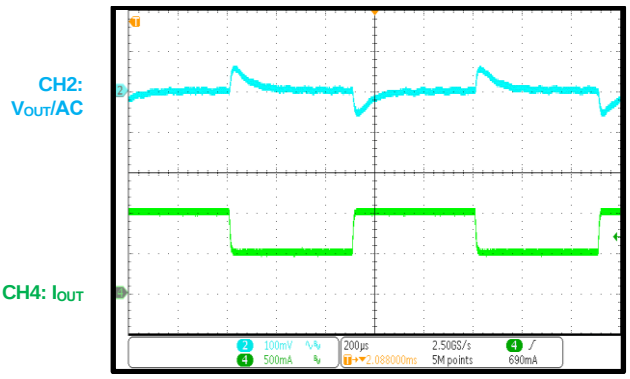
SCP Steady State

I_{OUT} = 0A



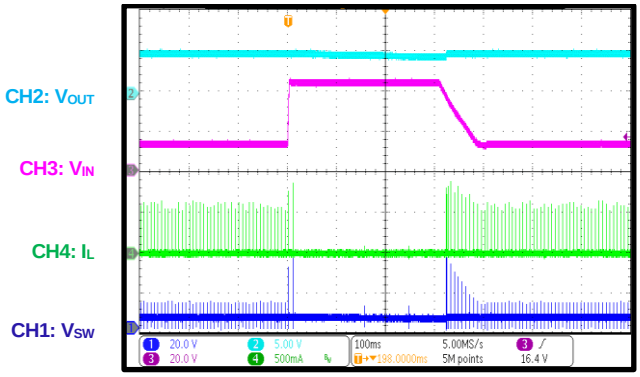
Load Transient

I_{OUT} = 0.5A to 1A, 1.6A/µs



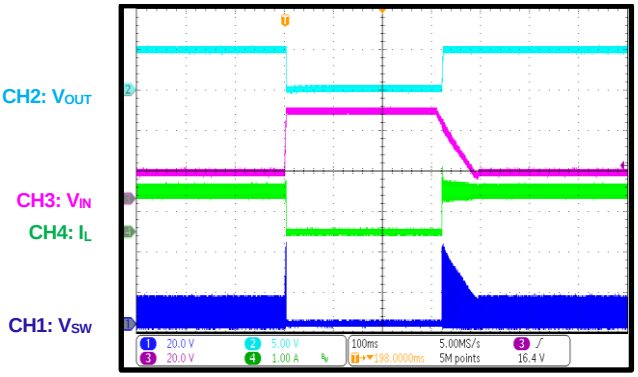
Load Dump

V_{IN}= 12V to 42V, I_{OUT} = 0A



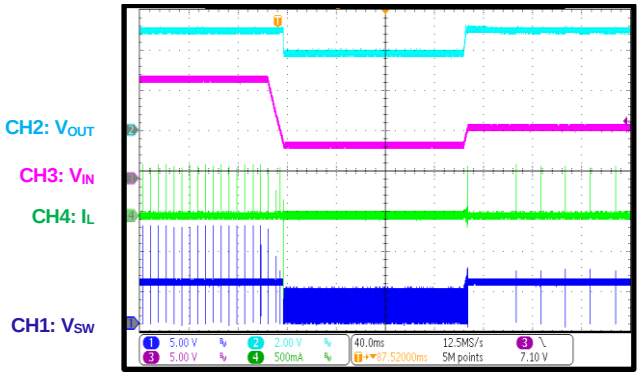
Load Dump

V_{IN} = 12V to 42V, I_{OUT} = 1A



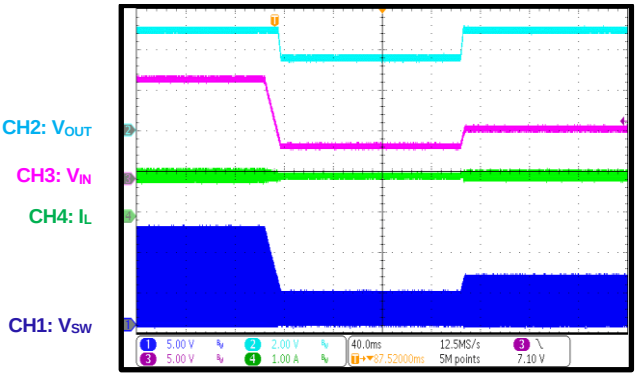
Cold Crank

V_{IN} = 12V to 3.3V to 6V, I_{OUT} = 0A



Cold Crank

V_{IN} = 12V to 3.3V to 6V, I_{OUT} = 1A

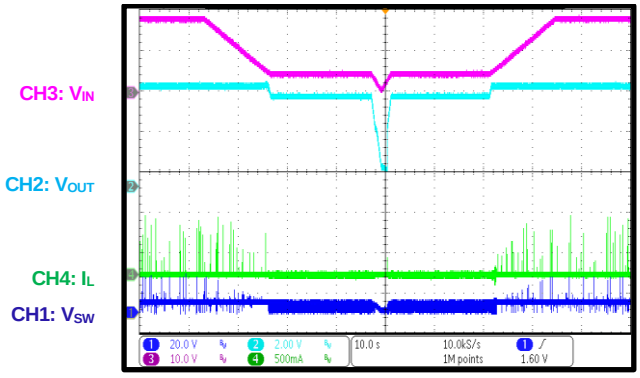


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 5.6µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

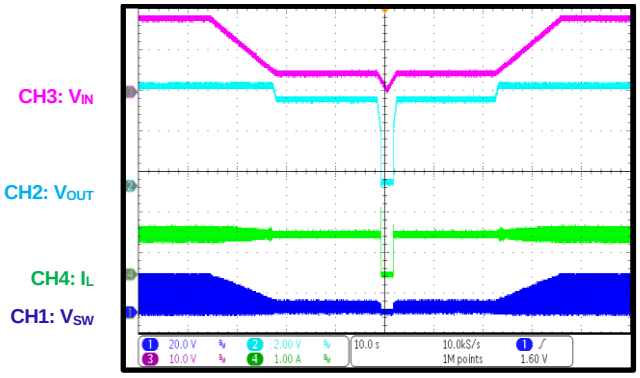
V_{IN} Ramps Down and Up

V_{IN} = 18V to 4.5V to 0V to 4.5V to 18V,
I_{OUT} = 0A



V_{IN} Ramps Down and Up

V_{IN} = 18V to 4.5V to 0V to 4.5V to 18V,
I_{OUT} = 1A



FUNCTIONAL BLOCK DIAGRAMS

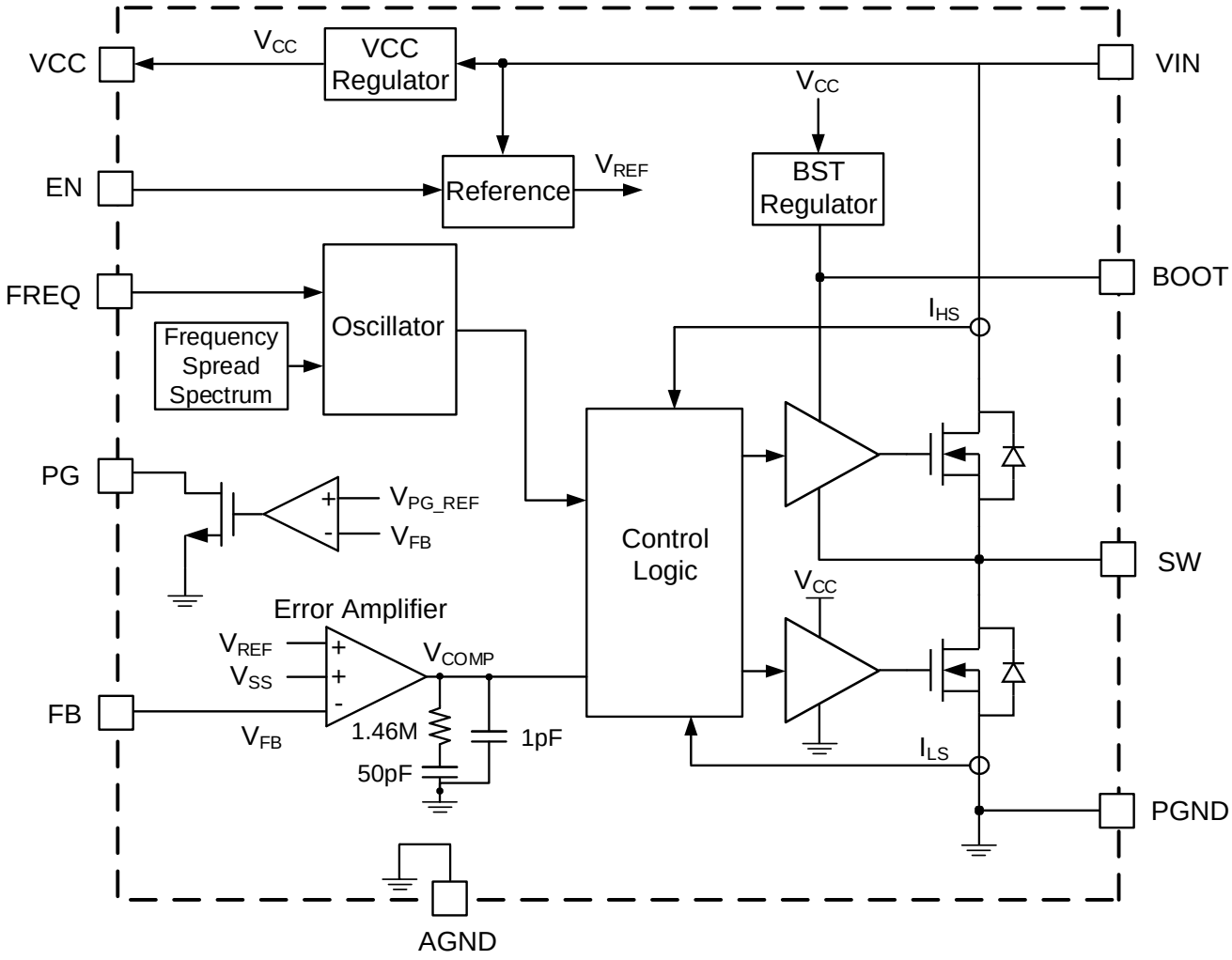


Figure 3: Functional Block Diagram (Adjustable Output)

FUNCTIONAL BLOCK DIAGRAMS *(continued)*

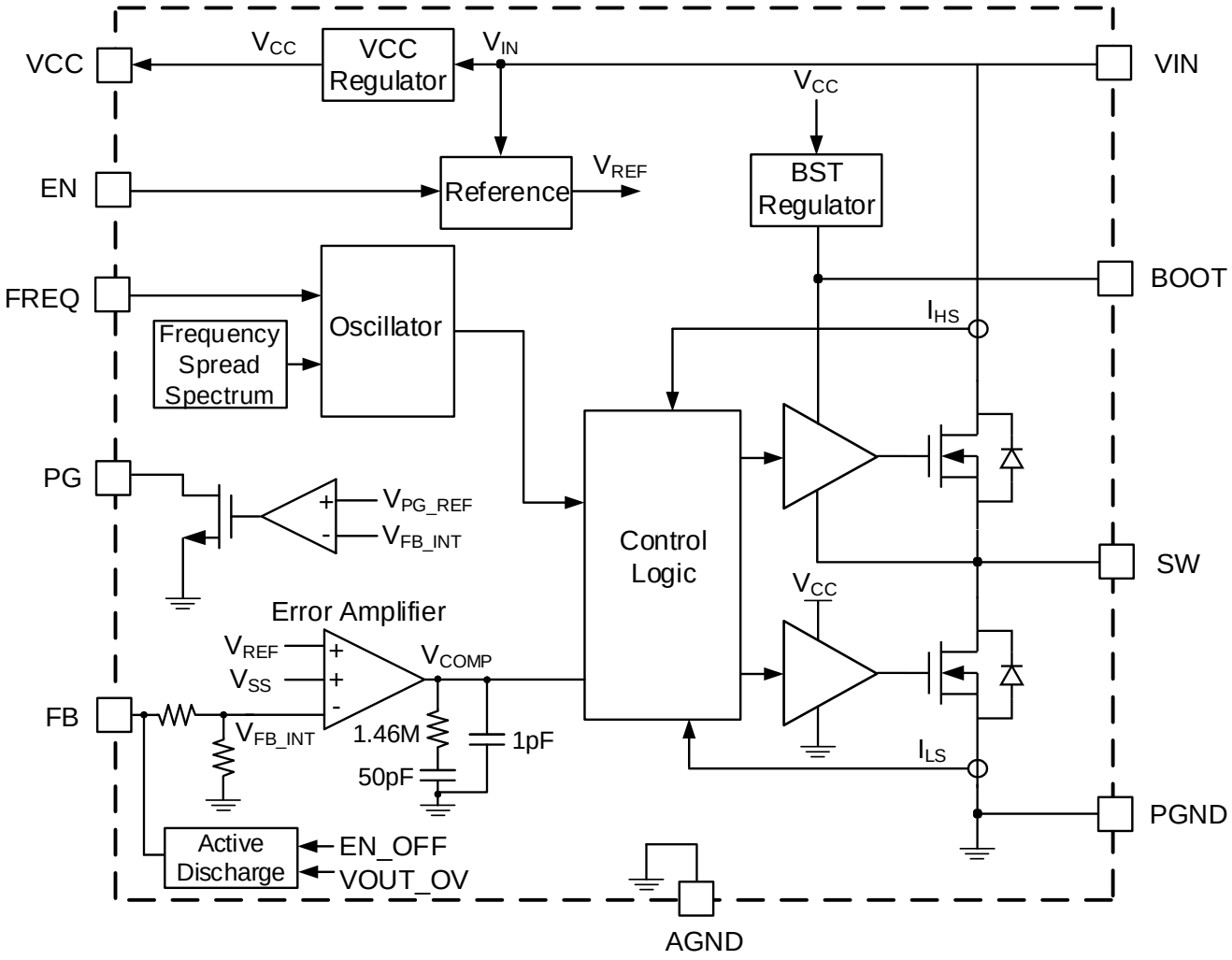


Figure 4: Functional Block Diagram (Fixed Output)

OPERATION

The MP4321 is a synchronous, step-down switching converter with integrated internal high-side and low-side power MOSFETs(HS-FET and LS-FET, respectively). It can achieve up to 1A of highly efficient output current (I_{OUT}) with peak current control mode.

The device features a wide input voltage range (V_{IN}) range, 350kHz to 2.5MHz configurable switching frequency (f_{SW}), internal soft start (SS), and precise current limit (I_{LIMIT}). The MP4321's low operational quiescent current (I_Q) makes it well-suited for battery-powered applications.

Pulse-Width Modulation (PWM) Control

At moderate to high output currents, the MP4321 operates with a fixed frequency, peak current control mode to regulate the output voltage (V_{OUT}). A PWM cycle is initiated by the internal clock. At the rising edge of the clock, the HS-FET turns on and remains on until the control signal reaches the value set by the internal COMP voltage (V_{COMP}).

If the HS-FET is off, then the LS-FET turns on and remains on until the next cycle starts or until the inductor current (I_L) drops below the zero current detection (ZCD) threshold. The LS-FET remains off for at least the minimum off time (t_{OFF_MIN}) before the next cycle starts.

If the current in the HS-FET cannot reach the value set by V_{COMP} within one PWM period, the HS-FET remains on and skips a turn-off operation. The HS-FET is forced off once it reaches the value set by V_{COMP}, or once its maximum on time (t_{ON_MAX}) (7µs) is complete. This mode extends the duty cycle, which achieves low dropout while $V_{IN} \approx V_{OUT}$.

Light-Load Operation

The MP4321 operates in advanced asynchronous modulation (AAM) mode to optimize efficiency under light-load and no-load conditions.

The MP4321 enters asynchronous operation as the inductor current (I_L) approaches 0A under light-load conditions. If the load decreases further, V_{COMP} drops to its set value, and the device enters AAM mode (see Figure 5).

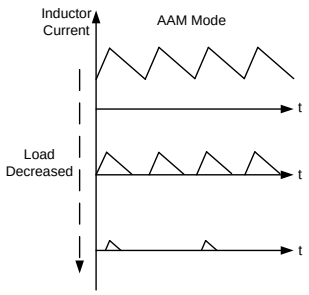


Figure 5: AAM Mode

In AAM mode, the internal clock is resets once V_{COMP} reaches its set value. The crossover time is used as a benchmark for the next clock. If the load increases and V_{COMP} exceeds its set value, then the device operates in continuous conduction mode (CCM) or discontinuous conduction mode (DCM), which have a constant f_{SW}.

Error Amplifier (EA)

The error amplifier (EA) compares the feedback (FB) voltage (V_{FB}) to the internal reference voltage (V_{REF}) (typically 0.8V), and outputs a current that is proportional to the difference between the voltages. This I_{OUT} charges the compensation network to set V_{COMP}, which controls the power MOSFET's current.

During normal operation, the minimum V_{COMP} is 0.5V, and the maximum is 2V. If the IC shuts down, V_{COMP} is pulled down to AGND internally.

Frequency Spread Spectrum (FSS)

The MP4321 employs a 15kHz modulation frequency and a 128-step triangular profile to spread the internal f_{SW} across a 20% (±10%) window. The steps vary with the f_{SW} to ensure that the exact f_{SW} steps cycle by cycle (see Figure 6).

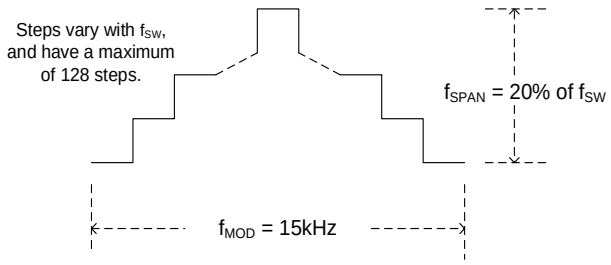


Figure 6: Frequency Spread Spectrum

Sidebands are created by modulating f_{SW} via the triangle modulation waveform. The emission power of the fundamental f_{SW} and its harmonics are reduced. This significantly reduces peak EMI noise.

Soft Start (SS)

Soft start (SS) is implemented to prevent V_{OUT} from overshooting during start-up. The soft-start time (t_{SS}) is fixed internally.

Once an SS is initiated, the soft-start voltage (V_{SS}) rises from 0V to 1.2V according to the internal slew rate. If V_{SS} drops below the internal V_{REF} (0.8V), then V_{SS} takes over and the EA uses V_{SS} as its reference. If V_{SS} exceeds V_{REF}, then the EA uses V_{REF} as its reference.

During start-up through EN, the first pulse occurs after about 830µs. The VCC voltage (V_{CC}) is regulated, the internal bias is generated, and the compensation network is charged. Then V_{OUT} ramps up and reaches its set value after 2.9ms. SS is complete after 1.5ms. PG is also be pulled high after a 70µs delay.

Pre-Biased Start-Up

If V_{FB} exceeds V_{SS} during start-up, this means that the output has a pre-biased voltage. Both the HS-FET and LS-FET remain off until V_{SS} exceeds V_{FB}.

Thermal Shutdown

Thermal shutdown prevents the device from operating at exceedingly high temperatures. If the die temperature exceeds the thermal shutdown threshold (about 175°C), the device shuts down. Once the temperature drops below 155°C, the device initiates an SS to resume normal operation.

Start-Up and Shutdown

If both V_{IN} and the EN voltage (V_{EN}) exceed their respective thresholds, the IC starts up. The reference block starts up first to generate a stable V_{REF} and reference currents. Then the internal regulator turns on to provide a stable supply for the remaining circuitries.

Once the internal supply rail is up, then the internal circuits being normal operation. If the BOOT voltage (V_{BOOT}) does not reach its refresh rising threshold (about 2.5V), then the LS-FET turns on to charge BOOT. The HS-FET remains off during this charging period. Once an SS is initiated, V_{OUT} starts to ramp up slowly until it reaches its target voltage. V_{OUT} should reach its target voltage within 5ms.

Three events can shut down the chip: EN goes low, V_{IN} drops below its UVLO threshold, and thermal shutdown. During shutdown, the signaling path is blocked to avoid any fault triggering. Then V_{COMP} is pulled down, and the HS-FET turns off.

APPLICATION INFORMATION

Selecting the Input Capacitor (C_{IN})

The step-down converter has a discontinuous input current (I_{IN}), and requires a capacitor to supply AC current to the converter while maintaining the DC V_{IN}. Use low-ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are recommended due to their low ESR and small temperature coefficients.

For most applications, a 4.7µF to 10µF is sufficient. It is strongly recommended to use an additional lower-value capacitor (e.g. 0.1µF) with a small package size (0603) to absorb high-frequency switching noise. Place the smaller capacitor as close to the VIN and AGND pins as possible.

Since the input capacitor (C_{IN}) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in C_{IN} (I_{CIN}) can be estimated with Equation (1):

$$I_{CIN} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (1)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, which can be calculated with Equation (2):

$$I_{CIN} = \frac{I_{LOAD}}{2} \quad (2)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current (I_{LOAD_MAX}). C_{IN} can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1µF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple (ΔV_{IN}) caused by the capacitance can be estimated with Equation (3):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (3)$$

V_{IN} Over-Voltage Protection (OVP)

The MP4321 stops switching once V_{IN} exceeds its over-voltage protection (OVP) rising threshold (37.5V). The device resumes normal operation once V_{IN} drops below the over-voltage falling threshold (36.5V).

Floating Driver and Bootstrap (BST) Charging

It is recommended to choose a BOOT capacitor (C_{BOOT}) that is between 22nF and 100nF.

It is not recommended to place a resistor (R_{BOOT}) in series with C_{BOOT}, unless there is a strict EMI requirement. R_{BOOT} reduces EMI and voltage stress at high input voltages; however, it also generates additional power consumption and reduces efficiency. If necessary, choose R_{BOOT} to be below 4Ω.

The voltage between BOOT and SW (V_{BOOT}) is regulated to about 5V by the dedicated internal bootstrap regulator. If V_{BOOT} drops below its regulated value, then a N-channel MOSFET pass transistor connected between VCC and BOOT turns on to charge C_{BOOT}. The external circuit should provide enough voltage headroom to facilitate charging. If the HS-FET is ON, BOOT is higher than VCC so the bootstrap capacitor can't be charged.

At higher duty cycles, the time available to charge C_{BOOT} is shorter. C_{BOOT} may not be charged sufficiently since the external circuit does not have sufficient voltage or time to charge C_{BOOT}. External circuitry can ensure that V_{BOOT} remains within its normal operating range.

If V_{BOOT} exceeds its UVLO threshold, then the HS-FET turns off, and the LS-FET turns on. The LS-FET has a t_{OFF_MIN} to refresh V_{BOOT} via f_{SW}.

Setting the Switching Frequency (f_{SW})

f_{SW} can be set via an external resistor (R_{FREQ}) connected between the FREQ and AGND pins (see the f_{SW} vs. R_{FREQ} curves on and page 15).

Connect R_{FREQ} between the FREQ and AGND pins, placed as close to the IC as possible.

Table 1 shows the resistor values for different f_{SW}.

Table 1: f_{SW} vs. R_{FREQ}

R_{FREQ} (kΩ)	f_{SW} (kHz)	R_{FREQ} (kΩ)	f_{SW} (kHz)
100	355	30.1	1150
93.1	385	26.1	1300
86.6	415	22.6	1450
80.6	450	20.5	1600
75	480	19.6	1750
68.1	520	17.8	1900
59	600	16.2	2050
51.1	700	15	2200
40.2	850	14.3	2350
34.8	1000	13.3	2500

It is not possible to have both a high f_{SW} and a high V_{IN} due to the HS-FET's minimum on time (t_{ON_MIN}). The control loop sets the maximum possible f_{SW} as the set frequency automatically. This also reduces power loss. V_{OUT} is regulated by varying the duration of the HS-FET's off time (t_{OFF}), which reduces f_{SW}.

The device is guaranteed to adhere to the HS-FET's t_{ON_MIN}. This means that the device operates at the target f_{SW} for as long as possible, and f_{SW} changes only while the device is operating at a high V_{IN}. For more details, see the f_{SW} vs. V_{IN} curve on page 15, where R_{FREQ} = 15kΩ and V_{OUT} = 3.3V.

Selecting the Internal VCC Capacitor

It is recommended to use a 1µF VCC capacitor (C_{VCC}). Most of the internal circuitry is powered by the internal 5V VCC regulator. This regulator uses the VIN pin as its input to operate across the entire V_{IN} range. If V_{IN} exceeds 5V, then VCC is in full regulation. If V_{IN} drops below 5V, then the VCC output degrades.

Setting the Feedback (FB) Voltage

If the device has an adjustable output, the feedback voltage (V_{FB}) is typically 0.8V. The external resistor divider (R_5 + R_6) sets the output voltage (see Figure 7).

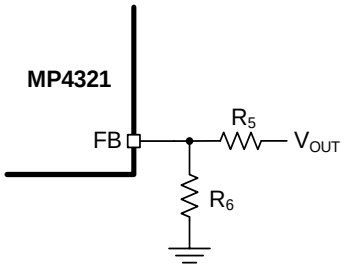


Figure 7: FB Network with Adjustable Output

R_6 can be calculated with Equation (4):

$$R_6 = \frac{R_5}{\frac{V_{OUT}}{0.8V} - 1} \quad (4)$$

With a fixed output, the FB resistor divider is integrated internally. This means that the FB pin should be connected to the output directly to set V_{OUT}. The following fixed outputs can be selected: 1V, 1.8V, 2.5V, 3.0V, 3.3V, 3.8V, and 5V (see Figure 8).

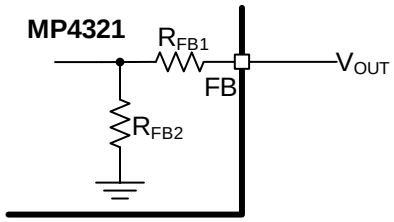


Figure 8: FB Network with Fixed Output

Table 2 shows the resistor values for different V_{OUT}.

Table 2: R_{FB} vs. V_{OUT}

V_{OUT} (V)	R_{FB1} (kΩ)	R_{FB2} (kΩ)
1	64	256
1.8	320	256
2.5	544	256
3	704	256
3.3	800	256
3.8	960	256
5	1344	256

Power Good (PG) Indication

The PG resistor (R_7) should have a resistance of about 100kΩ. The MP4321 includes an open-drain power good (PG) output that indicates whether V_{OUT} is within its nominal range.

Connect PG to a logic high power source (e.g. 3.3V) via a pull-up resistor. If V_{OUT} is within 94.5% to 105.5% of the nominal voltage, then PG is pulled high. If V_{OUT} exceeds 107% or drops below 93% of the nominal voltage, then PG is pulled low. Float PG if not used.

Enable (EN) and Under-Voltage Lockout (UVLO) Protection

The enable (EN) pin is a digital control pin that turns the converter on and off.

Enable via External Logic High/Low Signal

If the EN voltage (V_{EN}) reaches 0.7V, then the bottom gate (BG) turns on once V_{IN} exceeds 2.7V. BG turns on to provides an accurate V_{REF} for the V_{EN} threshold. Pull EN above 1.02V to turns the converter on; pull EN below 0.85V to turn it off. There is no internal pull-up or pull-down resistor connected to the EN pin. Do not float EN. An external pull-up or pull-down resistor is required if the control signal cannot give an accurate high or low logic.

Configurable V_{IN} UVLO Protection

The MP4321 has an internal, fixed UVLO threshold. The rising threshold is 3.65V, and the falling threshold is about 2.9V. For applications requiring a higher UVLO point, place an external resistor divider between the VIN and EN pins (see Figure 9).

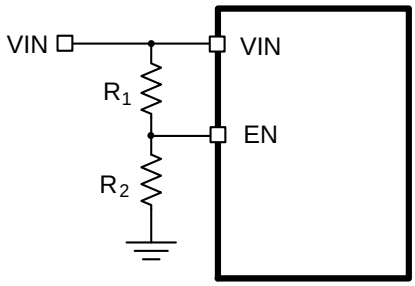


Figure 9: Configurable UVLO via the EN Divider

The UVLO rising threshold can be calculated with Equation (5):

$$V_{IN\_UVLO\_RISING} = (1+\frac{R_1}{R_2}) \times V_{EN\_RISING} \quad (5)$$

Where V_{EN_RISING} is 1.02V.

The UVLO falling threshold can be calculated with Equation (6):

$$V_{IN\_UVLO\_FALLING} = (1+\frac{R_1}{R_2}) \times V_{EN\_FALLING} \quad (6)$$

Where $V_{EN\_FALLING}$ is 0.85V.

If EN is not used to turn the IC on and off, connect EN to a high voltage source (e.g. VIN) to turn the device on by default.

Selecting the Inductor and the Output Capacitors

The inductor (L_1) can be estimated with Equation (7):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1-\frac{V_{OUT}}{V_{IN}}) \quad (7)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

For most applications, a inductor with a DC current rating that exceeds at least 25% of I_{LOAD_MAX} is recommended. For higher efficiency, choose an inductor with a lower DC resistance. A larger-value inductor results in less ripple current and a lower output ripple voltage (ΔV_{OUT}); however, a larger-value inductor has a larger physical size, higher series resistance, and lower saturation current. A good rule to determine the inductance is to have the inductor ripple current be approximately 30% of the I_{LOAD_MAX}.

The peak inductor current (I_{L_PEAK}) can be calculated with Equation (8):

$$I_{L\_PEAK} = I_{LOAD} + \frac{V_{OUT}}{2 \times f_{SW} \times L} \times (1-\frac{V_{OUT}}{V_{IN}}) \quad (8)$$

Choose an inductor that does not saturate under I_{L_PEAK}.

ΔV_{OUT} can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1-\frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (9)$$

The output capacitor (C_{OUT}) maintains the DC V_{OUT}. Use ceramic, tantalum, or low-ESR electrolytic capacitors for C_{OUT}. For the best results, use low-ESR capacitors to keep ΔV_{OUT} low.

When using ceramic capacitors**,** the capacitance dominates the impedance at f_{SW} and causes the majority of ΔV_{OUT}. For simplification, ΔV_{OUT} can be calculated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1-\frac{V_{OUT}}{V_{IN}}) \quad (10)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at f_{SW}. For simplification, ΔV_{OUT} can be estimated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1-\frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (11)$$

When selecting C_{OUT}, consider the allowed V_{OUT} overshoot if the load is suddenly removed. In this scenario, energy stored in the inductor is transferred to C_{OUT}, causing its voltage to rise. To achieve optimal overshoot relative to the regulated voltage, C_{OUT} can be estimated with Equation (12):

$$C_{OUT} = \frac{I_{OUT}^2 \times L}{V_{OUT}^2 \times ((V_{OUTMAX} / V_{OUT})^2 - 1)} \quad (12)$$

Where V_{OUTMAX} / V_{OUT} is the allowable maximum overshoot.

After calculating the capacitance that meets both the ripple requirement and overshoot requirement, choose the larger of the two capacitances for application.

The characteristics of C_{OUT} also affect the stability of the regulation system. The MP4321 can be optimized for a wide range of capacitances and ESR values.

Peak and Valley Current Limits

Both the HS-FET and LS-FET feature cycle-by-cycle current limiting. If I_L reaches the high-side peak current limit (I_{LIMIT_HS}) (typically 2A) while the HS-FET is on, then the HS-FET turns off to prevent the current from rising further.

If the LS-FET is on, the next clock's rising edge is held until I_L drops below the low-side valley current limit (I_{LIMIT_LS}) (typically 1.5A). I_L drops to a sufficiently low value once the HS-FET turns on again. This prevents current runaway if an overload condition or short-circuit occurs.

Short-Circuit Protection (SCP)

If the output is shorted to ground and V_{OUT} drops below 70% of its nominal voltage, then the part shuts down and discharges V_{SS}. Once V_{SS} is fully discharged, the device initiates an SS to resume normal operation. This hiccup process is repeated until the fault is removed.

Output Over-Voltage Protection (OVP) and Discharge

If V_{OUT} exceeds 130% of its nominal voltage, then the MP4321 shuts down. An internal 75Ω discharge path between the FB to AGND pins discharges V_{OUT}. This discharge path is only active with a fixed output. The part resumes normal operation once V_{OUT} drops below 125% of its nominal voltage, and the discharge path is disabled.

For a fixed output, the V_{OUT} discharge path also activates if a shutdown through EN occurs while V_{CC} exceeds its under-voltage lockout (UVLO) rising threshold. Once V_{CC} drops below its UVLO falling threshold, the discharge path is deactivated.

Design Guide

Table 3 shows the design guide index.

Table 3: Design Guide Index

Pin #	Name	Component	Design Guide Index
1, 11	PGND		Ground connection (PGND, pin 1, pin 6, and pin 11)
2, 10	VIN	C1A, C1B, C1C, C1D	Selecting the input capacitors (VIN, pin 2, and pin 10)
3	BOOT	R4, C4	Floating driver and bootstrap charging (BOOT, pin 3)
4	FREQ	R3	Setting f_{SW} (FREQ, pin 4)
5	VCC	C3	Setting the internal V_{CC} (VCC, pin 5)
6	AGND		Ground connection (AGND, pin 1, pin 6, and pin 11)
7	FB	R5, R6	Feedback (FB, pin 7)
8	PG	R7	Power good indication (PG, pin 8)
9	EN	R1, R2	Enable (EN) and configuring UVLO (EN, pin 9)
12	SW	L1, C2A, C2B	Selecting the inductor and the output capacitor (SW, pin 12)

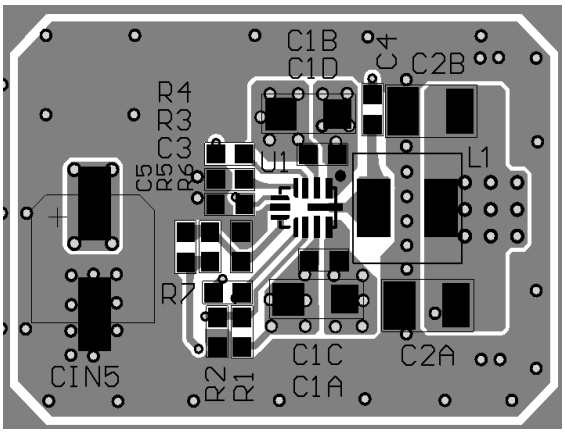
PCB Layout Guidelines (14)

Efficient PCB layout is critical for stable operation, especially the placement of the input capacitor. A 4-layer layout is recommended to improve thermal performance. For the best results, refer to Figure 10 and follow the guidelines below:

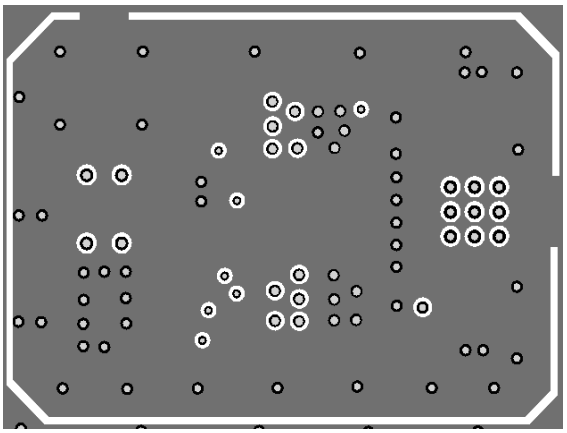
1. Place the symmetric input capacitors as close to VIN and AGND as possible.
2. Use a large ground plane to connect PGND.
3. If the bottom layer is a ground plane, place multiple vias near PGND.
4. Connect the high-current paths (AGND and VIN) using short, direct, and wide traces.
5. To minimize high-frequency noise, place the ceramic input capacitors, especially the small-sized (0603) input bypass capacitor, as close to VIN and PGND as possible.
6. Keep the connection between the input capacitor and VIN as short and wide as possible.
7. Place the VCC capacitor as close to VCC and AGND as possible.
8. Route SW and BOOT away from sensitive analog areas, such as FB.
9. Place the feedback resistors as close to the IC as possible to make the FB trace as short as possible.
10. Use multiple vias to connect the power planes to the internal layers.

Note:

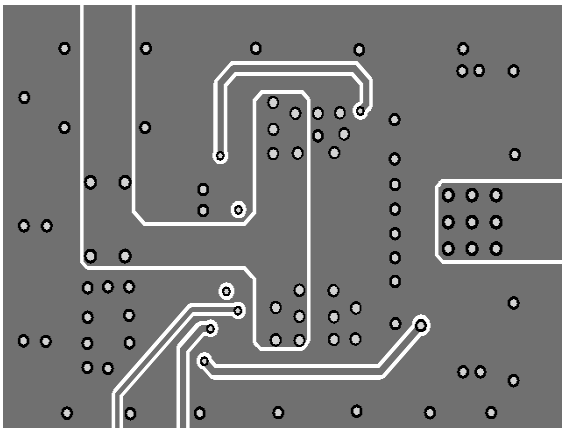
14) The recommended PCB layout is based on Figure 11 on page 35.



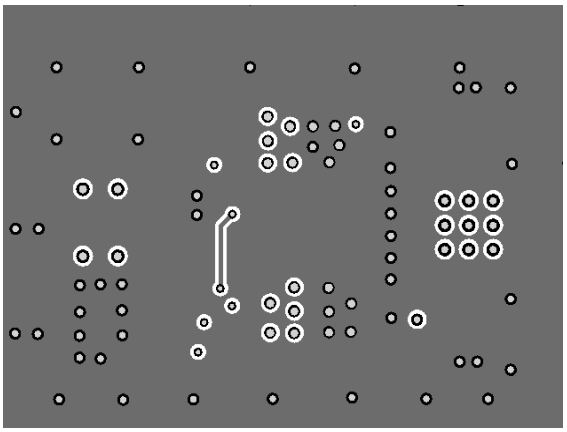
Top Silk and Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer and Bottom Silk

Figure 10: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

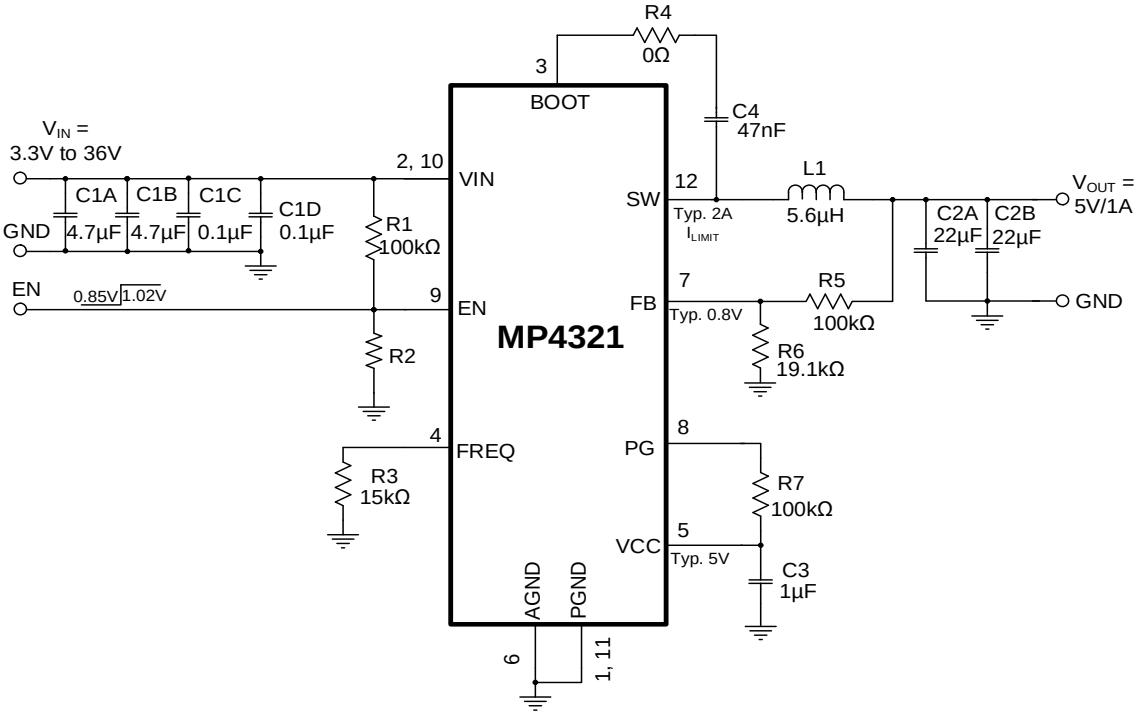


Figure 11: Typical Application Circuit with Bootstrap Resistor (R4) (V_{OUT} = 5V, f_{SW} = 2.2MHz)

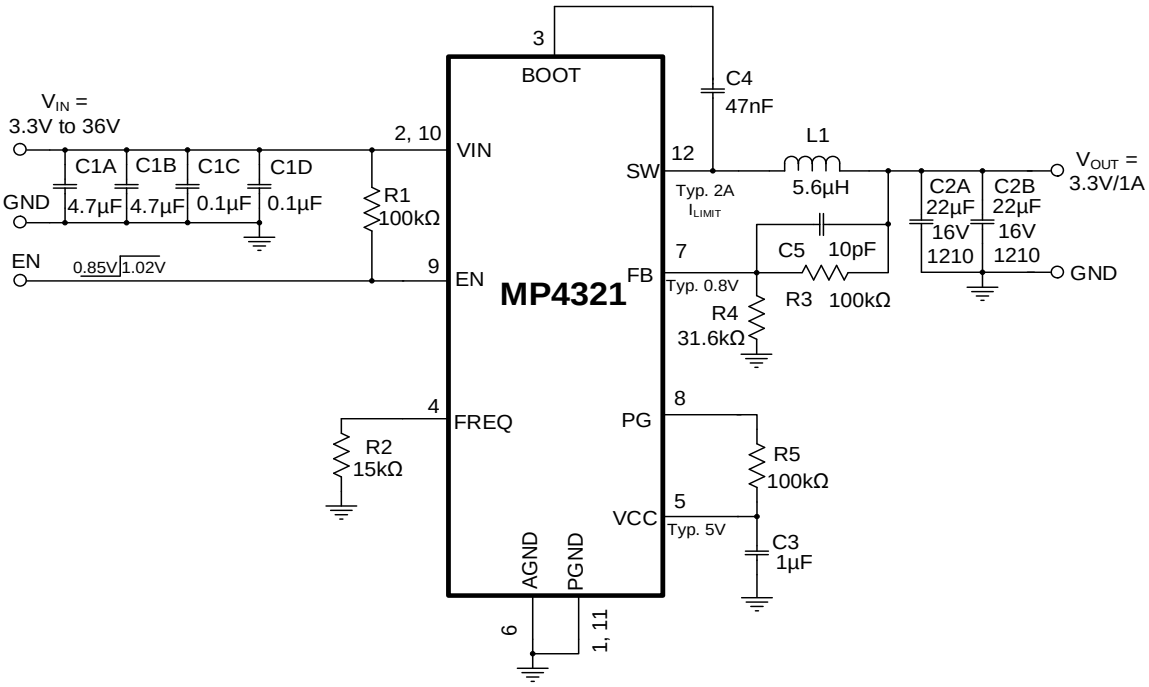


Figure 12: Typical Application Circuit (V_{OUT} = 3.3V, f_{SW} = 2.2MHz)

TYPICAL APPLICATION CIRCUITS *(continued)*

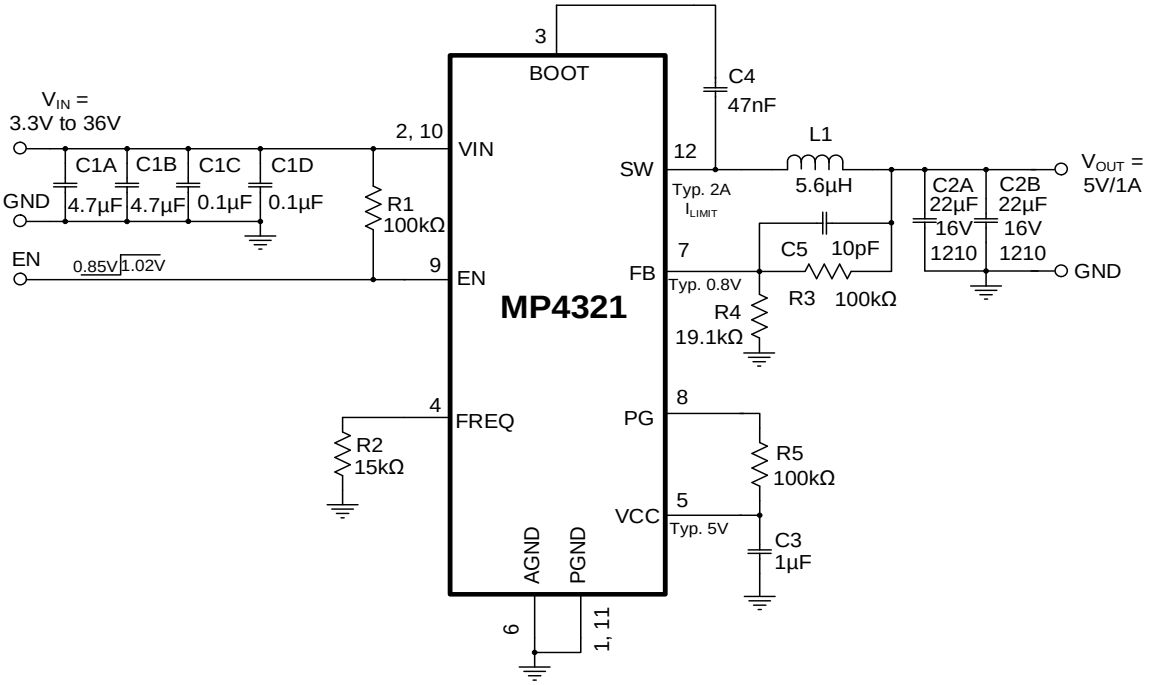


Figure 13: Typical Application Circuit (V_{OUT} = 5V, f_{SW} = 2.2MHz)

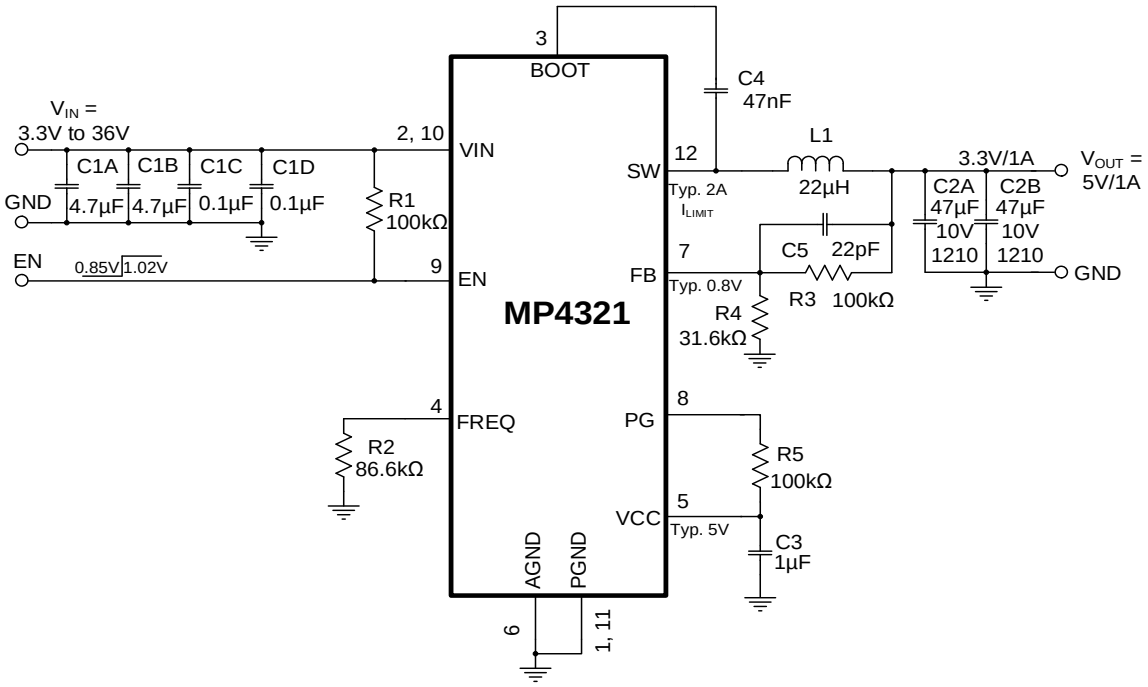


Figure 14: Typical Application Circuit (V_{OUT} = 3.3V, f_{SW} = 415kHz)

TYPICAL APPLICATION CIRCUITS *(continued)*

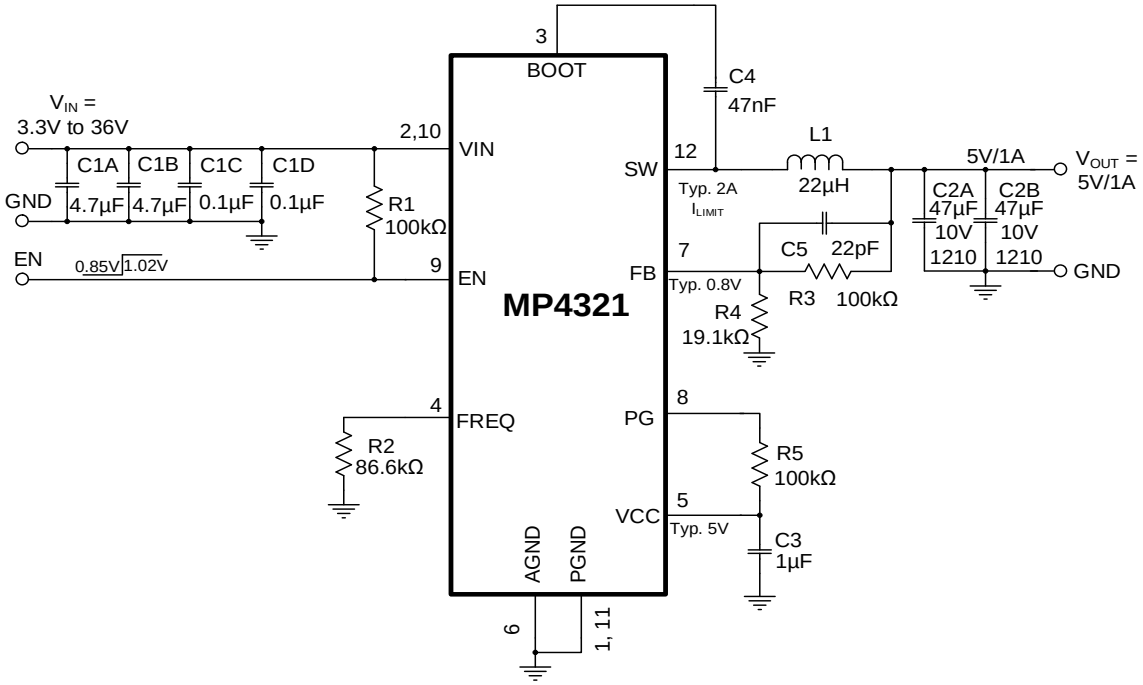


Figure 15: Typical Application Circuit (V_{OUT} = 5V, f_{SW} = 415kHz)

TYPICAL APPLICATION CIRCUITS *(continued)*

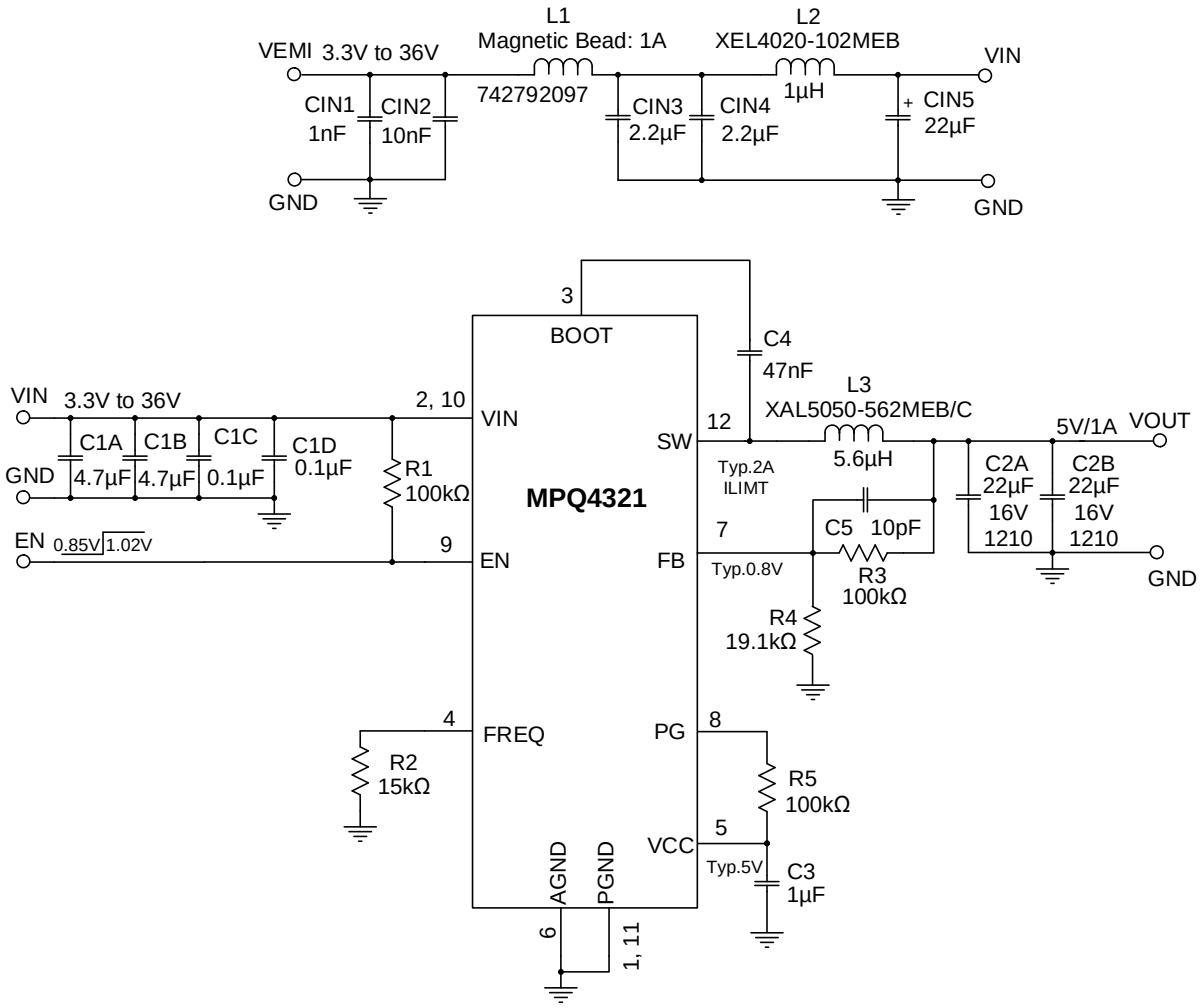


Figure 16: Typical Application Circuit (V_{OUT} = 5V, f_{SW} = 2.2MHz with EMI Filters)

TYPICAL APPLICATION CIRCUITS *(continued)*

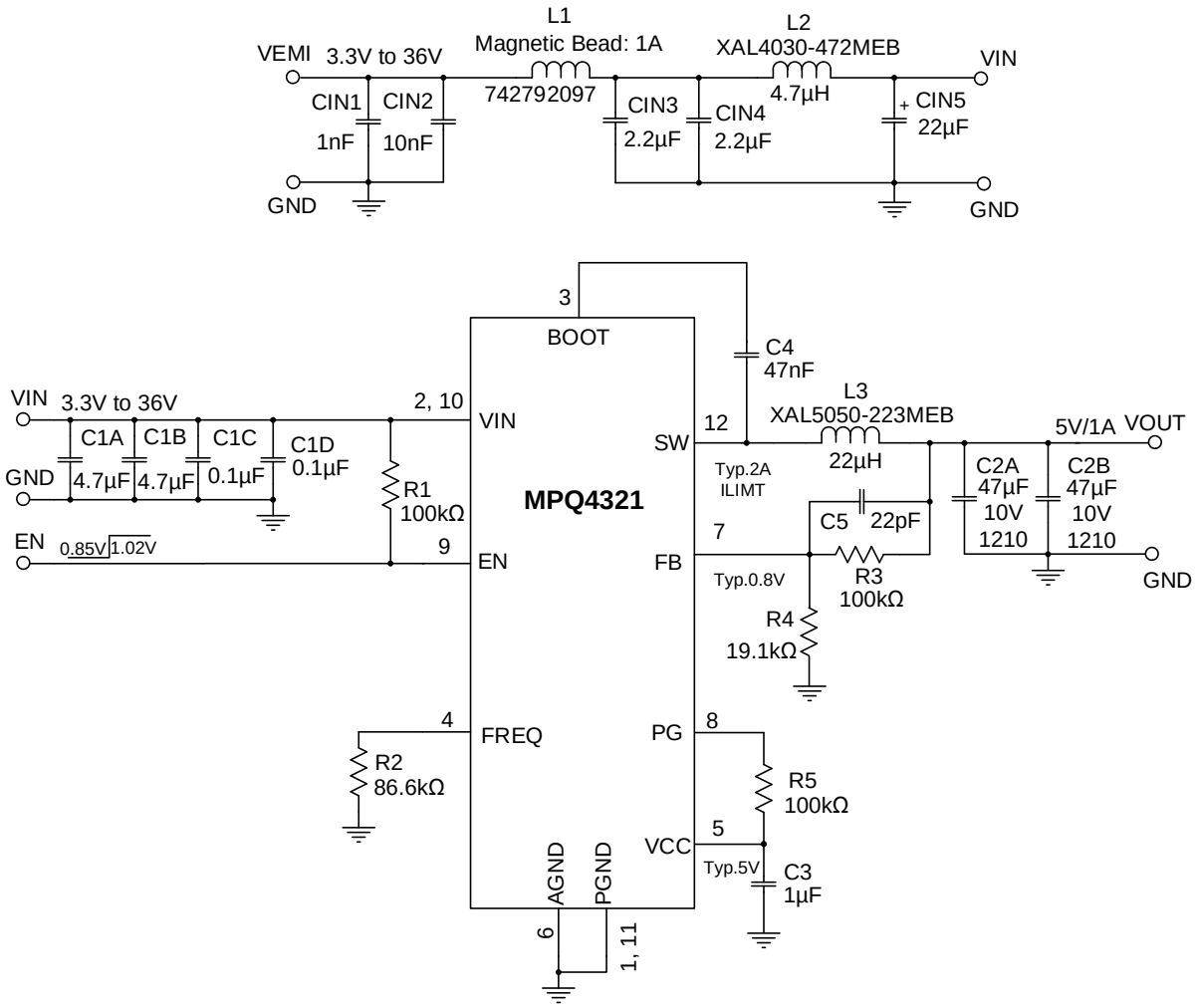
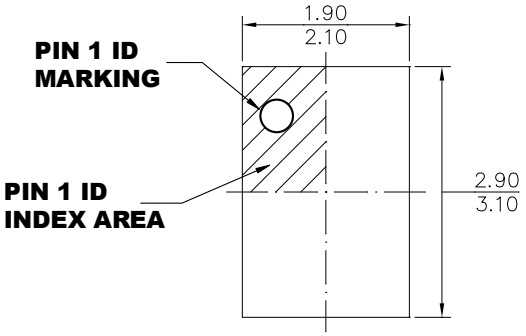


Figure 17: Typical Application Circuit (V_{OUT} = 5V, f_{SW} = 415kHz with EMI Filters)

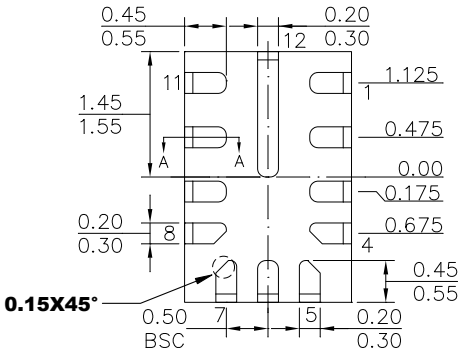
PACKAGE INFORMATION

QFN-12 (2mmx3mm)

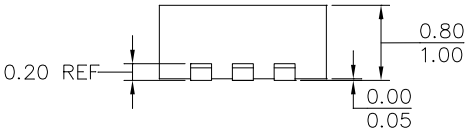
Wettable Flank



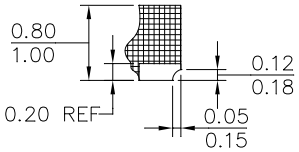
TOP VIEW



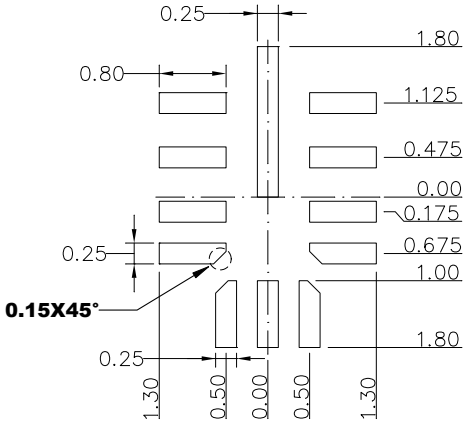
BOTTOM VIEW



SIDE VIEW



SECTION A-A

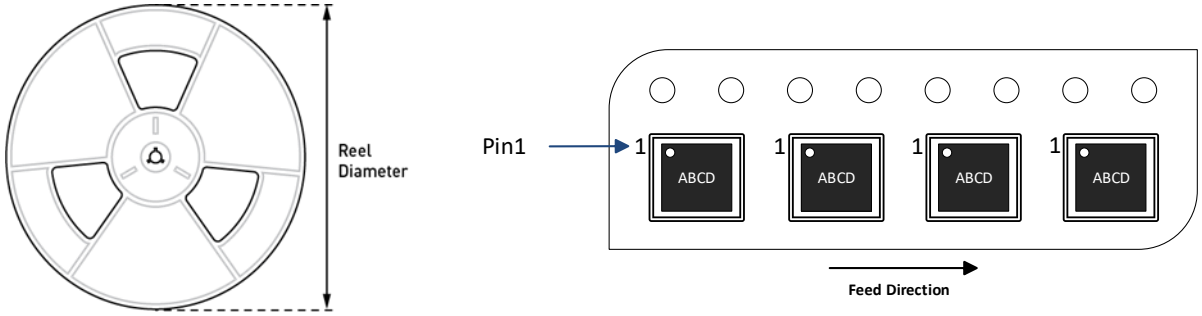


RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITIES SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube (15)	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP4321GDE-Z	QFN-12 (2mmx3mm)	5000	N/A	N/A	13in	12mm	8mm

Notes:

15) N/A means “not applicable.” Contact MPS for 500 pieces of tape and reel prototype quantities. The order code for a 500-piece partial reel is “-P”. The tape and reel dimensions are the same as the full reel.

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	1/12/2022	Initial Release	-
1.1	4/28/2023	Updated the minimum start-up V_{IN} from 3.8V to 3.9V; updated the description of θ_{JC} in note 8 and note 9	5
		Added the valley current limit maximum values (2A); updated the valley current limit minimum values from 1.1A to 1A; minor formatting udpates	7
		Updated the recommended C_{BOOT} to “22nF to 100nF”; updated “P-channel MOSFET” to “N-channel MOSFET”	30
		Updated C4 from “0.1µF” to “47nF” in Figure 11, Figure 12, Figure 13, Figure, 14, Figure 15, Figure 16, and Figure 17	35–39