MP28210

Ultra-Low 500nA I_Q, Wide Input 2V to 5.5V, 1A Step-Down Regulator with 1.2mmx1.6mm CSP Package

DESCRIPTION

The MP28210 is a monolithic power management unit containing a 1A, high-efficiency, step-down, switching converter. The nA quiescent current provides extremely high efficiency when the load current is within the µA range. With a minimum input voltage as low as 2V, the MP28210 allows the system to operate directly from the battery.

The constant-on-time (COT) control scheme provides fast transient response, high light-load efficiency, and requires minimal capacitance. The regulation can be made tight by integrating an error amplifier to correct the output voltage.

The CTRL pins control the on/off and output voltage selection functions.

Fault protection features include under-voltage lockout (UVLO), over-current protection (OCP), and thermal shutdown.

The MP28210 requires a minimal number of readily-available, standard external components, and is available in a small CSP-12 (1.2mmx1.6mm) package.

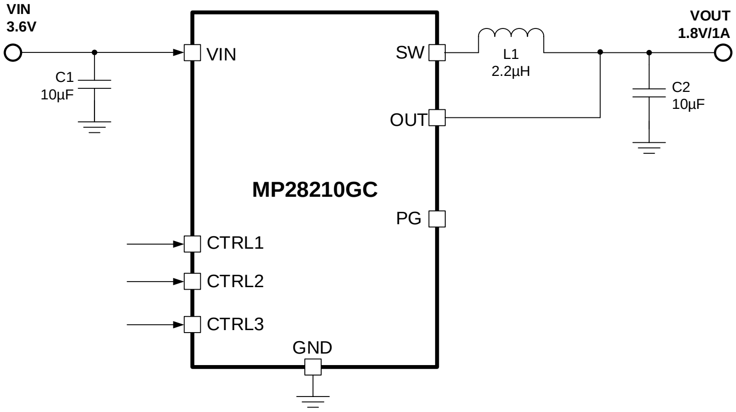
FEATURES

- Ultra-Low 500nA I_Q
- Wide 2.0V to 5.5V Operating Input Range
- 7 Selectable Output Voltages
- Up to 1A Output Current
- 1.5MHz Switching Frequency in Continuous Conduction Mode (CCM)
- 100% Duty Cycle in Dropout Mode
- 0.25Ω and 0.25Ω Internal Power MOSFET Switches
- Cycle-by-Cycle Over-Current Protection (OCP)
- Short-Circuit Protection (SCP) with Hiccup Mode
- Available in a CSP-12 (1.2mmx1.6mm) Package

APPLICATIONS

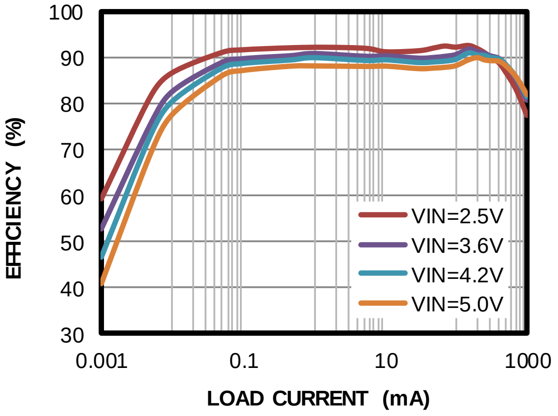
- Wearables
- Internet-of-Things (IoT)
- Portable Instruments
- Battery-Powered Devices

TYPICAL APPLICATION



Efficiency vs. Load Current

V_{OUT} = 1.8V, L1 = 2.2µH (DCR = 144mΩ)



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP28210GC	CSP-12 (1.2mmx1.6mm)	*See Below*	1

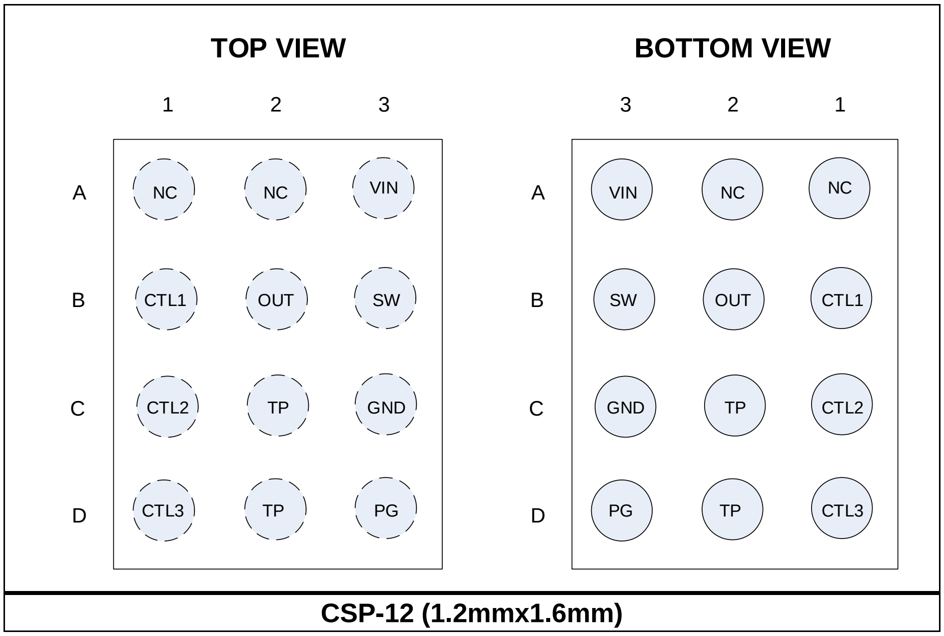
* For Tape & Reel, add suffix –Z (e.g. MP28210GC–Z).

TOP MARKING

KDY
LLL

KD: Product code of MP28210GC
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



CSP-12 (1.2mmx1.6mm)

PIN FUNCTIONS

Pin #	Name	Description
A3	VIN	**Input supply voltage for the step-down switcher.** Place a small decoupling capacitor as close to VIN and GND as possible.
B1	CTRL1	**Step-down switcher control signal (CTL means CTRL).** Dynamically adjust the step-down switcher output voltage value. Do not float the CTRL pins. When used, ensure that the CTRL voltage is not below V_{IN}. If unused, tie the CTRL pin(s) to GND. See Table 1 on page 13 to set the buck output value.
C1	CTRL2	
D1	CTRL3	
C3	GND	**Ground.**
D3	PG	**Power good indicator for the step-down switcher.** PG is an open-drain output.
B2	OUT	**Output voltage sensing for the step-down switcher.** Connect the load to OUT. Use an output capacitor to reduce the output voltage ripple.
B3	SW	**Switch output for the step-down switcher.** SW is the drain of the internal, high-side, P-channel MOSFET. Connect the inductor to SW to complete the converter.
A1	NC	**No connection.** It is recommended to connect this pin to ground.
A2	NC	**No connection.** It is recommended to connect this pin to ground.
C2	TP	**Internal test point.** Connect this pin to ground.
D2	TP	**Internal test point.** Connect this pin to ground.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) 6V
V_{SW} .... -0.3V to V_{IN} + 0.3V
………………………….. -0.3V (-5V for <10ns) to +6V (8V for <10ns or 10V for <3ns)
All other pins ....-0.3V to +6V
Continuous power dissipation (T_A = 25°C) (2) (4)
EV28210-C-00A...................................... 2.27W
Junction temperature ....150°C
Lead temperature ....260°C
Storage temperature .... -65°C to +150°C

ESD Ratings

Human body model (HBM) .... ±2000V
Charged device model (CDM) .... ±1750V

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ....2.0V to 5.5V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance

	θ_{JA}	θ_{JC}	
EV28210-C-00A (4)	55	8.2	°C/W
CSP-12 (1.2mmx1.6mm) (5)	95	30	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on MPS demon board, 2-layer 63mmx63mm PCB.
5) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 3.6V, T_J = -40°C to +125°C (6), typical value is tested at T_J = 25°C, the over-temperature limit is guaranteed by characterization, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Buck Section						
Input voltage range	V_{IN}		2.0		5.5	V
Buck under-voltage lockout rising threshold	$V_{IN\_UVLO\_R}$		1.65	1.8	1.95	V
Buck under-voltage lockout threshold hysteresis	$V_{IN\_UVLO\_H}$			150		mV
Shutdown supply current	I_{SD_25}	CTRL1/2/3 = 0V, or EN = 0		70		nA
Quiescent supply current	I_{Q_BUCK}	No load, CTRL1/2/3 = H/H/L, OUT = 1.8V, no switching		500		nA
High-side switch on resistance	R_{DSON_H}			0.25		Ω
Low-side switch on resistance	R_{DSON_L}			0.25		Ω
Switch leakage current	I_{LK_SW}	CTRL1/2/3 = 0V, V_{IN} = 5.5V, V_{SW} = 0V and 5.5V, T_J = 25°C	-100	0	+100	nA
High-side current limit	I_{LIM_H}		1.3	1.5	1.7	A
Low-side switch valley sourcing current	I_{LIMV_L}		1.1			A
Low-side switch zero-crossing current	I_{ZCD}		0	20		mA
On time	t_{ON}	V_{IN} = 3.6V, V_{OUT} = 1.8V	280	330	380	ns
Minimum on time	t_{MIN_ON}			60		ns
Minimum off time	t_{MIN_OFF}			100		ns
Maximum duty cycle	D_{MAX}		100			%
Output voltage accuracy	V_{OUT}	CTRL1/2/3 = H/H/L, T_J = 25°C, I_{OUT} = 0.1A	1.782	1.800	1.818	V
		CTRL1/2/3 = H/H/L, I_{OUT} = 0.1A, T_J = -40°C to 85°C	1.773		1.827	
Line/load regulation of buck (7)		From 2.5V to 5.5V, from 0A to 1A	-1		+1	%
Internal soft-start time	t_{SS}			0.5		ms
Discharge resistance during enable off	R_{DIS_OFF}			50		Ω
CTRL high logic	$CTRL_H$		1.2			V
CTRL low logic	$CTRL_L$				0.4	V
CTRL input current	I_{CTRL}	V_{CTRL} = 3.6V		1		nA
		V_{CTRL} = 0V		0		
		V_{EN} = 0V		0		
CTRL turn-on delay	t_D			300		µs

ELECTRICAL CHARACTERISTICS

V_{IN} = 3.6V, T_J = -40°C to +125°C (6), typical value is tested at T_J = 25°C, the over-temperature limit is guaranteed by characterization, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
CTRL pull-down resistor	R_{PD}	Not present when CTRL is high to avoid I_Q impact		2		MΩ
Power good threshold	PG	FB with respect to the regulation		90		%
Power good hysteresis	PG_{HYS}			10		%
Power good delay	PG_{TD}			75		µs
Power good sink current capability	V_{PG_LO}	Sink 1mA			0.4	V
Power good leakage current	I_{PGLK}	V_{PGBUS} = 1.8V			10	nA
Thermal shutdown (7)	T_{SD}			150		°C
Thermal hysteresis (7)	T_{SDHY}			30		°C

Notes:

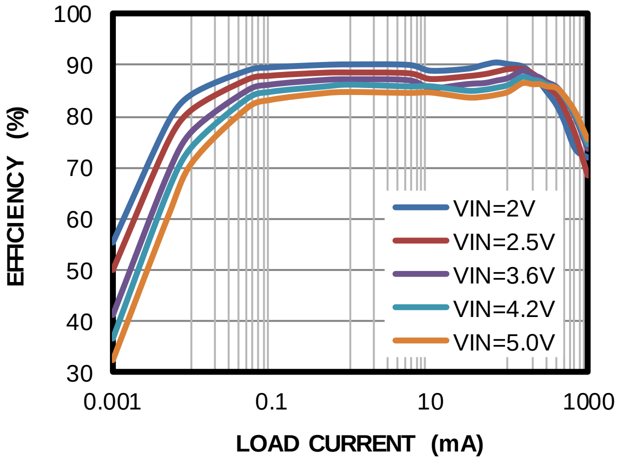
6) Not tested in production. Guaranteed by over-temperature correlation.
7) Guaranteed by engineering sample characterization.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.6V, V_{OUT} = 1.8V, L_1 = 2.2µH, C_{IN} = 10µF, C_{OUT} = 10µF, T_A = 25°C, unless otherwise noted.

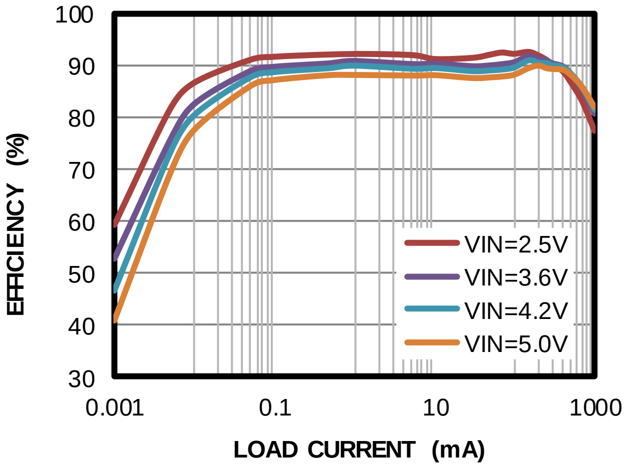
Efficiency vs. Load Current

V_{OUT} = 1.2V



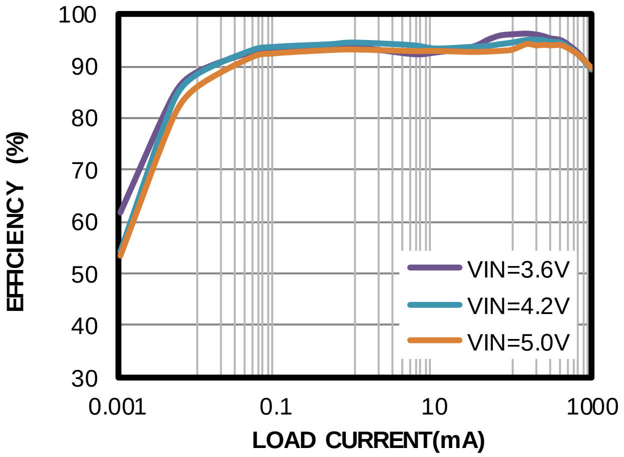
Efficiency vs. Load Current

V_{OUT} = 1.8V

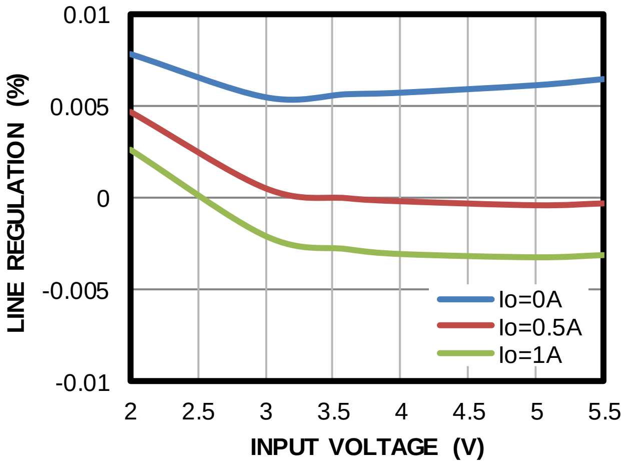


Efficiency vs. Load Current

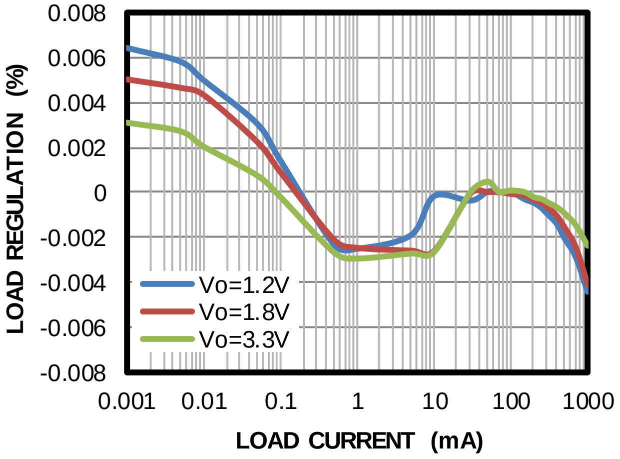
V_{OUT} = 3.3V



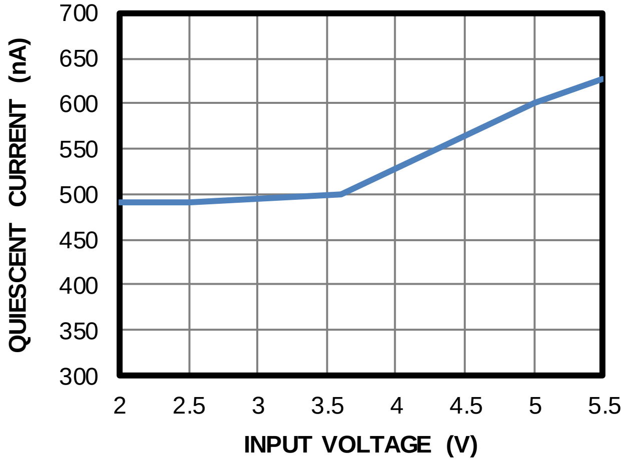
Line Regulation vs. Input Voltage



Load Regulation vs. Load Current



Buck Quiescent Current vs. Input Voltage

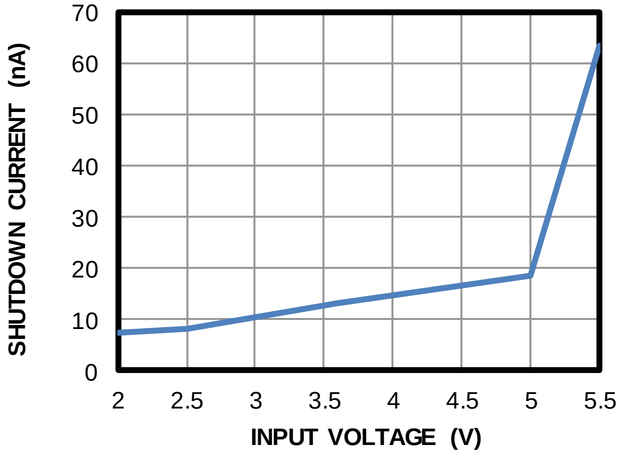


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

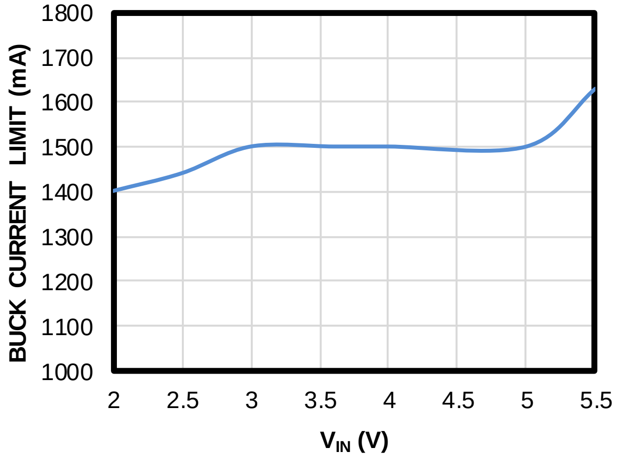
V_{IN} = 3.6V, V_{OUT} = 1.8V, L_1 = 2.2µH, C_{IN} = 10µF, C_{OUT} = 10µF, T_A = 25°C, unless otherwise noted.

Shutdown Current vs. Input Voltage

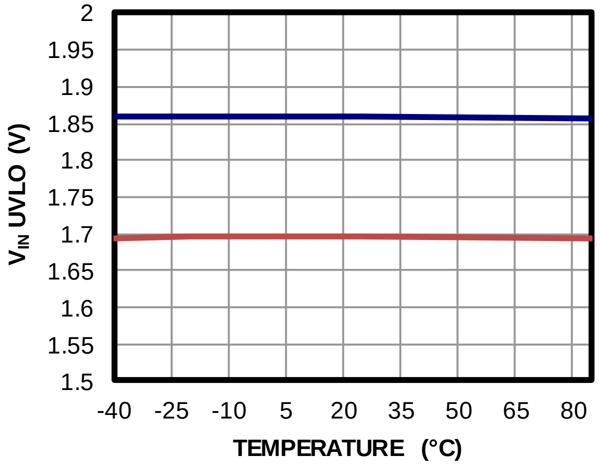
CTRL1/2/3 = 0V



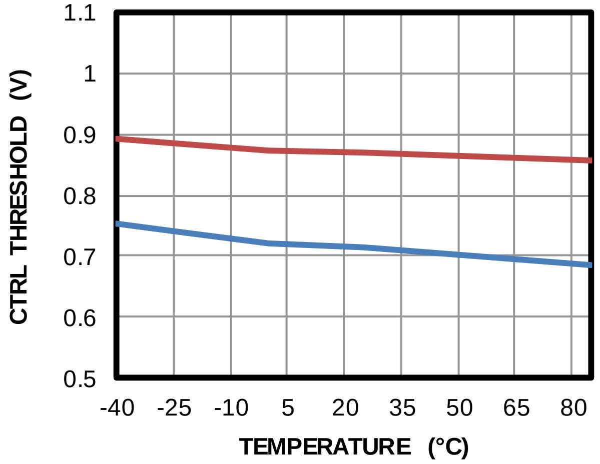
Buck Current Limit vs. V_{IN}



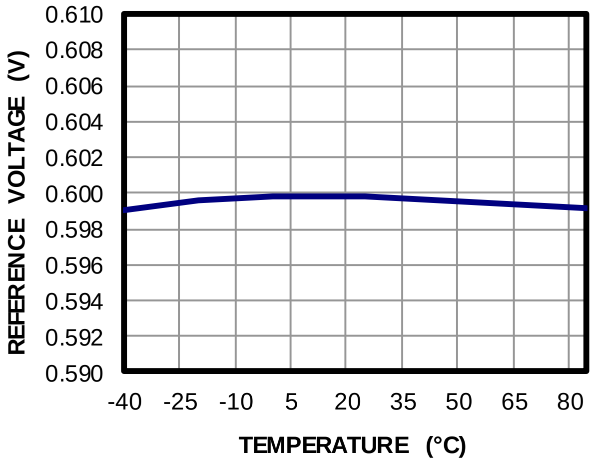
V_{IN} UVLO Rising Threshold vs. Temperature



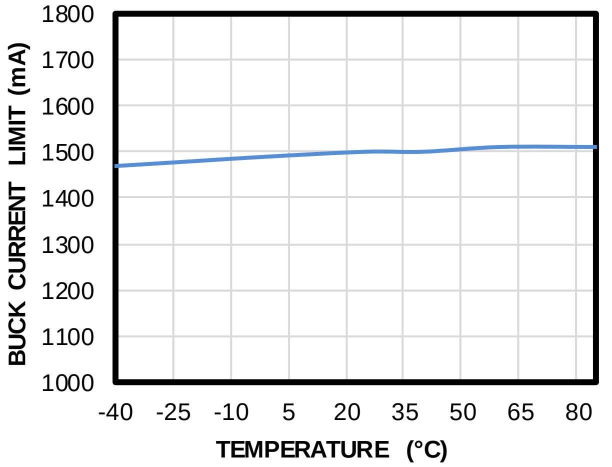
CTRL Rising and Falling Threshold vs. Temperature



Reference Voltage vs. Temperature



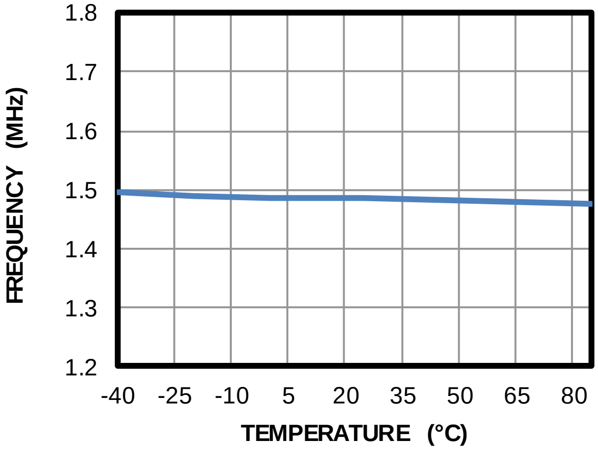
Buck Current Limit vs. Temperature



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

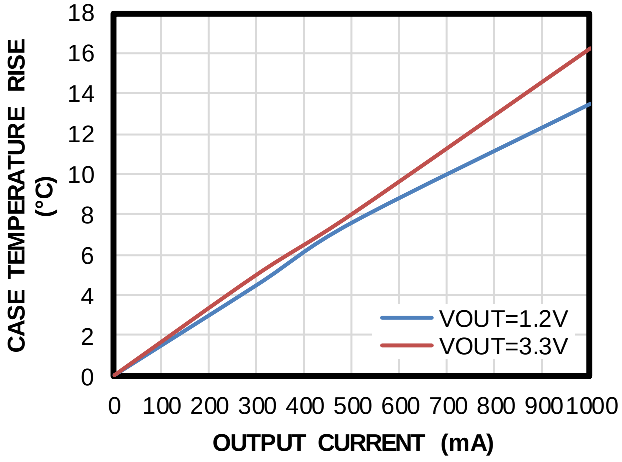
V_{IN} = 3.6V, V_{OUT} = 1.8V, L_1 = 2.2µH, C_{IN} = 10µF, C_{OUT} = 10µF, T_A = 25°C, unless otherwise noted.

Frequency vs. Temperature



T_{RISING} vs. Output Current

V_{IN} = 5V

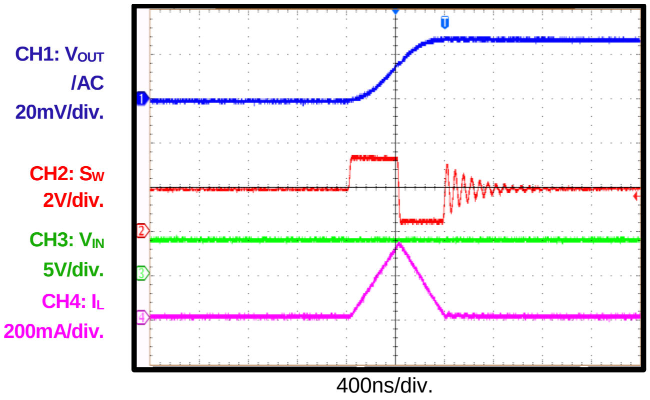


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, V_{OUT} = 1.8V, L_1 = 2.2µH, C_{IN} = 10µF, C_{OUT} = 10µF, T_A = 25°C, unless otherwise noted.

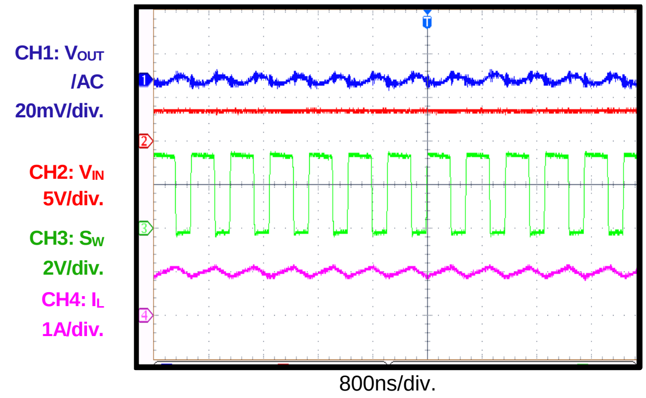
Steady State

I_{OUT} = 0A



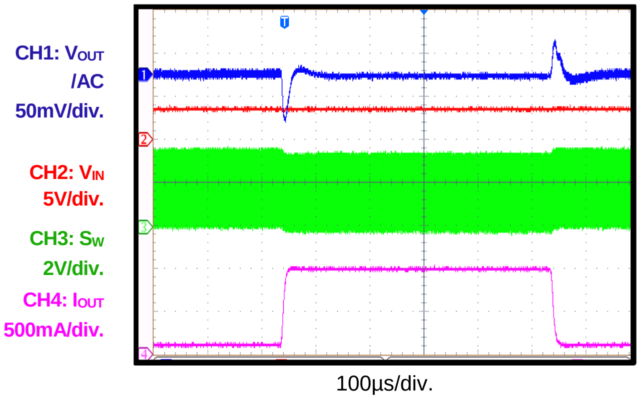
Steady State

I_{OUT} = 1A



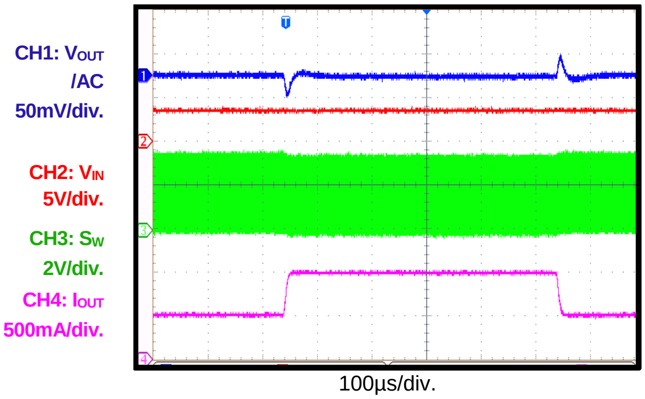
Load Transient

I_{OUT} = 100mA to 1000mA, 2.5A/µs



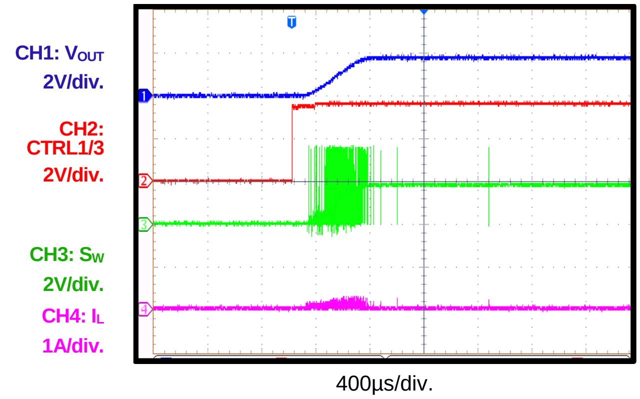
Load Transient

I_{OUT} = 500mA to 1000mA, 2.5A/µs



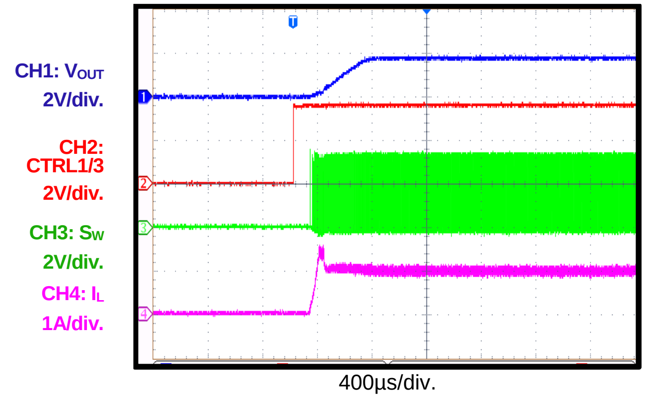
CTRL On

I_{OUT} = 0A



CTRL On

I_{OUT} = 1A

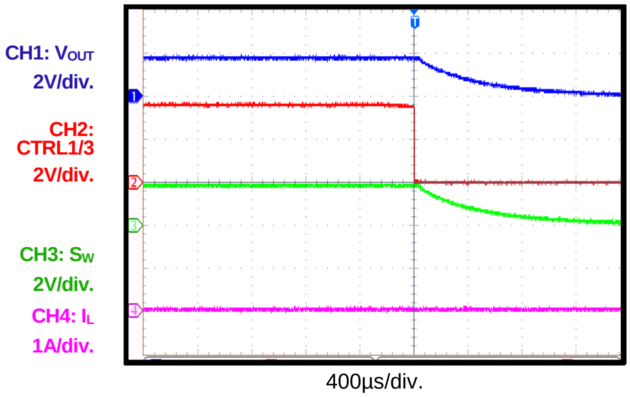


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, V_{OUT} = 1.8V, L_1 = 2.2µH, C_{IN} = 10µF, C_{OUT} = 10µF, T_A = 25°C, unless otherwise noted.

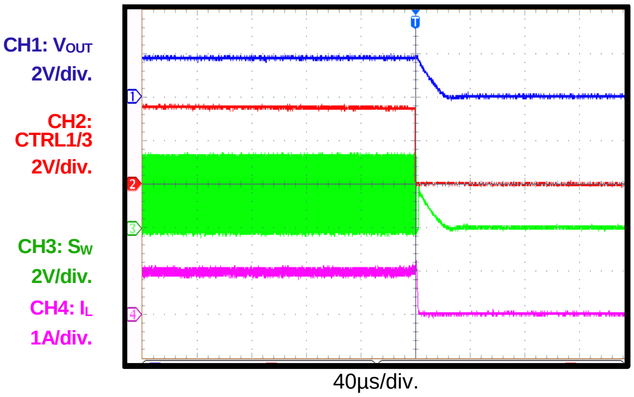
CTRL Off

I_{OUT} = 0A



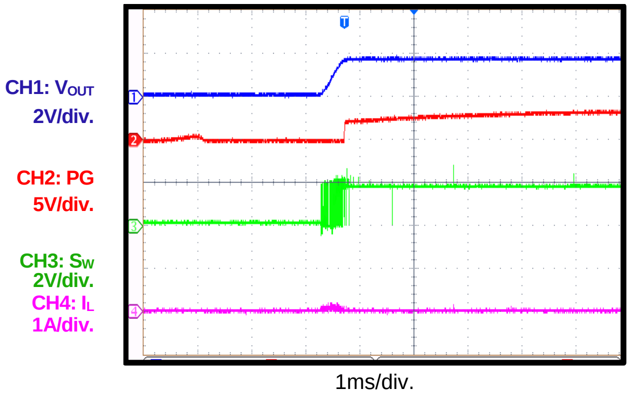
CTRL Off

I_{OUT} = 1A



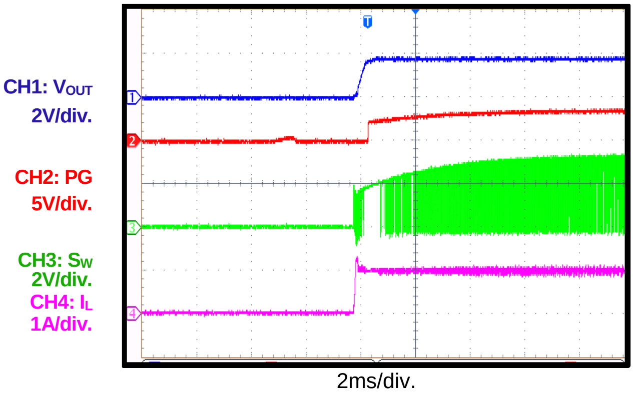
PG On

I_{OUT} = 0A



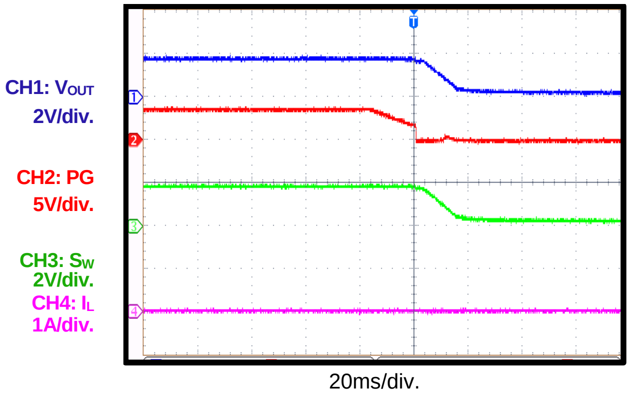
PG On

I_{OUT} = 1A



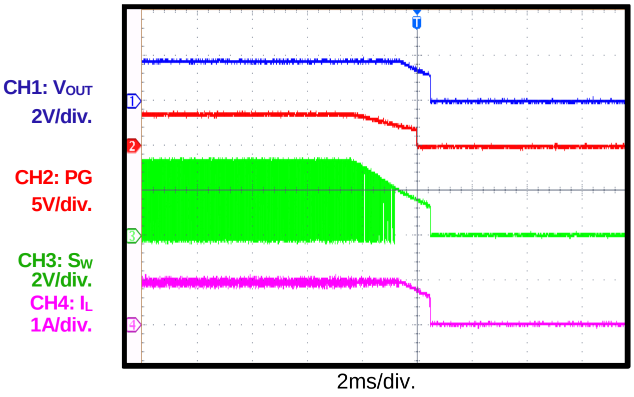
PG Off

I_{OUT} = 0A



PG Off

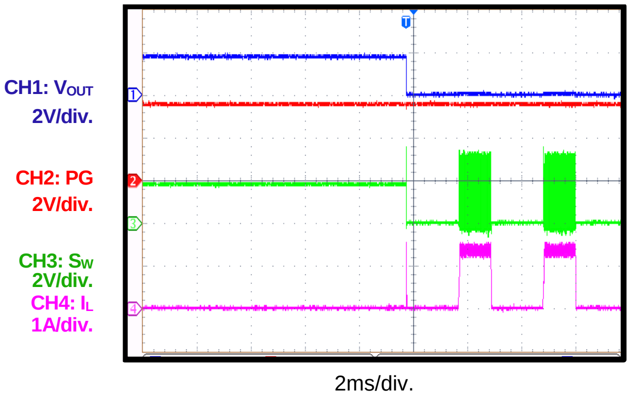
I_{OUT} = 1A



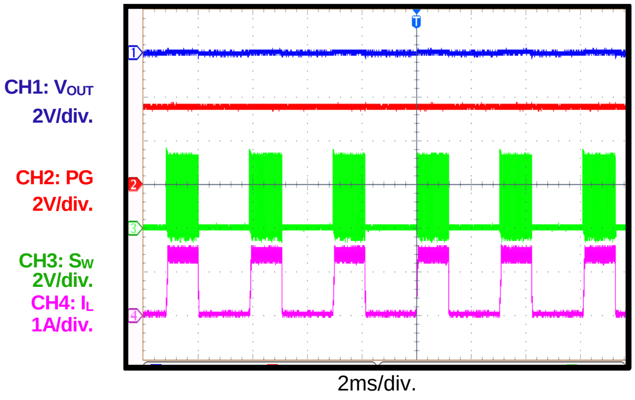
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, V_{OUT} = 1.8V, L_1 = 2.2µH, C_{IN} = 10µF, C_{OUT} = 10µF, T_A = 25°C, unless otherwise noted.

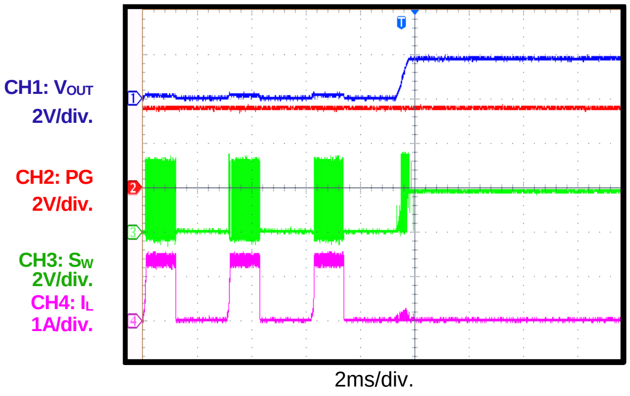
Short-Circuit Entry



Short-Circuit Steady



Short-Circuit Recovery



FUNCTIONAL BLOCK DIAGRAM

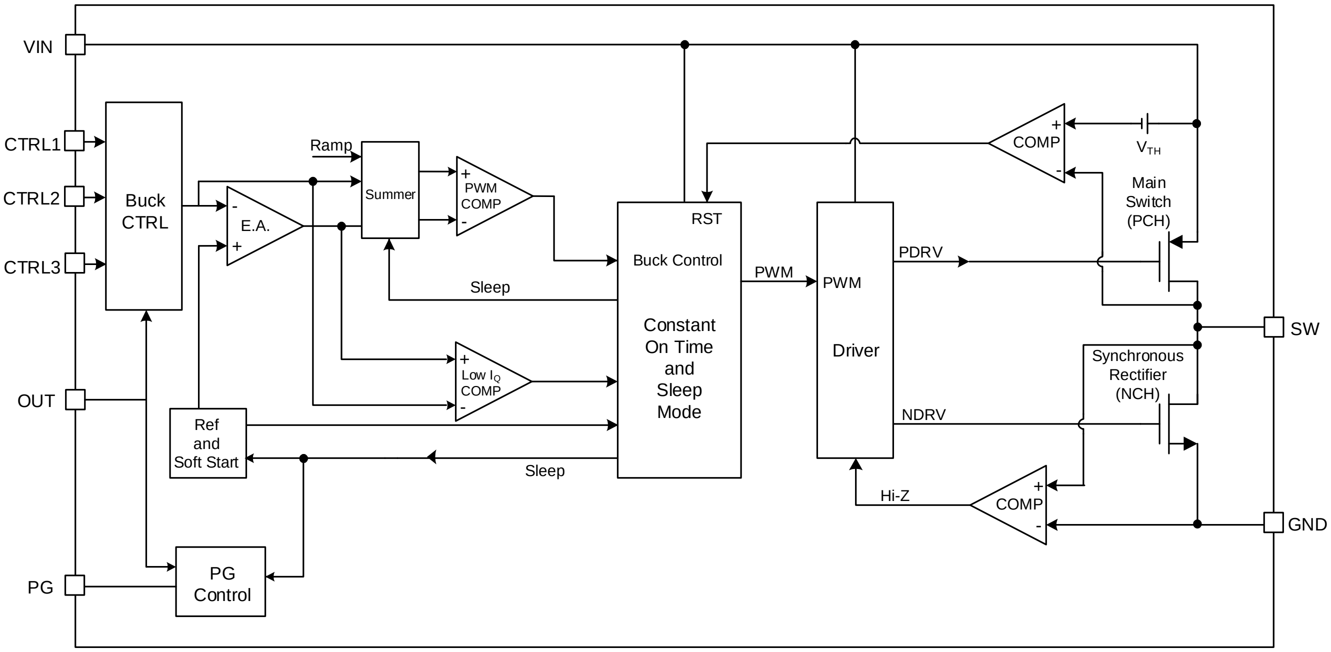


Figure 1: Functional Block Diagram

OPERATION

The MP28210 is a step-down converter with an ultra-low quiescent current and a low-dropout regulator. The step-down converter has a 500nA quiescent current, allowing the MP28210 to achieve extremely high efficiency at an ultra-low load current.

Constant-On-Time Control (COT) for the Buck

The MP28210 uses constant-on-time (COT) control to implement output voltage regulation. The one-shot on timer is controlled by the input and output voltages. At different input and output voltages, the switching frequency is fairly stable (typically 1.5MHz), which helps the system design.

With COT control, the output ripple is small, and the load transient response is fast. COT control enables the use of output and input capacitors with lower capacitance. The MP28210 automatically enters pulse-skip mode when the low-side MOSFET’s (LS-FET’s) current reaches 0A. Pulse-skip mode helps improve light-load efficiency. The COT control scheme provides a seamless transition from pulse-width modulation (PWM) mode to pulse-frequency modulation (PFM) mode, and vice versa.

Light-Load Operation

If the load current decreases and the LS-FET’s current reaches 0A, both the high-side switch (HS-FET) and LS-FET turn off. Output energy is provided by the output capacitors during this period until the output voltage drops, reaches the regulation voltage, and triggers another on pulse.

Generally, the switching frequency in PFM mode depends on the load current. The switching frequency is lower when the load current is lighter. With PFM control in light-load mode, plus the ultra-low quiescent operation current, the MP28210 can achieve the highest efficiency at an extremely light load. This helps extend the charge cycle of any battery-powered system.

When the buck works in light-load operation, it needs at least 5µs to exit light load. In light-load mode, the output voltage drops while exiting light-load mode.

Control (CTRL)

CTRL1, CTRL2, and CTRL3 control the start-up parameters and set the output voltages of the step-down regulator. When CTRL1, CTRL2, and CTRL3 are low, the MP28210’s step-down switcher is disabled. If any CTRL pin is pulled high, the switcher is enabled. The output voltage is configurable, and is set based on which CTRL pin is pulled high (see Figure 1).

Table 1: CTRL Pins vs. Output Voltages

Step-Down Switcher			
CTRL3	**CTRL2**	**CTRL1**	**OUT**
0	0	0	Disabled
0	0	1	1.2V
0	1	0	1.5V
0	1	1	1.8V
1	0	0	2.5V
1	0	1	2.8V
1	1	0	3.0V
1	1	1	3.3V

The output voltage can be configured during normal operation, and supports dynamic output voltage scaling. Do not float the CTRL pins. Any used CTRL voltage cannot be below V_{IN}, and any unused CTRL pin must be tied to GND.

Soft Start (SS)

When the converter is enabled, the internal reference is powered up. After a certain delay time, the device enters soft start (SS). The step-down switcher output voltage ramps up to the regulation voltage in about 0.5ms.

Power Good (PG) Indicators for the Buck

The MP28210 has an open-drain output power good (PG) indicator with a maximum $R_{DS(ON)}$ below 400Ω. PG requires a 100kΩ to 500kΩ external pull-up resistor for power good indication. This resistor can be pulled up to VIN, or tied to a CTRL pin if the CTRL voltages do not need to be adjusted dynamically.

The PG comparator is active when the device is enabled. The comparator is driven to a high impedance if the output voltage trips the PG threshold (typically 90% of the regulation voltage). It is pulled low if the output voltage falls below the PG hysteresis threshold (typically 80% of the regulation voltage).

The output is also pulled low if the input voltage is lost or the part is disabled.

Output Discharge Function

Once the step-down regulator is disabled, it utilizes the output discharge function. This feature prevents residual charge voltages on the capacitors, which may impact a proper system start-up. When the input voltage is high and the related converters are disabled, the output discharge is active.

100% Duty Cycle Mode

When the input voltage drops below the regulation output voltage, the output voltage drops and the on time increases. Further reducing the input voltage drives the MP28210 into 100% duty cycle mode. The HS-FET is always on, and the output voltage is determined by load current multiplied by $R_{DS(ON)}$, which is determined by the HS-FET and inductor.

Current Limit

The MP28210 has an internal current limit for the step-down converter.

The HS-FET current is monitored cycle by cycle and compared to the current-limit threshold. Once the current-limit comparator is triggered, the HS-FET turns off and the LS-FET turns on, reducing the inductor current. The HS-FET cannot turn on until the LS-FET current drops below the low-side current limit.

Short Circuit and Recovery

If the buck converter's output voltage is shorted to GND, the current limit is triggered. If the current limit is triggered every cycle for 200µs, the MP28210's buck converter enters hiccup mode.

The short-circuit condition can also be triggered if the output voltage drops below 50% of the regulation output voltage as the device reaches the current limit. The buck converter disables the output power stage, discharges the output voltage, then attempts to recover after hiccup mode. If the short-circuit condition remains, the MP28210 repeats this operation until the short circuit is removed and the output voltage rises back to its regulation level.

Thermal Shutdown Circuit and Recovery

If thermal shutdown signal is triggered, the MP28210 turns off immediately. Once the temperature returns to below the thermal hysteresis threshold, the device restarts and resumes normal operation.

APPLICATION INFORMATION

Inductor Selection

Most applications work best with a 1µH to 2.2µH inductor. Select an inductor with a DC resistance below 200mΩ to optimize efficiency.

High-frequency, switch-mode power supplies with a magnetic device introduce strong electronic magnetic inference (EMI) in the system. Unshielded power inductors should be avoided since they have poor magnetic shielding. Metal alloy or multiplayer chip power shield inductors are recommended in application since they can decrease influence effectively. Table 2 lists recommended inductors.

Table 2: Recommended Inductors

Inductance	Manufacturer P/N	Package	Manufacturer
2.2µH	DFE201612P-2R2M	2016	Tokyo
2.2µH	74479775222A	2012	Wurth

For most designs, the inductance value can be calculated with Equation (1):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \qquad (1)$$

Where ΔI_L is the inductor ripple current. Choose the inductor current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (2):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \qquad (2)$$

Input Capacitor Selection

The input capacitor reduces the surge current drawn from the input, as well as the switching noise from the device. Select an input capacitor with a switching frequency impedance below the input source impedance to prevent a high-frequency switching current from flowing to the input source. It is recommended to use low-ESR ceramic capacitors with X5R or X7R dielectrics due to their small temperature coefficients. For most applications, a 10µF capacitor is sufficient.

The input capacitor requires an adequate ripple current rating since it absorbs the input switching current.

Estimate the RMS current in the input capacitor with Equation (3):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \qquad (3)$$

The worst-case scenario occurs when $V_{IN} = 2V_{OUT}$, calculated with Equation (4):

$$I_{C1} = \frac{I_{LOAD}}{2} \qquad (4)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality, 0.1µF ceramic capacitor as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated with Equation (5):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \qquad (5)$$

Output Capacitor Selection

The output capacitor limits the output voltage ripple and ensures a stable regulation loop. Select an output capacitor with low impedance at the switching frequency. For most applications, a 10µF capacitor is sufficient. Estimate the output voltage ripple with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C2}\right)$$

(6)

Where L_1 is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes most of the output voltage ripple.

For simplification, the output voltage ripple can be estimated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^{2} \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \qquad (7)$$

The characteristics of the output capacitor also affect the stability of the regulation system.

PCB Layout Guidelines

Designing an efficient PCB layout for the switching power supply, especially the high-switching frequency converter, is critical for stable operation. Without careful placement, the regulator could exhibit poor line or load regulation and stability issues. For the best results, refer to Figure 2 and follow the guidelines below:

1. Place the input capacitor as close to the IC pins as possible. This helps the high-speed step-down regulator provide clean voltage control for the chip.
2. Place C_{IN} close to VIN and GND to absorb noise.

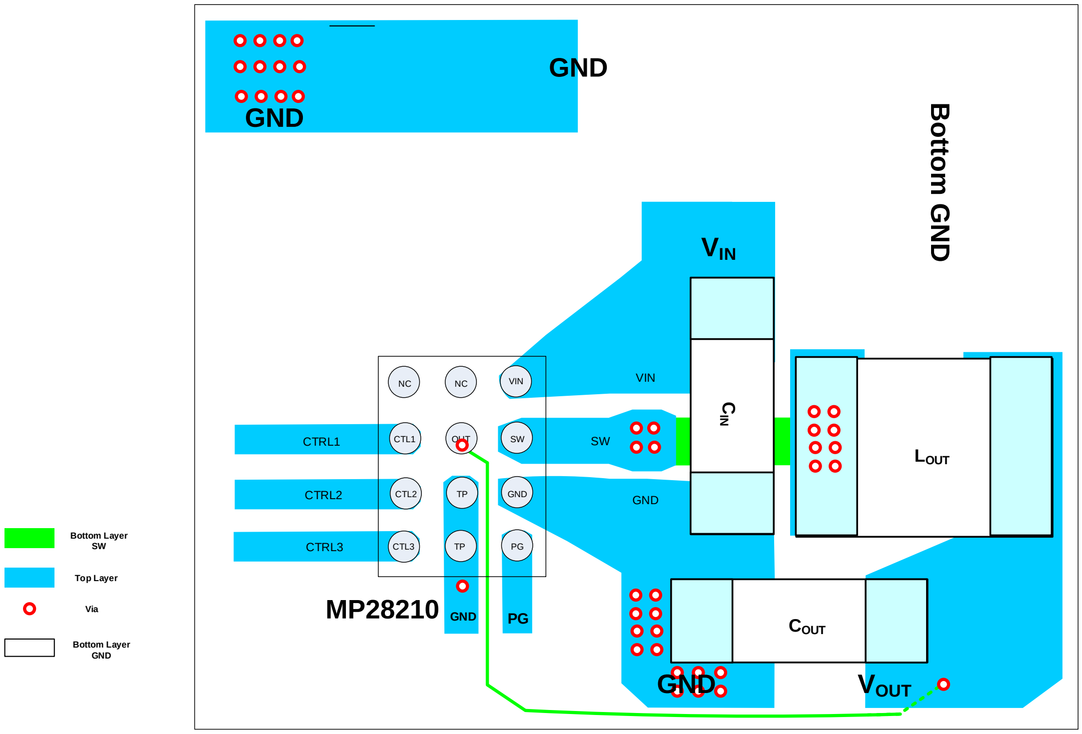


Figure 2: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

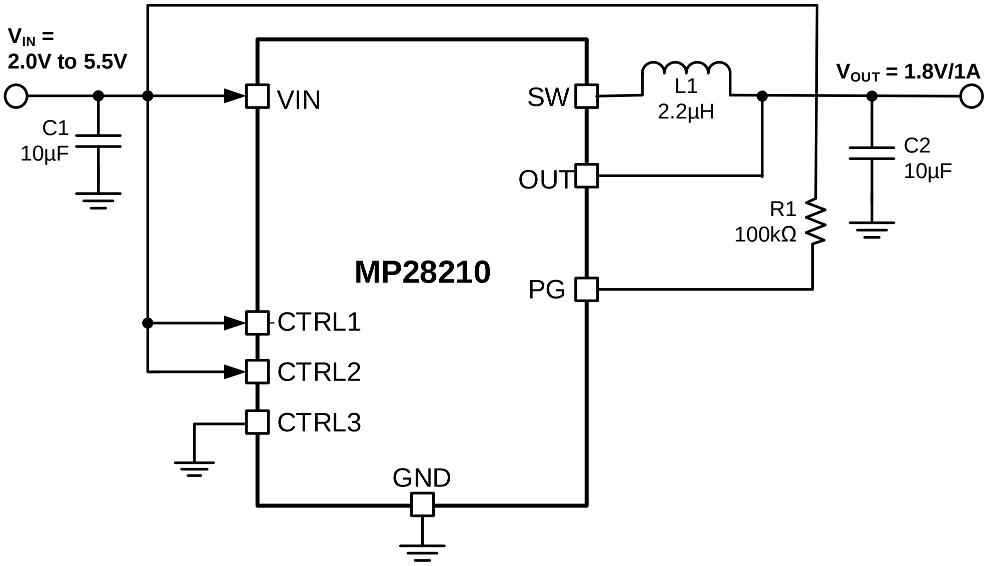


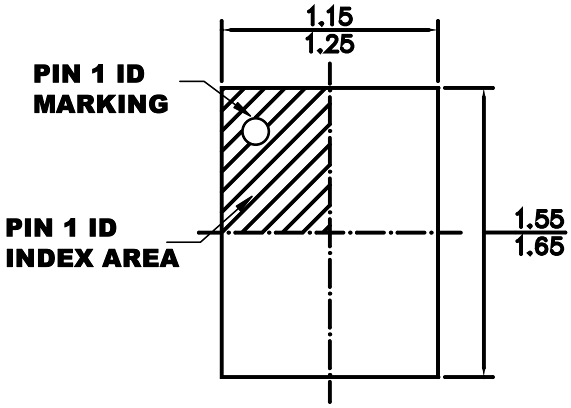
Figure 3: Typical Application Circuit for MP28210GC (8)

Note:

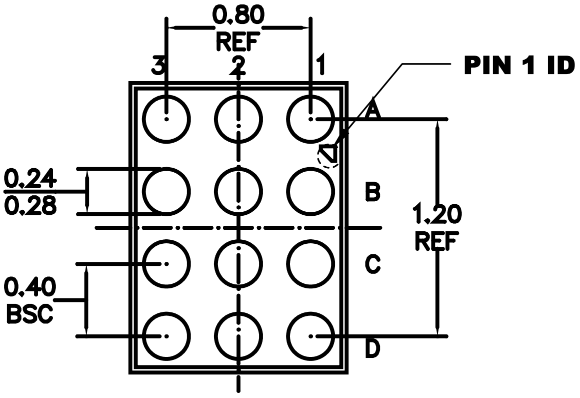
8) V_{IN} must exceed the V_{IN} under-voltage lockout (UVLO) threshold.

PACKAGE INFORMATION

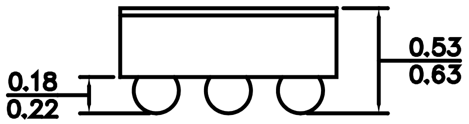
CSP-12 (1.2mmx1.6mm)



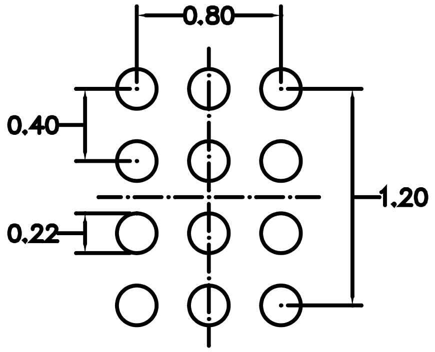
TOP VIEW



BOTTOM VIEW



SIDE VIEW

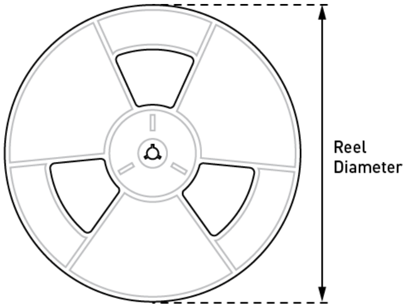


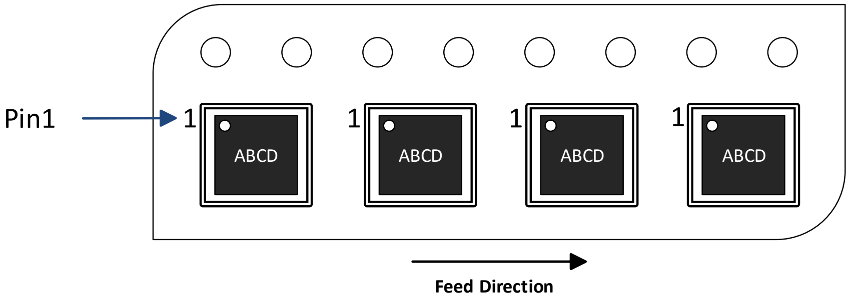
RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) BALL COPLANARITY SHALL BE 0.05 MILLIMETER MAX.
3) JEDEC REFERENCE IS MO-211.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION





Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP28210GC–Z	CSP-12 (1.2mmx1.6mm)	3000	N/A	7in	8mm	4mm

Revision History

Revision #	Revision Date	Description	Pages Updated
1.0	7/17/2020	Initial Release	-