UNIVERSAL FLASH STORAGE

(UFS 3.1)

UFS64G-TX17-GA3A-DK
UFS128-TX17-GA3A-DK

Datasheet
v1.1

Kingston Solutions Inc.

CONTENTS

Product Features：

<Common>

- Packaged NAND flash memory with UFS 3.1 interface
- Compliant with UFS Specification Ver.3.1
- Support for High Speed Gear Rates : Up to HS-GEAR4 (2 lane)
  - PWM : supports to Gear 1
  - HS-BURST: supports to Gear 1~4
- UFS layering ：
  - -UFS Command Set Layer (UCS)
  - -UFS Transport Protocol Layer (UTP)
  - -UFS Interconnect Layer (UIC)
- Temperature ：
  - Operation : -25℃ ~ 85℃ ， Storage : -40℃ ~ 85℃
- Operating voltage ：
  - VCCQ=1.14~1.26V, 1.2V (Typ) ， VCC = 2.4~2.7V, 2.5V (Typ)
- Error free memory access
  - Internal error correction code (ECC) to protect data communication
  - Internal enhanced data management algorithm
  - Solid protection of sudden power failure safe-update operations for data content
- Security
  - Discard
  - Replay Protected Memory Block (RPMB)
  - Support secure bad block erase commands
  - Enhanced write Protection with permanent and partial protection options
- Performance
  - High Priority Interrupt
  - Background Operation
  - Command Queuing
  - Data tag
  - Context ID
  - Cache Operation
  - Write Booster
  - Host Performance Booster
- Reliability
  - Dynamic Capacity
  - Real Time Clock
  - Production State Awareness (PSA)
- Quality
  - RoHS compliant (for detailed RoHS declaration, please contact your KSI representative.)
- Similar functional features as eMMC.
  - Multiple logical units with configurable characteristics
  - Reliable write operation
  - Task management
  - Device Health (EOL)
  - Field Firmware Update (FFU)

1 Introduction

Kingston UFS products follow the JEDEC UFS 3.1 standard. It is an ideal universal storage solution for many electronic devices, including smartphones, camera, Tablets, Electronic toys , Smart home ,Wearable ,Automotive sensor ,Artificial intelligence robotics , Virtual reality (VR), Unmanned aerial vehicle that require mass storage. UFS encloses the 3D NAND and UFS controller inside as one JEDEC standard package, providing a standard interface to the host. The UFS controller directly manages NAND flash, including ECC, wear-leveling, IOPS optimization and read sensing.

2 Specification

2.1 Device Summary

Product Part Number	NAND Density	Package	Operating voltage
UFS64G-TX17-GA3A-DK	64GB	FBGA153	V_{CC}= 2.4~2.7 V V_{CCQ}= 1.14V~1.26V
UFS128-TX17-GA3A-DK	128GB		

2.2 System Performance

Products	Write Booster value	
	Sequential Read (MB/s)	Sequential Write (MB/s)
UFS64G-TX17-GA3A-DK	1100	390
UFS128-TX17-GA3A-DK	1400	780

Note 1: For performance number under other test conditions, please contact KSI representatives.
Note 2: Performance numbers might be subject to change without notice.
Note 3: Values given for an 2 lane bus width, a clock frequency of 26MHz(HS-Gear 4)

Products	Typical value	
	Sequential Read (MB/s)	Sequential Write (MB/s)
UFS64G-TX17-GA3A-DK	1100	80
UFS128-TX17-GA3A-DK	1400	170

Note 1: For performance number under other test conditions, please contact KSI representatives.
Note 2: Performance numbers might be subject to change without notice.
Note 3: Values given for an 2 lane bus width, a clock frequency of 26MHz(HS-Gear 4)

2.3 Power Consumption

Products	Read(mA)		Write(mA)		Idle(uA)		Sleep(uA)		Deep Sleep(uA)	
	$V_{CCQ(1.2V)}$	$V_{CC(2.5V)}$	$V_{CCQ(1.2V)}$	$V_{CC(2.5V)}$	$V_{CCQ(1.2V)}$	$V_{CC(2.5V)}$	$V_{CCQ(1.2V)}$	$V_{CC(2.5V)}$	$V_{CCQ(1.2V)}$	$V_{CC(2.5V)}$
UFS64G-TX17-GA3A-DK	600	270	420	150	1100	50	650	50(0)	350	50(0)
UFS128-TX17-GA3A-DK	640	300	470	250	1100	100	650	100	350	100

Note 1: Values given for an 2 lane bus width, a clock frequency of 26MHz(HS-Gear 4),100ms RMS current value, V_{CC}= 2.5V±5%, V_{CCQ}=1.2V±5%, Ta = 25℃
Note 2: Idle = Hibernate State, current is measured at Vcc=2.5V±5%, 2 lane bus width without clock frequency.
Note 3: Sleep = SSU(Sleep) + Hibernate. When in sleep state, VCC could be turned off and value will be 0.
Note 4: Deep Sleep = Power off for UniPro and M-PHY. When in deep sleep state, VCC could be turned off and value will be 0..
Note 5: Current numbers might be subject to change without notice.

2.4 Capacity According To Partition

Capacity	Boot partition 1	Boot partition 2	RPMB
64 GB	4MB	4MB	4MB
128 GB	4MB	4MB	4MB

2.5 User Density

Total user density depends on device type.
For example, 52MB in the SLC mode requires 156 MB in TLC.

Device	User Density
64GB	640021856256 Bytes
128GB	128043712512 Bytes

3 Mechanical Specification

3.1 Ball Definition

Table 3-1 FBGA153 Ball information

Name	Type	Description
VCC	Supply	Supply voltage for the memory devices
VCCQ	Supply	Supply voltage used typically for the memory controller and optionally for the PHY interface, the memory IO, and any other internal very low voltage block
VDDiQ	Input	Input terminal to provided bypass capacitor for VCCQ internal regulator
VDDi	Input	Input terminal to provide bypass capacitor for VCC internal regulator
VSS	Supply	Ground
RST_n	Input	Input hardware reset signal. This is an active low signal
REF_CLK	Input	Input reference clock. When not active, this signal should be pull-down or driven low by the host SoC.
Differential input signals into UFS device from the host		
DIN_t or DIN0_t DIN_c or DIN0_c	Input	Downstream data lane 0 DIN_t is the positive node of the differential signal.
DIN1_t, DIN1_c	Input	Downstream data lane 1
Differential output signals from the UFS device to the host		
DOUT_t or DOUT0_t DOUT_c or DOUT0_c	Output	Downstream data lane 0 DOUT_t is the positive node of the differential signal.
DOUT1_c, DOUT1_c	Output	Upstream data lane 1
NC		No connect. Need Keep floating.
VSF		Vendor Specific Function. Need Keep floating.
RFU		No connect. Reserved for future use. Need Keep floating.

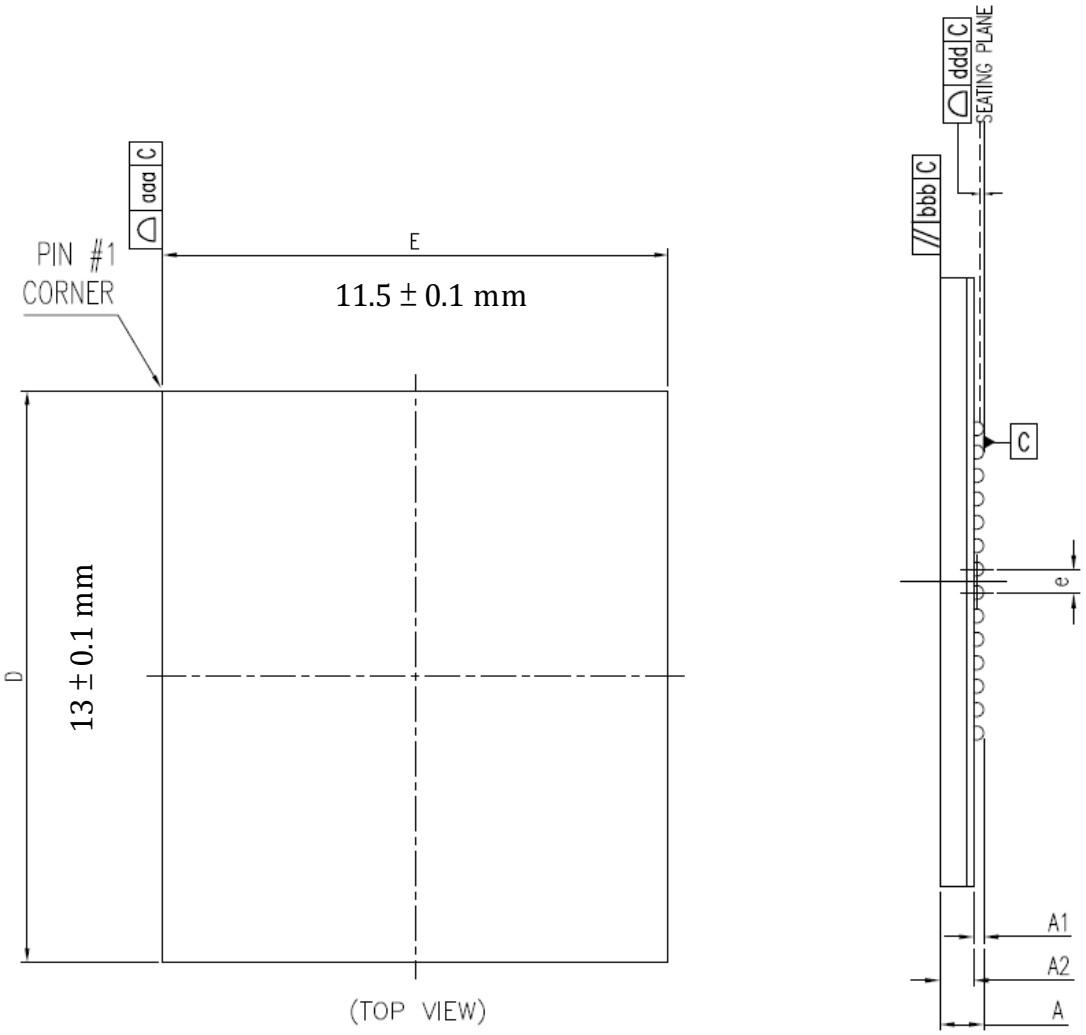
Figure 3-1 Ball assignment for FBGA 153L

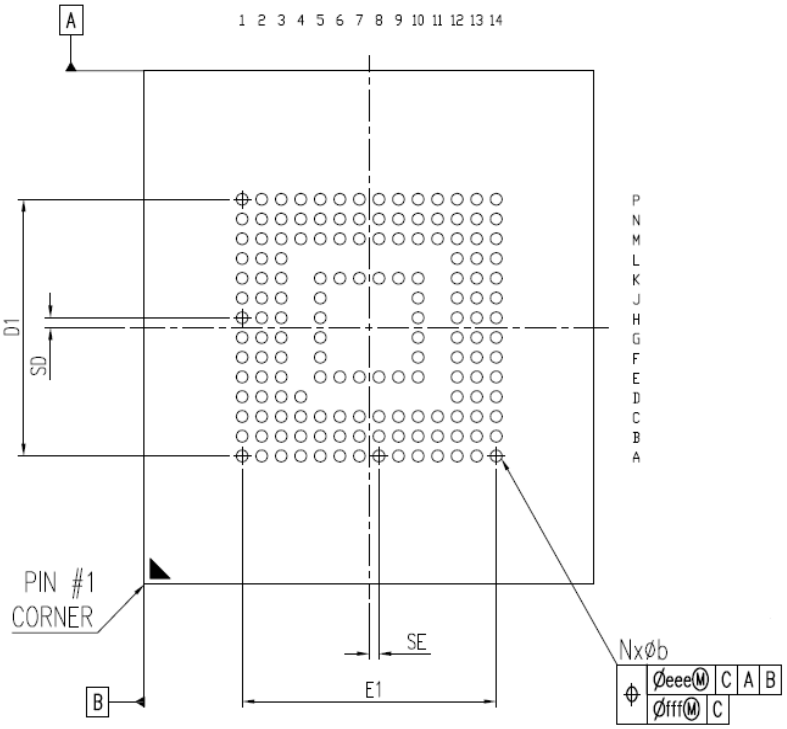
	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	NC	NC	VDDiQ	VCCQ	VCCQ	NC	NC	NC	VDDi	NC	NC	NC	NC	NC
B	NC	VSS	RFU	VCCQ	VCCQ	NC	NC	VCC	VCC	NC	VSS	VSS	RFU	NC
C	VSS	VSS	VSS	VCCQ	VCCQ	NC	NC	VCC	VCC	RFU	VSS	VSS	RFU	RFU
D	DIN1_t	DIN1_c	VSS	NC(Index)								VSS	VSS	VSS
E	VSS	VSS	VSS		VCCQ	VSF1	VSF2	VCC	VSF3	VSF4		VSS	RFU	RFU
F	DIN0_t	DIN0_c	VSS		VCCQ					VSF5		VSS	VSS	VSS
G	VSS	VSS	VSS		VSF6					VSS		VSS	RFU	RFU
H	REF_CLK	RST_n	VSS		VSS					VSS		VSS	VSS	VSS
J	VSS	VSS	VSS		VSS					VSF7		VSS	RFU	RFU
K	DOUT0_c	DOUT0_t	VSS		VSS	NC	NC	VCC	NC	VSF8		VSS	VSS	VSS
L	VSS	VSS	VSS									VSS	RFU	RFU
M	DOUT1_c	DOUT1_t	VSS	VSS	VSS	RFU	RFU	NC	NC	RFU	NC	VSS	VSS	VSS
N	NC	VSS	VSS	VSS	VSS	RFU	RFU	VCC	VCC	RFU	VSS	VSS	RFU	NC
P	NC	NC	RFU	VSS	VSS	RFU	RFU	VCC	VCC	VSF9	VSS	VSS	NC	NC

3.2 Package Dimension

11.5mm*13mm*0.8mm Max. : For 64GB

11.5mm*13mm*1.0mm Max. : For 128GB





(BOTTOM VIEW)

For 64GB

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.62	0.73	**0.80**	0.024	0.029	**0.031**
A1	**0.15**	0.21	0.26	**0.006**	0.008	0.010
A2	0.46	0.52	**0.60**	0.018	0.020	**0.024**
b	0.25	0.30	0.35	0.010	0.012	0.014
D	12.90	13.00	13.10	0.508	0.512	0.516
E	11.40	11.50	11.60	0.449	0.453	0.457
e	0.50 BSC.			0.020 BSC.		
JEDEC	MO-276(REF.)/MM					
aaa	0.15					
ccc	0.20					
ddd	0.08					
eee	0.15					
fff	0.05					

N	SE (mm)	SD (mm)	E1 (mm)	D1 (mm)
153L	0.25 BSC.	0.25 BSC.	6.50 BSC.	6.50 BSC.

For 128GB

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.81	0.93	**1.00**	0.032	0.037	**0.039**
A1	**0.15**	0.21	0.26	**0.006**	0.008	0.010
A2	0.65	0.72	**0.80**	0.026	0.028	**0.031**
b	0.25	0.30	0.35	0.010	0.012	0.014
D	12.90	13.00	13.10	0.508	0.512	0.516
E	11.40	11.50	11.60	0.449	0.453	0.457
e	0.50 BSC.			0.020 BSC.		
JEDEC	MO-276(REF.)/MM					
aaa	0.15					
ccc	0.20					
ddd	0.08					
eee	0.15					
fff	0.05					

N	SE (mm)	SD (mm)	E1 (mm)	D1 (mm)
153L	0.25 BSC.	0.25 BSC.	6.50 BSC.	6.50 BSC.

3.3 UFS Block Diagram

Figure 3.2 represents a conceptual drawing of UFS device. Utilization of internal regulators and Connection of those to different parts of the sub-system may differ per implementation.

Figure 3-2 Device Block diagram

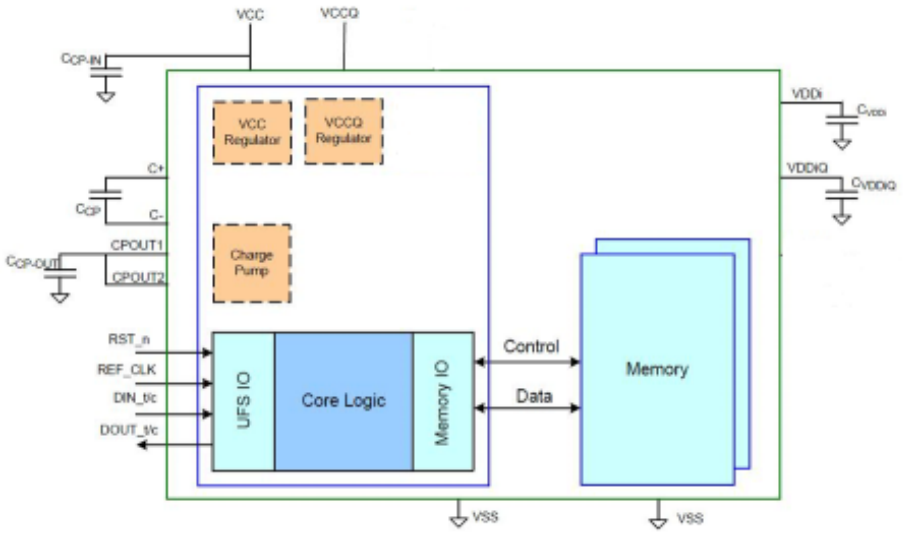


Table 3-2 - Power Supply Parameter

Parameter	Symbol	Min	Max	Unit	Notes
VCC DC operating range	VCC	2.4	2.7	V	3
VCCQ DC operating range	VCCQ	1.14	1.26	V	1,3
Supply Voltage power up timing for 3.3 V	tPRUH		35	ms	2
Supply Voltage power up timing for 2.5 V	tPRUH		35	ms	2
Supply Voltage power up timing for 1.2 V	tPRUV		20	Ms	2
VCC internal regulator capacitor	C_{VDDi}	1		µF	
VCCQ internal regulator capacitor	C_{VDDiQ}	1		uF	

NOTE 1 See [JESD8-12A]

NOTE 2 Power up timing starts when the supply voltage crosses 300 mV and ends when it reaches the minimum operating value

NOTE 3 Depending on the vendor, valid power configuration may be defined in each UFS device vendor's data sheet. Refer to the vendor datasheet for the detail

3.4 Reference Clock

The M-PHY specification defines the reference clock optional for the State Machine Type I [MIPI M-PHY].As the PWM signaling is self-clocked the reference clock is not required for the data latching. Therefore, UFS devices shall be able to operate without reference clock in LS-MODE (LINE-CFG, SLEEP and PWM-BURST).

Still existence of the reference clock may be utilized to enable lower BER and faster HS-MODE PLL/DLL locking. Thus a UFS device shall implement a square wave single ended reference clock input and it requires the presence of a reference clock with the characteristics described in this section when operating in HS-MODE(STALL and HS-BURST). In order to avoid potential race conditions, it is recommended that such reference clock is already present when requesting a power mode change into Fast_Mode or FastAuto_Mode.

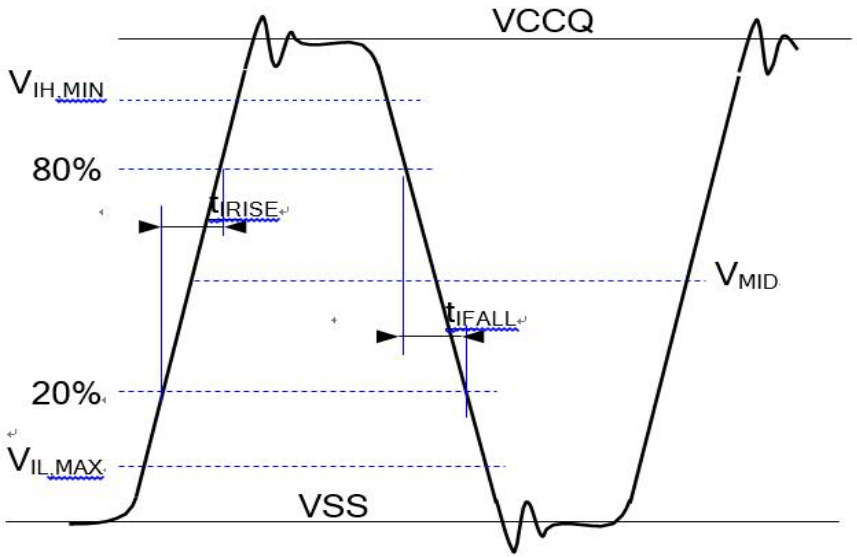
Table 3-3 – Reference Clock

Parameter	Symbol	Nominal		Unit	Notes
Frequency	fref	19.2 / 26 / 38.4		MHz	1
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Notes**
Frequency Error	fERROR	-150	+150	ppm	
Input High Voltage	VIH	0.65 * VCCQ		V	2
Input Low Voltage	VIL		0.35 * VCCQ	V	2
Input Clock Rise Time	t_{IRISE}		2	ns	3
Input Clock Fall Time	t_{IFALL}		2	ns	3
Duty Cycle	t_{DC}	45	55	%	4
Phase Noise	N		-66	dBc	5
Noise Floor Density	$N_{density}$		-140	dBc/H	6
Input Impedance	RL_{RX}	100		kΩ	7
	CL_{RX}		5	pF	

NOTE 1 HS-BURST rates A and B are achieved with integer multipliers of f_{ref}.
NOTE 2 Figure 3-3 shows the input levels $V_{IL,MAX}$ to $V_{IH,MIN}$.
NOTE 3 Clock rise time and clock fall time shall be measured from 20% to 80% of the window defined by $V_{IL,MAX}$ to $V_{IH,MIN}$, see Figure 3-3.
NOTE 4 Clock duty cycle shall be measured at the crossings of the REF_CLK signal with the midpoint V_{MID}, defined as: $V_{MID} = (V_{IL,MAX} + V_{IH,MIN}) / 2$, see Figure 3-3.
NOTE 5 Integrated single side band phase noise from 50kHZ to 10MHz. This parameter refers to the random jitter only.
NOTE 6 White noise floor. This parameter refers to the random jitter only.
NOTE 7 RL_{RX} and CL_{RX} include Rx package and Rx input impedance.

3.4.1 Reference Clock

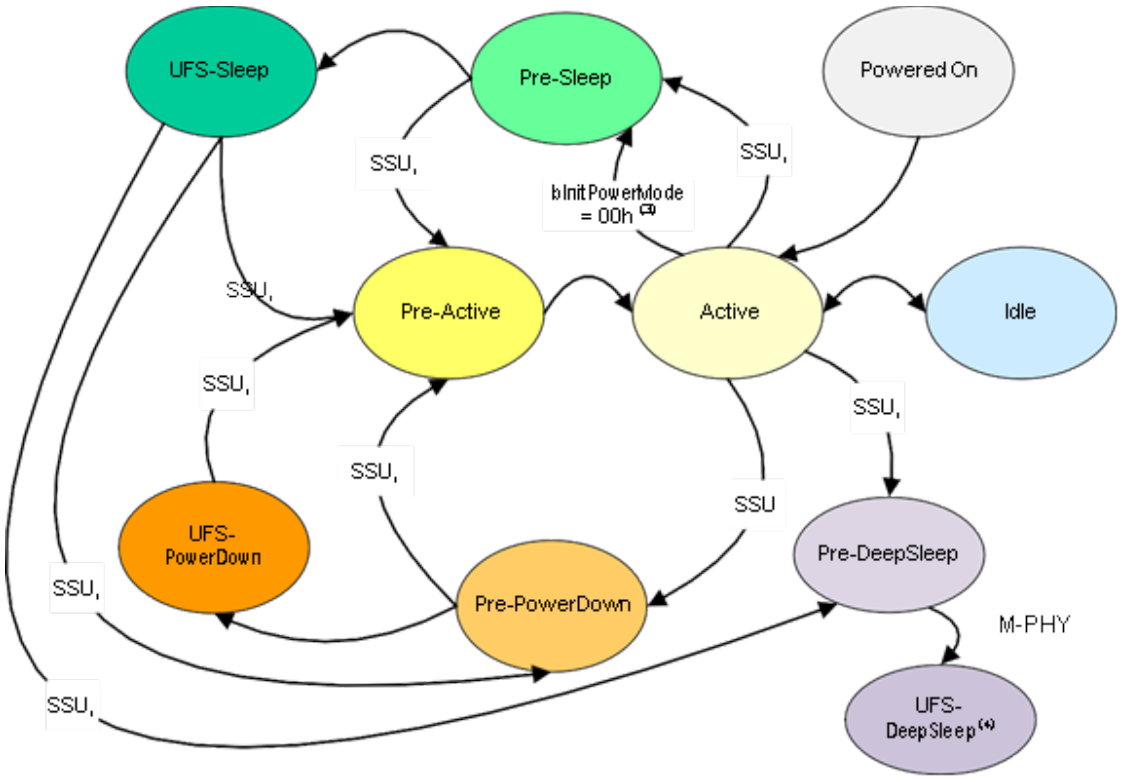
Figure 3-3- Clock input levels, rise time and fall time



3.5 Power Mode

The UFS device support multiple power mode which controlled by the START STOP UNIT command and some attributes. UFS will support seven power mode(Active,Idle,Pre-active,UFS sleep,Pre-sleep,UFS-PowerDown,Pre-Power down) defined by JEDEC UFS 3.1 specification.

Figure 3-4- Power Mode state Machine



(1) This transition may occur only if the SSU command that caused the transition to Pre-Sleep had IMMED set to one.

(2) This transition may occur only if the SSU command that caused the transition to Pre-PowerDown had IMMED set to one.

(3) This automatic transition shall occur at the end of device initialization if bInitPowerMode = 00h.

(4) The only way to exit from UFS-DeepSleep power mode is using a hardware reset or a power cycle.

UFS Power mode	Unipro Power Mode	M-phy Power Mode	VCC Power
ACTIVE	FAST_STATE	HS-BURST	ON
IDLE	HIB_STATE	Hibern8	ON
SLEEP	HIB_STATE	Hibern8	OFF/ON
DEEP SLEEP	OFF_STATE	UNPOWERED	OFF/ON
POWER DOWN	HIB_STATE	Hibern8	OFF/ON

3.5.1 Active Power Mode

Valid values for the bActiveICCLevel are from "00h" to "0Fh", other values are reserved and should not be set. UFS devices should primarily use settings of "06h" and "0Ch", for normal (battery) and high (plugged in) power operating modes.

The bInitActiveICCLevel parameter in the Device Descriptor allows the user to configure the Active ICC level after power on or reset.

The bInitPowerMode parameter in the Device Descriptor defines the power mode to which the device shall transition to after completing the initialization phase (fDeviceInit cleared to zero).
Active Mode can be entered from the Powered On mode or the Pre-Active mode after the completion of all setup necessary to handle commands.

The following power mode may be: Idle, Pre-Sleep, or Pre-PowerDown.
All supported commands are available in Active Mode.

3.5.2 Idle Power Mode

The Idle power mode is reached when the device is not executing any operation. In general, the M-PHY interface may be in STALL, SLEEP or HIBERN8 state. If background operations are continuing, the device should be considered Active power mode.

This mode can only be entered from an Active power mode, and the following state is always the Active power mode. The receipt of any command will transition the device into Active power mode.

3.5.3 Pre-Active Power Mode

The Pre-Active power mode is a transitional mode associated with Active power mode. The power consumed will be no more than that consumed in Active power mode. The device shall remain in this power mode until all of the preparation needed to accept commands has been completed.

Pre-Active power mode can be entered from Pre-Sleep, Sleep, Pre-PowerDown, or PowerDown. The following power mode is the Active power mode.

a. The Device well known logical unit may successfully complete only: START STOP UNIT command and REQUEST SENSE command; other commands may be terminated with CHECK CONDITION status, with the sense key set to NOT READY, with the additional sense code set to LOGICAL UNIT IS IN PROCESS OF BECOMING READY. See table 3-4 for further detail.
b. A REQUEST SENSE command shall terminated with GOOD status and provide pollable sense data with the sense key set to NO SENSE, and the additional sense code set to LOGICAL UNIT TRANSITIONING TO ANOTHER POWER CONDITION.

3.5.4 UFS-Sleep Power Mode

The UFS-Sleep power mode allows to reduce considerably the power consumption of the device.

VCC powersupply can be removed in this state.

The UFS-Sleep power mode is entered from Pre-Sleep power mode.

While in UFS-Sleep power mode:

a. the Device well known logical unit may successfully complete only: START STOP UNIT command and REQUEST SENSE command; other commands may be terminated with CHECK CONDITION status, with the sense key set to NOT READY and the additional sense code set to LOGICAL UNIT NOT READY, INITIALIZING COMMAND REQUIRED. See table 3-4 for further detail.
b. REQUEST SENSE command shall be terminated with GOOD status and provide pollable sense data with the sense key set to NOT READY and the additional sense code set to LOGICAL UNIT NOT READY, INITIALZING COMMAND REQUIRED.

It is recommended to put the link in HIBERN8 state, although it is actually under host control and can come up and down independently of the UFS power mode.

VCC power supply should be restored before issuing START STOP UNIT command to request transition to Active power mode or PowerDown power mode.

3.5.5 Pre-Sleep Power Mode

The Pre-Sleep Mode is a transitional mode associated with UFS-Sleep entry. The power consumed will be no more than that consumed in Active power mode. Pre-Sleep can be entered from Active power mode.

The device will automatically advance to Sleep power mode once any outstanding operations and management activities have been completed.
The device will transition from Pre-Sleep power mode to Pre-Active power mode if START STOP UNIT command with POWER CONDITION = 1h is issued.

While in Pre-Sleep power mode:

a. The Device well known logical unit may successfully complete only: START STOP UNIT command, REQUEST SENSE command and task management functions; other commands may be terminated with CHECK CONDITION status, with the sense key set to ILLEGAL REQUEST. See table 3-4 for further detail.
b. A REQUEST SENSE command shall be terminated with GOOD status and provide pollable sense data with the sense key set to NO SENSE and the additional sense code set to LOGICAL UNIT TRANSITIONING TO ANOTHER POWER CONDITION.

3.5.6 Pre-DeepSleep Power Mode

The Pre-DeepSleep power mode is a transitional mode associated with UFS-DeepSleep entry. The power consumed shall be no more than that consumed in Active power mode. Pre-DeepSleep may be entered from Active or UFS-Sleep power mode.

The device sends the response with GOOD status to START STOP UNIT command with the POWER CONDITION field set to 4h after any outstanding operations and management activities have been completed. Then the device waits for HIBERN8 state transition. The host is expected to put the link in HIBERN8 state after receiving the response to the START STOP UNIT command. The device shall transit to UFS-DeepSleep power mode after HIBERN8 state transition is completed.

While in Pre-DeepSleep power mode, the Device does not respond to any host commands

3.5.7 UFS-PowerDown Power Mode

The UFS-PowerDown power mode is the maximum power saving mode. All volatile data may be lost and VCC or all power supplies can be removed.
This mode is automatically entered from the Pre-PowerDown power mode, at the completion of the power mode transition.

While in UFS-PowerDown power mode:

a. The Device well known logical unit may successfully complete only: START STOP UNIT command and REQUEST SENSE command; other commands may be terminated with CHECK CONDITION status, with the sense key set to NOT READY and the additional sense code set to LOGICAL UNIT NOT READY, INITIALIZING COMMAND REQUIRED. See table 3-4 for further detail.
b. A REQUEST SENSE command shall be terminated with GOOD status and provide pollable sense data with the sense key set to NOT READY, and the additional sense code set to LOGICAL UNIT NOT READY, INITIALIZING COMMAND REQUIRED.

3.5.8 Pre-PowerDown Power Mode

The Pre-PowerDown power mode is a transitional mode associated with UFS-PowerDown entry.
The power consumed will be no more than that consumed in Active power mode. Pre-PowerDown can be entered from Active or Sleep.

The device will automatically advance to PowerDown power mode once any outstanding operations and management activities have been completed.

The device will transition to Pre-Active mode if START STOP UNIT command with POWER CONDITION field set to 1h is issued.

The following power mode may be PowerDown or Pre-Active.

While in Pre-PowerDown power mode:

a. The Device well known logical unit may successfully complete only: START STOP UNIT command REQUEST SENSE command and task management functions; other commands may be terminated

with CHECK CONDITION status, with the sense key set to ILLEGAL REQUEST. See table 3-4 for further detail.

b. A REQUEST SENSE command shall be terminated with GOOD status and provide pollable sense data with the sense key set to NO SENSE and the additional sense code set to LOGICAL UNIT TRANSITIONING TO ANOTHER POWER CONDITION.

3.5.9 Responses to SCSI commands

Table 3-4 - defines the Device well known logical unit response to a START STOP UNIT command for a given power mode. It is assumed that the IMMED bit in START STOP UNIT commands is set to zero.

Table 3-4 – Device Well Known Logical Unit Responses to SSU command

Current Power Mode	PC	STATUS	SENSE KEY	ASC, ASCQ
Pre-Active	1h	GOOD [1]	-	-
	Others	CHECK CONDITION	NOT READY	LOGICAL UNIT NOT READY, START STOP UNIT COMMAND IN
Active	1h, 2h, 3h	GOOD [1]	-	-
	Others	CHECK CONDITION	ILLEGAL REQUEST	INVALID FIELD IN CDB
Pre-Sleep	2h	GOOD [1]	-	-
	Others	CHECK CONDITION	NOT READY	LOGICAL UNIT NOT READY, START STOP UNIT COMMAND IN
UFS-Sleep	1h, 2h, 3h	GOOD [1]	-	-
	Others	CHECK CONDITION	ILLEGAL REQUEST	INVALID FIELD IN CDB
Pre-DeepSleep	Device is not able to accept START STOP UNIT command in this power mode			
UFS-DeepSleep	Device is not able to accept START STOP UNIT command in this power mode			
Pre-PowerDown	3h	GOOD [1]	-	-
	Others	CHECK CONDITION	NOT READY	LOGICAL UNIT NOT READY, START STOP UNIT COMMAND IN
UFS-PowerDown	1h, 3h	GOOD [1]	-	-
	Others	CHECK CONDITION	ILLEGAL REQUEST	INVALID FIELD IN CDB

NOTE 1 The START STOP UNIT command may not terminate with GOOD status for condition not due to CDB content.

3.5.10 Responses to SCSI commands (cont'd)

Table 3-5 - summarizes the response that the Device well known logical unit may provide to a command other than START STOP UNIT for various device power modes.

Table 3-5 - Device Well Known Logical Unit Responses to commands other than SSU

Power Mode	Command	STATUS	SENSE KEY	ASC, ASCQ
Pre-Active	REQUEST SENSE	GOOD (1)	-	-
	Others (1)	CHECK CONDITION	NOT READY	LOGICAL UNIT IS IN PROCESS OF BECOMING READY
Pre-Sleep, PrePowerDown	REQUEST SENSE	GOOD (1)	-	-
	Others (1)	CHECK CONDITION	ILLEGAL REQUEST	-
UFS-Sleep, UFS-PowerDown	REQUEST SENSE	GOOD (1)	-	-
	Others (1)	CHECK CONDITION	NOT READY	LOGICAL UNIT NOT READY, INITIALIZING COMMAND
Pre-DeepSleep UFS-DeepSleep	Device is not able to accept any command in this power mode.			
NOTE 1 Rows identified with "Others" define Device well known logical unit response to command other than START STOP UNIT command and REQUEST SENSE command.				

Table 3-6 defines the pollable sense data for various device power modes.

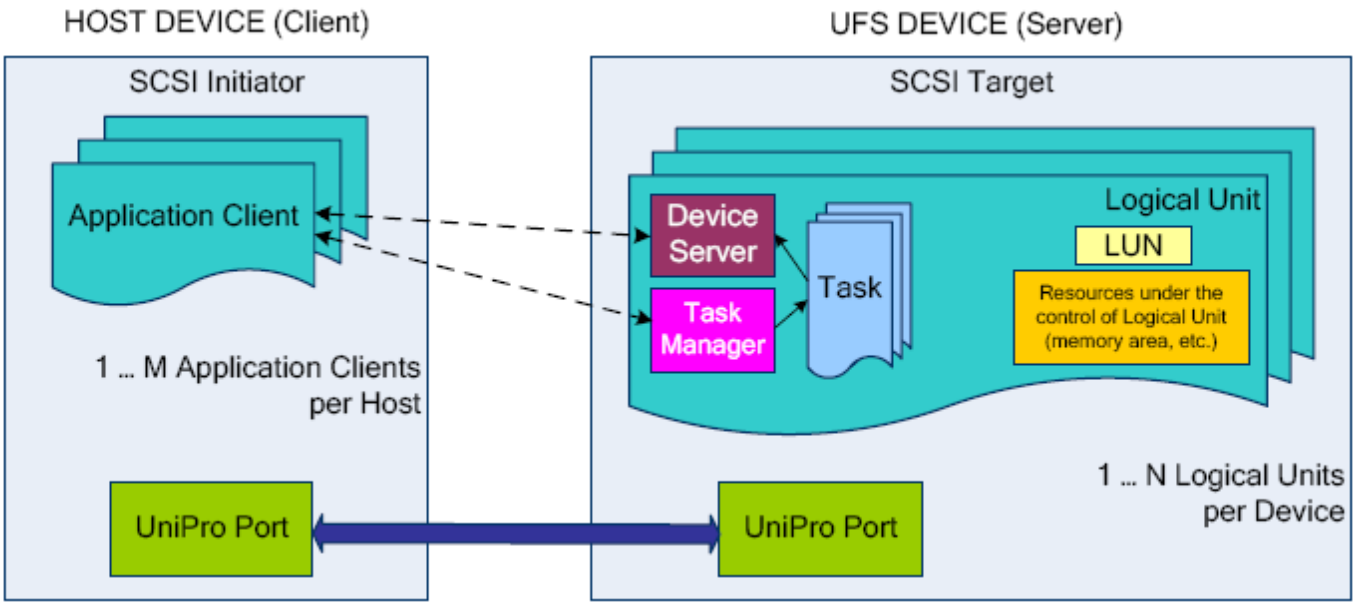
Table 3-6 Pollable Sense Data for each Power Modes

Power Mode	SENSE KEY	ASC, ASCQ
Pre-Active, Pre-Sleep, Pre-PowerDown	NO SENSE	LOGICAL UNIT TRANSITIONING TO ANOTHER POWER CONDITION
UFS-PowerDown, UFS-Sleep	NOT READY	LOGICAL UNIT NOT READY, INITIALIZING COMMAND REQUIRED

4 UFS SCSI Domain

4.1 UFS Logical Unit Definition

Figure 4-1- UFS SCSI Domain



- **1. A logical unit (LU):**
  It is an externally addressable, independent, processing entity that processes SCSI tasks (commands) and performs task management functions.
  1.1 Each logical unit is independent of other logical units in a device
  1.2 UFS shall support the amount of logical units specified by bMaxNumberLU, in addition to the well known logical units defined in JESD220D_10.8.5
  1.3 logical units may be used to store boot code, application code and mass storage data applications
- **2. DEVICE SERVER**: A conceptual object within a logical unit that processes SCSI commands.
- **3. TASK MANAGER**: A conceptual object within a logical unit that controls the sequencing of commands and performs task management functions.
- **4. TASK SET**: A conceptual group of 1 or more commands (a list, queue, etc.)
- **5. UniPro:**

  It is responsible for management of the link, including the PHY.
  The basic interface to the interconnect layer is UniPro definition of a CPort. CPort is used for all data
  transfer as well as all control and configuration messages. In general, multiple CPorts can be supported on a device and the number of CPorts is implementation dependent.

4.2 SCSI Command

Table 4-1 - UFS SCSI Command Set

Command name	Opcode	Command Support	Support	Note
FORMAT UNIT	04h	M	Yes	
INQUIRY	12h	M	Yes	
MODE SELECT (10)	55h	M	Yes	
MODE SENSE (10)	5Ah	M	Yes	
PRE-FETCH (10)	34h	M	Yes	
PRE-FETCH (16)	90h	O	Yes	
READ (6)	08h	M	Yes	
READ (10)	28h	M	Yes	
READ (16)	88h	O	Yes	
READ BUFFER	3Ch	M	Yes	
READ CAPACITY (10)	25h	M	Yes	
READ CAPACITY (16)	9Eh	M	Yes	
REPORT LUNS	A0h	M	Yes	
REQUEST SENSE	03h	M	Yes	
SECURITY PROTOCOL IN	A2h	M	Yes	
SECURITY PROTOCOL OUT	B5h	M	Yes	
SEND DIAGNOSTIC	1Dh	M	Yes	
START STOP UNIT	1Bh	M	Yes	
SYNCHRONIZE CACHE (10)	35h	M	Yes	
SYNCHRONIZE CACHE (16)	91h	O	No	
TEST UNIT READY	00h	M	Yes	
UNMAP	42H	M	Yes	
VERIFY (10)	2Fh	M	Yes	
WRITE (6)	0Ah	M	Yes	
WRITE (10)	2Ah	M	Yes	
WRITE(16)	8Ah	O	Yes	
WRITE BUFFER	3Bh	M	Yes	
M: mandatory, O: optional				
NOTE 1 SECURITY PROTOCOL IN command and SECURITY PROTOCOL OUT command are supported by the RPMB well known logical unit.				

5 UFS Supported Pages

Table 5-1 shows the mode pages supported by UFS device. This standard does not define any additional subpages.

Table 5-1 — UFS Supported Pages

PAGE NAME	PAGE CODE	SUBPAGE CODE	DESCRIPTION
CONTROL	0Ah	00h	Return CONTROL mode page
READ-WRITE ERROR RECOVERY	01h	00h	Return READ-WRITE ERROR RECOVERY mode page
CACHING	08h	00h	Return CACHING mode page
ALL PAGES	3Fh	00h	Return all mode pages (not including subpages)
ALL SUBPAGES	3Fh	FFh	Return all mode pages and subpages

If the device has more than one logical unit, host should read Mode Page Policy VPD in order to know whether the logical unit maintains its own copy of the mode page and subpage or all logical units share the mode page and subpage.

5.1 Control Mode Page

The Control mode page provides controls over SCSI features that are applicable to all device types (e.g., task set management and error logging).

Table 5-2 defines the Control mode page default value (PC = 10b).

Table 5-2 — Control Mode Page default value

Byte \ Bit	7	6	5	4	3	2	1	0
0	PS	SPF (0)	PAGE CODE (0Ah)					
1	PAGE LENGTH (0Ah)							
2	TST = 000b			TMF_ONLY =0b	DPICZ = 0b	D_SENSE =0b	GLTSD = 0b	RLEC = 0b
3	QUEUE ALGORITHM MODIFIER = 0001b				NUAR = 0b	QERR = 00b		Obsolete = 0b
4	VS = 0b	RAC = 0b	UA_INTLCK_CTRL = 00b		SWP = 0b	Obsolete = 000b		
5	ATO = 0b	TAS = 0b	ATMPE = 0b	RWWP = 0b	Reserved	AUTOLOAD MODE = 000b		
6	Obsolete = 0000h							
7								
8	(MSB) BUSY TIMEOUT PERIOD							
9								(LSB)
10	(MSB) EXTENDED SELF-TEST COMPLETION TIME							
11								(LSB)

NOTE 1 Default values for PS bit, BUSY TIMEOUT PERIOD field and EXTENDED SELF-TEST COMPLETION TIME field are device specific.

The following Control mode page field shall be changeable: SWP. The following Control mode page fields are not changeable: TST and BUSY TIMEOUT PERIOD. Other fields may or may not be changeable, refer to the vendor datasheet for details.

Table 5-3 — Control Mode Page Parameters

Byte	Bit	Description
1	7:5	**TST**: Indicates Task Set Type. 000b indicates the logical unit maintains one task set for all I_T nexuses. Others: reserved.
4	3:3	**SWP**: A software write protect (SWP) bit set to one specifies that the logical unit shall inhibit writing to the medium after writing all cached or buffered write data, if any. When SWP is one, all commands requiring writes to the medium shall be terminated with CHECK CONDITION status, with the sense key set to DATA PROTECT
8:9	7:0	**BUSY TIMEOUT PERIOD**: The BUSY TIMEOUT PERIOD field specifies the maximum time, in 100 milliseconds increments, that the application client allows for the device server to return BUSY status for commands from the application client. A 0000h value in this field is undefined. An FFFFh value in this field is defined as an unlimited period.
NOTE 1 In addition to the software write protection, logical units may be configured as permanently write protected or power on write protected. A logical unit is writeable if all types of write protection are disabled. Logical units may be write protected setting SWP to one or using one of the methods described in 12.3, Device Data Protection.		

5.2 Read-Write Error Recovery Mode Page

The Read-Write Error Recovery mode page specifies the error recovery parameters the device server shall use during any command that performs a read or write operation to the medium (e.g., READ command, WRITE command, or VERIFY command)

Table 5-4 defines the Read-Write Error Recovery mode page default value (PC = 10b).

Table 5-4 — Read-Write Error Recovery Mode Page default value

Bit Byte	7	6	5	4	3	2	1	0
0	PS	SPF (0b)	PAGE CODE (01h)					
1	PAGE LENGTH (0Ah)							
2	AWRE = 1b	ARRE = 0b	TB = 0b	RC = 0b	EER = 0b	PER = 0b	DTE = 0b	DCR = 0b
3	READ RETRY COUNT							
4	Obsolete = 00h							
5	Obsolete = 00h							
6	Obsolete = 00h							
7	TPERE = 0b	Reserved = 00000b					Restricted for MMC-6	
8	WRITE RETRY COUNT							
9	Reserved = 00h							
10	(MSB)	RECOVERY TIME LIMIT						
11								(LSB)
NOTE 1 Default values for PS field, READ RETRY COUNT field, WRITE RETRY COUNT field and RECOVERY TIME LIMIT are device specific.								

This standard does not define which Read-Write Error Recovery mode page fields are changeable, refer to vendor datasheet for details.

Table 5-5 — Read-Write Error Recovery Parameters

Byte	Bit	Description
3	7:0	**READ RETRY COUNT**: The READ RETRY COUNT field specifies the number of times that the device server shall attempt its recovery algorithm during read operations.
8	7:0	**WRITE RETRY COUNT**: The WRITE RETRY COUNT field specifies the number of times that the device server shall attempt its recovery algorithm during write operations.
10:11	7:0	**RECOVERY TIME LIMIT**: The RECOVERY TIME LIMIT field specifies in milliseconds the maximum time duration that the device server shall use for data error recovery procedures. When both a retry count and a recovery time limit are specified, the field that specifies the recovery action of least duration shall have priority.

5.3 Caching Mode Page

The Caching mode page defines the parameters that affect the use of the cache. A UFS device shall implement support for following parameters.

Table 5-6 defines the Caching mode page default value (PC = 10b).

Table 5-6 — Caching Mode Page default value

Bit Byte	7	6	5	4	3	2	1	0
0	PS	SPF (0b)	PAGE CODE (08h)					
1	PAGE LENGTH (12h)							
2	IC = 0b	ABPF = 0b	CAP = 0b	DISC = 0b	SIZE = 0b	WCE =1b	MF = 0b	RCD =0b
3	DEMAND READ RETENTION PRIORITY = 0000b				WRITE RETENTION PRIORITY = 0000b			
4	(MSB)	DISABLE PRE-FETCH TRANSFER LENGTH = 0000h						
5								(LSB)
6	(MSB)	MINIMUM PRE-FETCH = 0000h						
7								(LSB)
8	(MSB)	MAXIMUM PRE-FETCH = 0000h						
9								(LSB)
10	(MSB)	MAXIMUM PRE-FETCH CEILING = 0000h						
11								(LSB)
12	FSW = 0b	LBCSS = 0b	DRA = 0b	Vendor Specific = 00b		Reserved = 00b		NV_DIS = 0b
13	NUMBER OF CACHE SEGMENTS = 00h							
14	(MSB)	CACHE SEGMENT SIZE = 0000h						
15								(LSB)
16	Reserved = 00h							
17		Obsolete = 000000h						
18								
19								

The following Caching mode page fields shall be changeable: WCE and RCD. Other fields may or may not be changeable, refer to the vendor datasheet for details

5.4 Caching Mode Page Parameters

Table 5-7 — Caching Mode Page Parameters

Byte	Bit	Description
2	2:2	**WCE**: WRITE BACK CACHE ENABLE. A writeback cache enable bit set to zero specifies that the device server shall complete a WRITE command with GOOD status only after writing all of the data to the medium without error. A WCE bit set to one specifies that the device server may complete a WRITE command with GOOD status after receiving the data without error and prior to having written the data to the medium.
2	0:0	**RCD**: READ CACHE DISABLE. A read cache disable bit set to zero specifies that the device server may return data requested by a READ command by accessing either the cache or medium. A RCD bit set to one specifies that the device server shall transfer all of the data requested by a READ command from the medium (i.e., data shall not be transferred from the cache).
NOTE 1 Fields that are not supported by UFS should be set to zero, and are documented assigning a value of zero to them (e.g., PS=0b). The device may ignore values in fields that are not supported by UFS.		

5.5 Vital product data parameters

5.5.1 Overview

The vital product data (VPD) pages are returned by an INQUIRY command with the EVPD bit set to one and contain vendor specific product information about a logical unit and SCSI target device.

A UFS device shall support the following VPD pages:

- Supported VPD Pages
- Mode Page Policy

Support for other VPD pages is optional.

5.5.2 VPD page format

Table 5- shows the VPD page structure.

Table 5-8 — VPD page format

Bit / Byte	7	6	5	4	3	2	1	0
0	PERIPHERAL QUALIFIER			PERIPHERAL DEVICE TYPE				
1	PAGE CODE							
2	(MSB)	PAGE LENGTH (n-3)						
3								(LSB)
4	(MSB)	VPD parameters						
N								(LSB)

The PERIPHERAL QUALIFIER field and the PERIPHERAL DEVICE TYPE field are the same as defined for standard INQUIRY data (see 11.3.2.2 JESD220D_10.8.5).

The PAGE CODE field identifies the VPD page and contains the same value as in the PAGE CODE field in the INQUIRY CDB (see 11.3.2 JESD220D_10.8.5).

The PAGE LENGTH field indicates the length in bytes of the VPD parameters that follow this field. See

[SPC] for further details.

5.5.3 Supported VPD Pages VPD page

The Supported VDP Pages VPD page contains a list of the VPD page codes supported by the logical unit (see Table 5-9).

Table 5-9— Supported VPD Pages VPD page

Bit / Byte	7	6	5	4	3	2	1	0
0	PERIPHERAL QUALIFIER			PERIPHERAL DEVICE TYPE				
1	PAGE CODE (00h)							
2	(MSB)							
3	PAGE LENGTH (n-3)							(LSB)
4	Supported VPD page list							
N								

The supported VPD page list shall contain a list of all VPD page codes implemented by the logical unit in ascending order beginning with page code 00h.

The Mode Page Policy VPD page (see Table 5-10) indicates which mode page policy is in effect for each mode page supported by the logical unit.

Table 5-10 — Mode Page Policy VPD page

Bit / Byte	7	6	5	4	3	2	1	0
0	PERIPHERAL QUALIFIER			PERIPHERAL DEVICE TYPE				
1	PAGE CODE (87h)							
2	(MSB)			PAGE LENGTH (n-3)				
3								(LSB)
	Mode page policy descriptor list							
4				Mode page policy descriptor [first]				
7								
	...							
n-3				Mode page policy descriptor [last]				
N								

Each mode page policy descriptor (see Table 5-11) contains information describing the mode page policy for one or more mode pages or subpages.

Table 5-11 — Mode page policy descriptor

Bit / Byte	7	6	5	4	3	2	1	0
0	Reserved		POLICY PAGE CODE					
1	POLICY SUBPAGE CODE							
2	MLUS	Reserved					MODE PAGE POLICY	
3	Reserved							

The POLICY PAGE CODE field and POLICY SUBPAGE CODE field indicate the mode page and subpage to which the descriptor applies. See [SPC] for further details.

5.5.4 Mode Page Policy VPD page (cont'd)

If more than one logical unit are configured in the device, a multiple logical units share (MLUS) bit set to one indicates the mode page and subpage identified by the POLICY PAGE CODE field and POLICY SUBPAGE CODE field is shared by more than one logical unit.

A MLUS bit set to zero indicates the logical unit maintains its own copy of the mode page and subpage identified by the POLICY PAGE CODE field and POLICY SUBPAGE CODE field.

Table 5-12 describes the mode page policies.

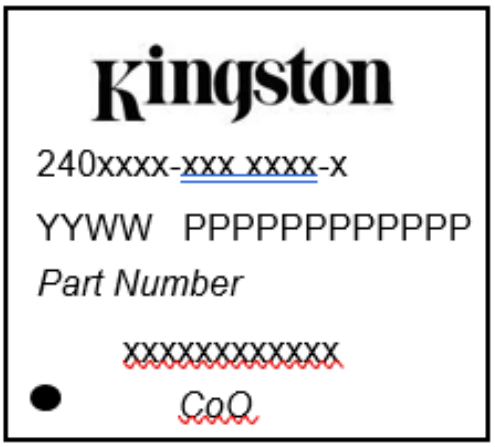
Code	Description
00b	Shared
01b	Per target port
10b	Obsolete
11b	Per I_T nexus

NOTE: This standard defines only one target port and one initator port.

MODE PAGE POLICY field shall be set to zero (Shared).

See [SPC] for further details about Mode Page Policy VPD page

6 Marking



Line 1: Kingston logo

Line 2: 240xxxx-xxx xxxx-x: Internal control number

Line 3: YYWW: Date code (YY– Last 2 digital of year, WW- Work week)

PPPPPPPPPPPP Internal control number (within 12 digits)

Line 4: Part Number: xxxxxx-xxxxxxx

Line 5: xxxxxxxxxxxx: Internal control number (within 12 digits)

Line 6: Country of Origin (CoO): TAIWAN *or* CHINA

7 Revision History

Rev.	History	Date	Remark	Editor
v1.0	Initial Release	02 / 2022		MC
v1.1	Added Kingston Contact Information	06 / 2023		KV

Contact Kingston

For more information, visit us at: https://www.kingston.com/en/solutions/embedded-and-industrial

For direct support, please contact us at: https://www.kingston.com/en/form/embedded

For quick questions, please email us at: emmc@kingston.com