

### DESCRIPTION

The MP2236C is a high-frequency, synchronous, rectified, step-down, switch-mode converter. The MP2236C offers a fully integrated solution that achieves up to 6A of continuous output current ( $I_{OUT}$ ), with excellent load and line regulation across a wide input supply range.

Constant-on-time (COT) control operation provides fast transient response. Full protection features include hiccup over-current protection (OCP) and thermal shutdown.

The MP2236C requires a minimal number of readily available, standard external components, and is available in a space-saving TSOT23-8 package.

### FEATURES

- Forced Continuous Conduction Mode (FCCM)
- Wide 3V to 18V Operating Input Voltage ( $V_{IN}$ ) Range
- 6A Continuous Output Current ( $I_{OUT}$ )
- 25m $\Omega$  and 12m $\Omega$  Low On Resistance ( $R_{DS(ON)}$ ) Internal Power MOSFETs
- Default 600mV Reference Voltage ( $V_{FB}$ )
- Adjustable Output Voltage ( $V_{OUT}$ )
- 600kHz Switching Frequency ( $f_{SW}$ )
- On time ( $t_{ON}$ ) Extension
- Hiccup Over-Current Protection (OCP)
- Thermal Shutdown Protection
- Available in a TSOT23-8 Package



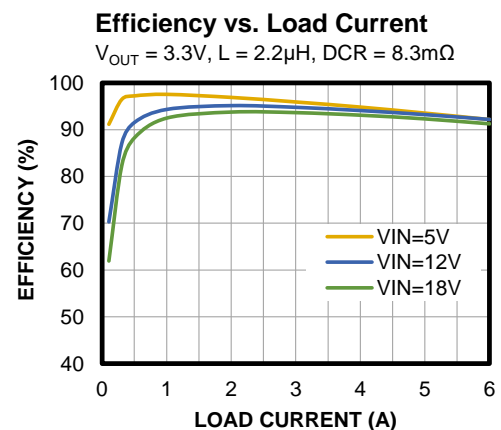
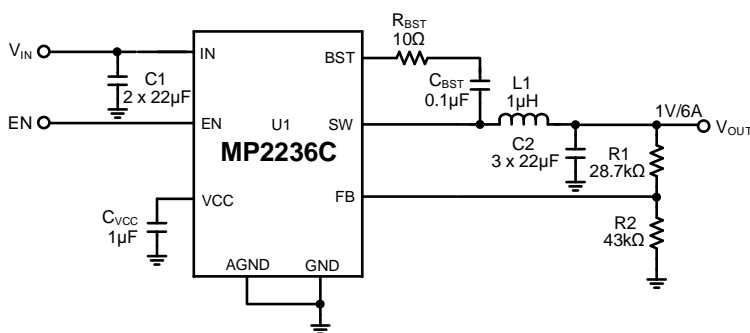
Optimized Performance with  
MPS Inductor MPL-AL6050 Series

### APPLICATIONS

- Flat-Panel Televisions and Monitors
- Digital TV Power Supplies
- Digital Set-Top Boxes
- Distributed Power Systems

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### TYPICAL APPLICATION



### ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP2236CGJ	TSOT23-8	See Below	1

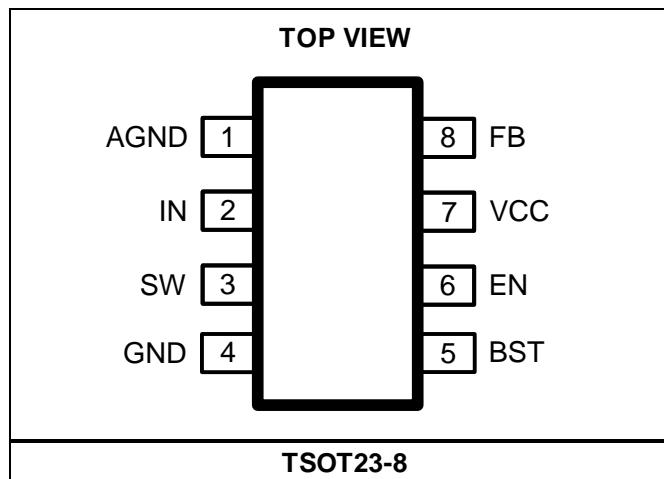
For Tape & Reel, add suffix -Z (e.g. MP2236CGJ-Z).

### TOP MARKING

| BRMY

BRM: Product code of MP2236CGJ  
Y: Year code

### PACKAGE REFERENCE



## PIN FUNCTIONS

Pin #	Name	Description
1	AGND	<b>Analog ground.</b> Connect AGND to GND using a short and wide PCB trace.
2	IN	<b>Supply voltage.</b> The MP2236C operates from a 3V to 18V input rail. Use a ceramic capacitor to decouple the input rail. Connect the IN pin using a wide PCB trace.
3	SW	<b>Switch output.</b> Connect the SW pin using a wide PCB trace.
4	GND	<b>System power ground.</b> The GND pin is the regulated output voltage ( $V_{OUT}$ )'s reference ground, and requires special consideration in the PCB layout. Connect GND to the ground plane with copper traces and vias.
5	BST	<b>Bootstrap.</b> Connect a 0.1 $\mu$ F capacitor between SW and BST to form a floating supply across the high-side MOSFET (HS-FET) driver.
6	EN	<b>Enable.</b> Drive the EN pin high to enable the MP2236C. EN has a 2M $\Omega$ pull-down resistor to GND.
7	VCC	<b>Internal bias supply.</b> Decouple the VCC pin with a 1 $\mu$ F capacitor. The VCC capacitor should be placed close to VCC and GND.
8	FB	<b>Feedback.</b> Connect the FB pin to the external resistor divider's tap from the output to GND to set $V_{OUT}$ .

### ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

$V_{IN}$ .....	-0.3V to +20V
$V_{SW}$ .....	-0.3V (-6.5V for <10ns) .....to $V_{IN} + 0.7V$ (25V for <25ns)
$V_{BST}$ .....	$V_{SW} + 4V$
$V_{EN}$ .....	20V
All other pins .....	-0.3V to +4V
Continuous power dissipation ( $T_A = 25^\circ C$ ) <sup>(2) (5)</sup>	
TSOT23-8 .....	1.89W
Junction temperature .....	150 $^\circ C$
Lead temperature.....	260 $^\circ C$
Storage temperature .....	-65 $^\circ C$ to +150 $^\circ C$

### ESD Ratings

Human body model (HBM) .....	$\pm 2000V$
Charged device model (CDM) .....	$\pm 750V$

### Recommended Operating Conditions <sup>(3)</sup>

Supply voltage ( $V_{IN}$ ) .....	3V to 18V
Output voltage ( $V_{OUT}$ ).....	0.6V to 8V .....or $V_{IN} \times D_{MAX}$ <sup>(4)</sup>
Operating junction temp ( $T_J$ ).....	-40 $^\circ C$ to +125 $^\circ C$

### Thermal Resistance $\theta_{JA}$ $\theta_{JC}$

TSOT23-8		
EVL2236C-J-00A <sup>(5)</sup> .....	66.....	23.... $^\circ C/W$
JESD51-7 <sup>(6)</sup> .....	100 .....	55.... $^\circ C/W$

#### Notes:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature,  $T_J$  (MAX), the junction-to-ambient thermal resistance,  $\theta_{JA}$ , and the ambient temperature,  $T_A$ . The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $P_D$  (MAX) =  $(T_J$  (MAX) -  $T_A$ ) /  $\theta_{JA}$ . Exceeding the maximum allowable power dissipation can generate an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- The device is not guaranteed to function outside of its operating conditions.
- For more information about  $D_{MAX}$ , see the Low-Dropout (LDO) Operation section on page 12.
- Measured on the EVL2236C-J-00A, a 4-layer PCB (63.5mmx63.5mm).
- The value of  $\theta_{JA}$  given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

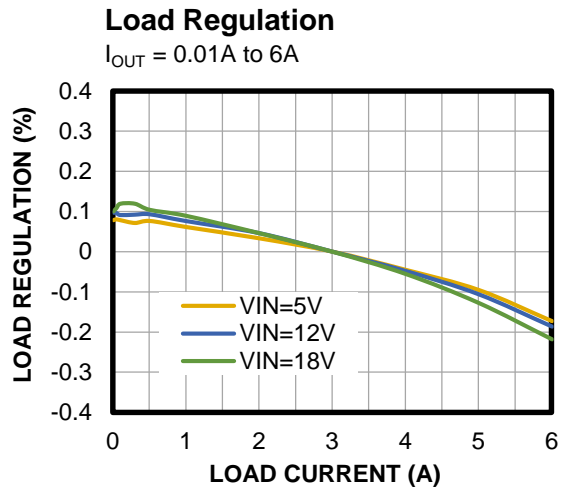
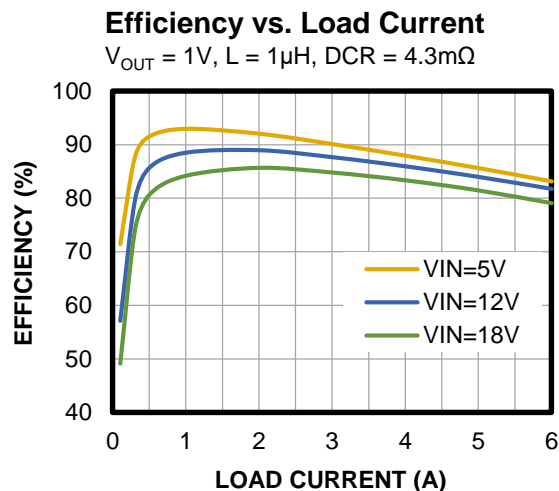
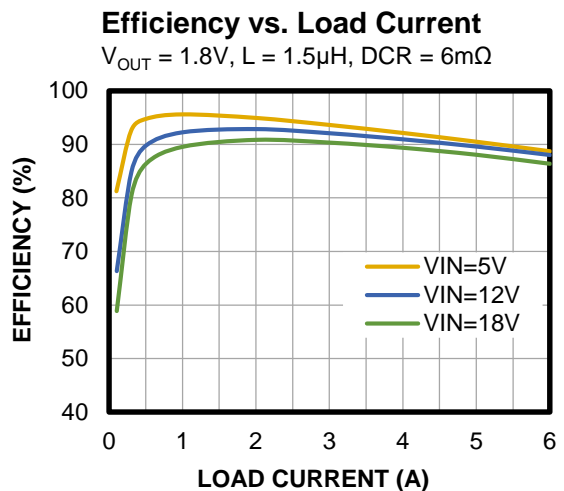
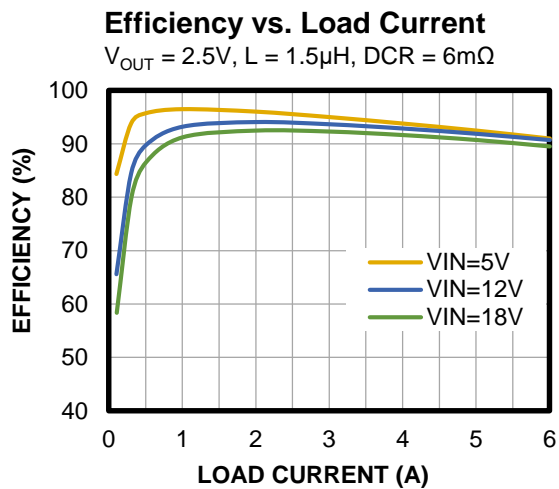
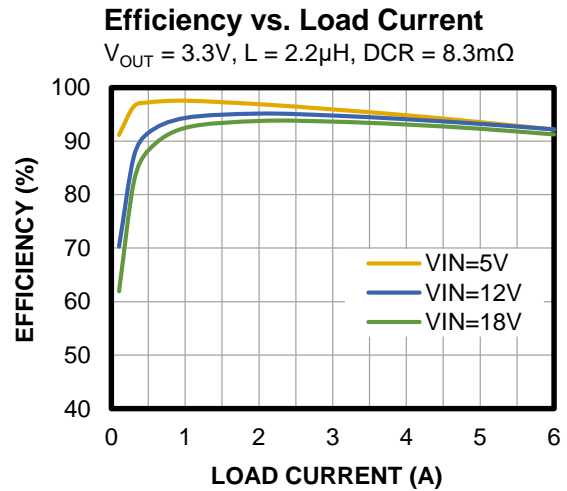
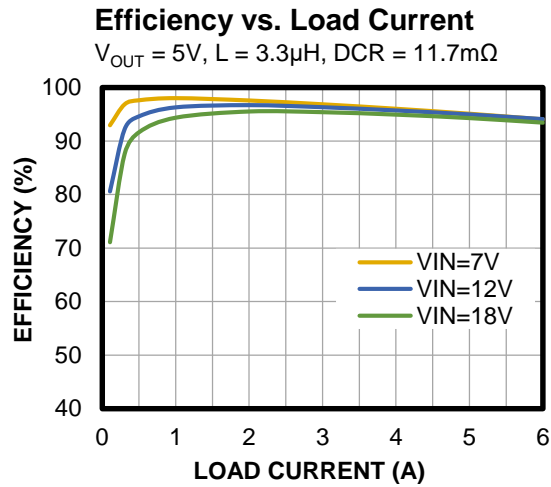
## ELECTRICAL CHARACTERISTICS

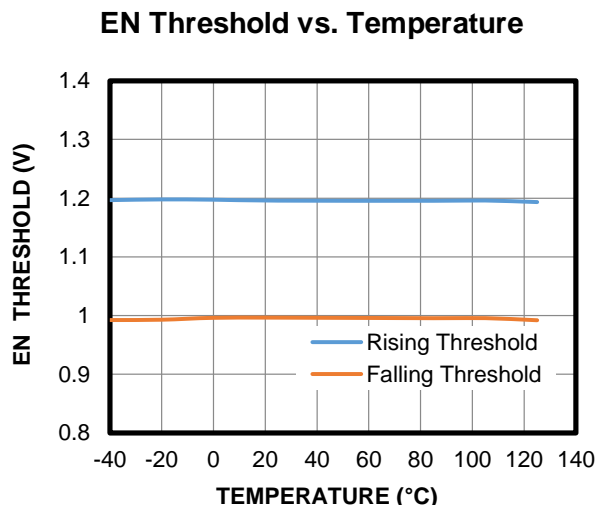
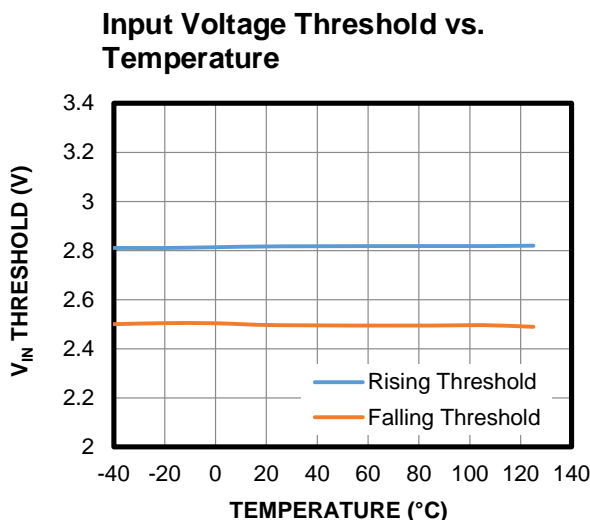
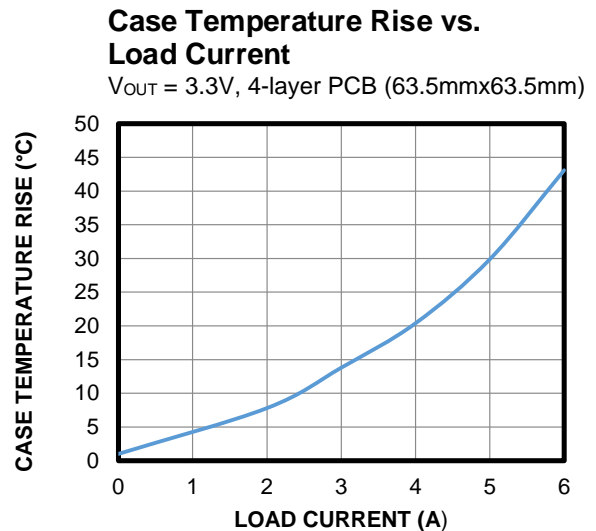
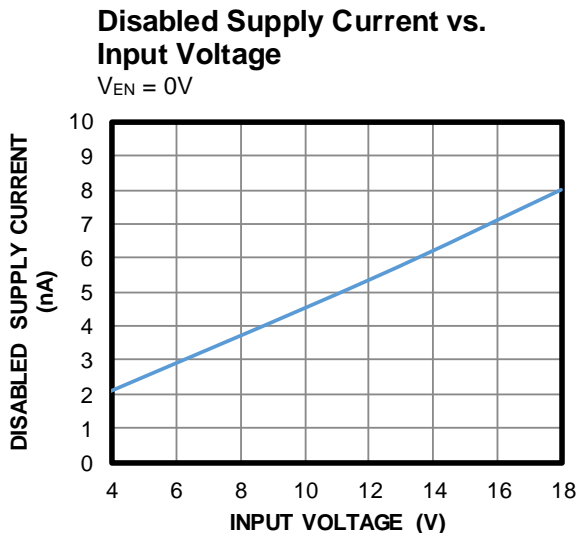
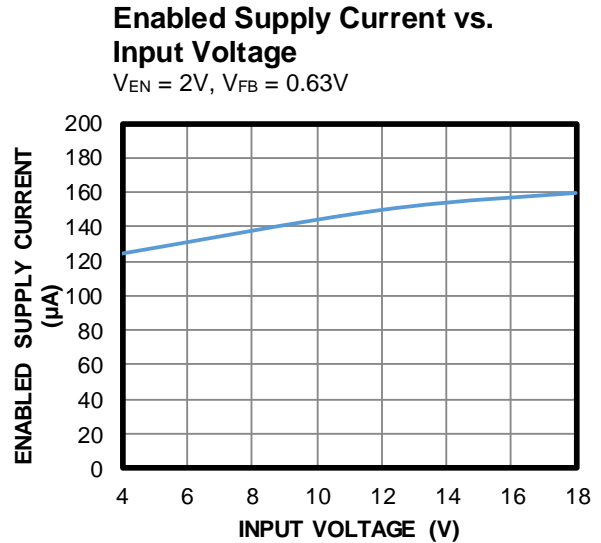
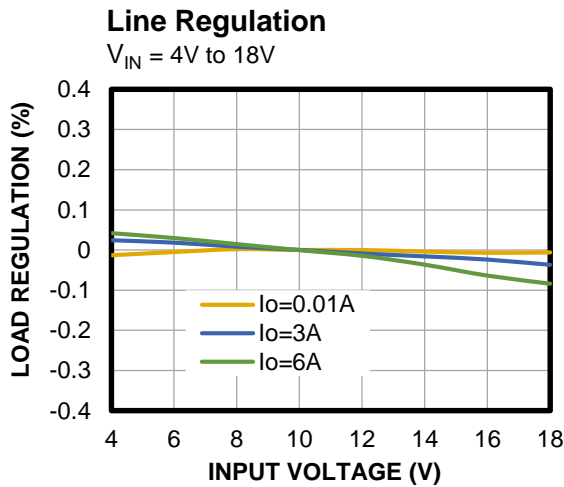
$V_{IN} = 12V$ ,  $T_J = -40^{\circ}C$  to  $+125^{\circ}C$  <sup>(7)</sup>, typical value is tested at  $T_J = 25^{\circ}C$ , unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Shutdown supply current	$I_{IN}$	$V_{EN} = 0V$ , $T_J = 25^{\circ}C$			1	$\mu A$
Quiescent supply current	$I_Q$	$V_{FB} = 0.63V$		550	650	$\mu A$
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)_{HS}}$	$V_{BST-SW} = 3.3V$		25		$m\Omega$
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)_{LS}}$			12		$m\Omega$
Switch leakage	$SW_{LKG}$	$V_{EN} = 0V$ , $V_{SW} = 0V$ , $T_J = 25^{\circ}C$			1	$\mu A$
Low-side (LS) valley current limit	$I_{LIMIT\_L}$		6	7.5		A
Switching frequency	$f_{SW}$	$V_{IN} = 12V$ , $V_{OUT} = 3.3V$	480	600	720	kHz
Minimum off time <sup>(8)</sup>	$t_{OFF\_MIN}$			170		ns
Minimum on time <sup>(8)</sup>	$t_{ON\_MIN}$			70		ns
Reference voltage	$V_{FB}$	$T_J = 25^{\circ}C$	594	600	606	mV
		$T_J = -40^{\circ}C$ to $+125^{\circ}C$	591	600	609	mV
Feedback (FB) current	$I_{FB}$	$V_{FB} = 0.63V$		10	50	nA
Enable (EN) rising threshold	$V_{EN\_RISING}$		1.12	1.2	1.28	V
EN hysteresis	$V_{EN\_HYS}$			200		mV
EN to GND pull-down resistor	$R_{EN}$	$V_{EN} = 2V$		2		$M\Omega$
$V_{IN}$ under-voltage lockout (UVLO) rising threshold	$V_{IN\_UVLO\_RISING}$		2.7	2.8	2.95	V
$V_{IN}$ UVLO threshold hysteresis	$V_{IN\_UVLO\_HYS}$			300		mV
VCC regulator voltage	$V_{CC}$	$I_{CC} = 5mA$		3.5		V
Under-voltage protection (UVP) threshold 1 <sup>(8)</sup>	$UVP_{TH1}$	Hiccup entry		80%		$V_{REF}$
Soft-start time	$t_{SS}$	$T_J = 25^{\circ}C$ , $V_{OUT}$ from 10% to 90%	0.5	1	1.5	ms
Thermal shutdown <sup>(8)</sup>	$T_{SD}$			150		$^{\circ}C$
Thermal hysteresis <sup>(8)</sup>	$T_{SD\_HYS}$			20		$^{\circ}C$

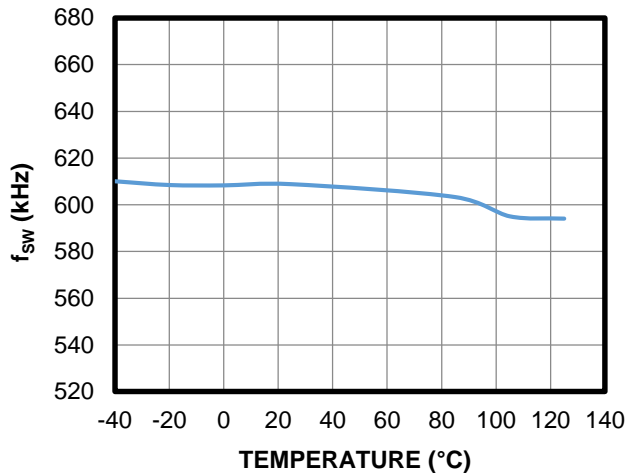
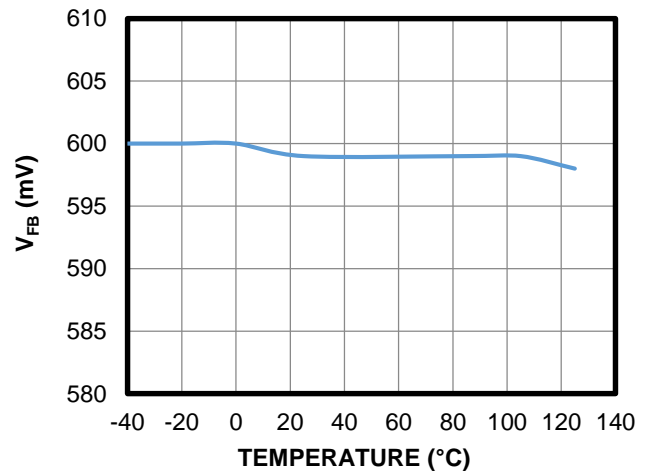
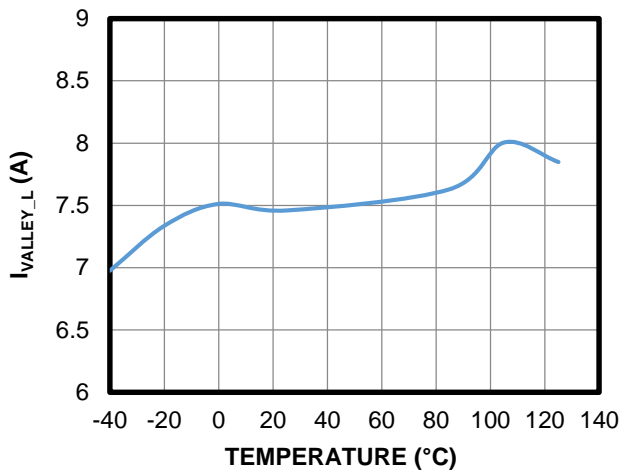
### Notes:

- 7) Not tested in production. Guaranteed by over-temperature correlation.  
 8) Derived by sample characterization. Not tested in production.

**TYPICAL CHARACTERISTICS**
 $V_{IN} = 12V, V_{OUT} = 1V, T_A = 25^\circ C$ , unless otherwise noted.


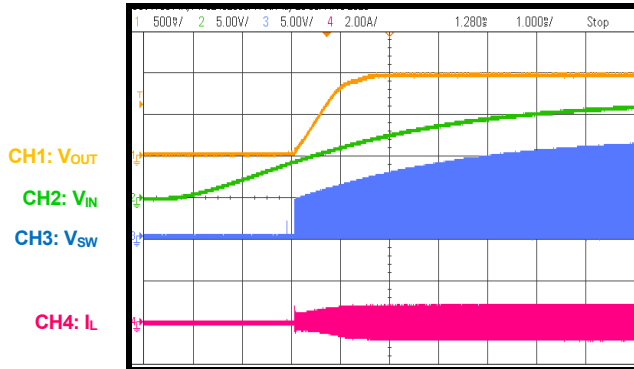
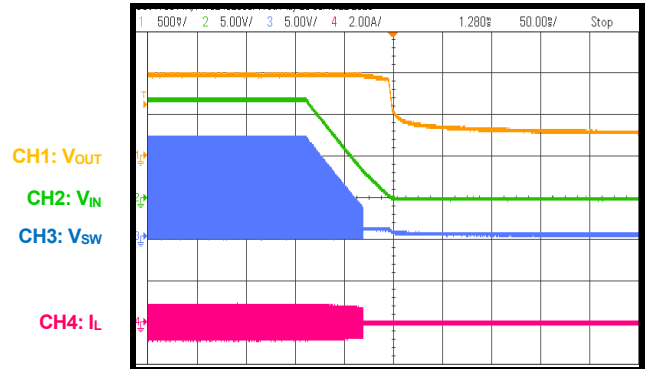
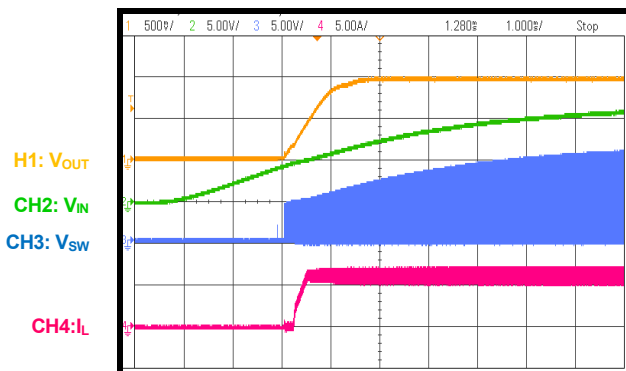
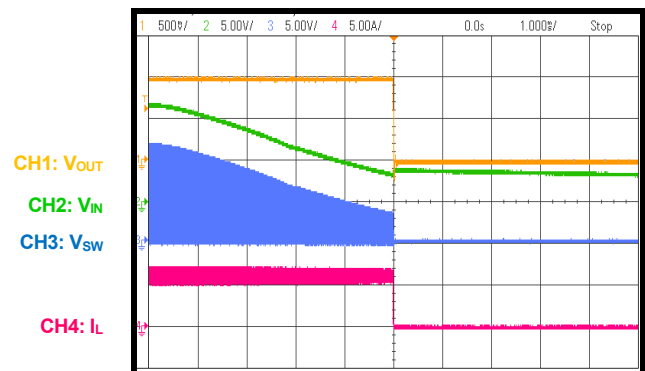
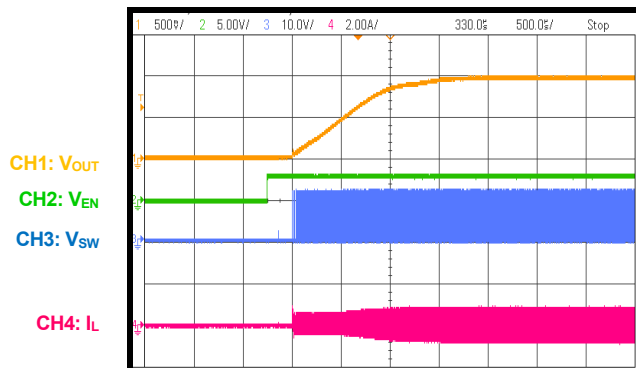
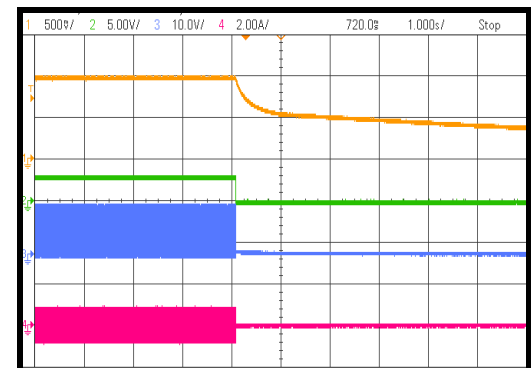
**TYPICAL CHARACTERISTICS (continued)**
 $V_{IN} = 12V, V_{OUT} = 1V, T_A = 25^{\circ}C$ , unless otherwise noted.


**TYPICAL CHARACTERISTICS (continued)**
 $V_{IN} = 12V$ ,  $V_{OUT} = 1V$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

**Switching Frequency vs. Temperature**

**FB Voltage vs. Temperature**

**LS Valley Current Limit vs. Temperature**


## TYPICAL PERFORMANCE CHARACTERISTICS

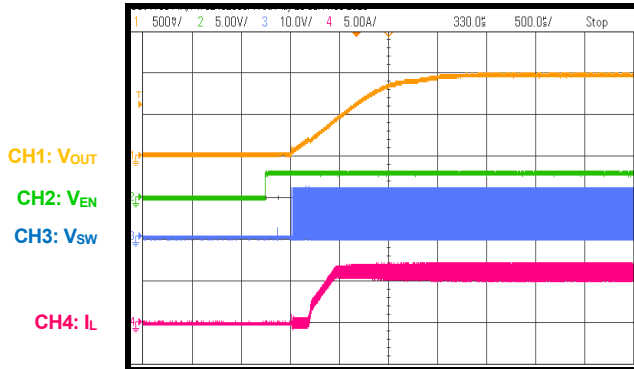
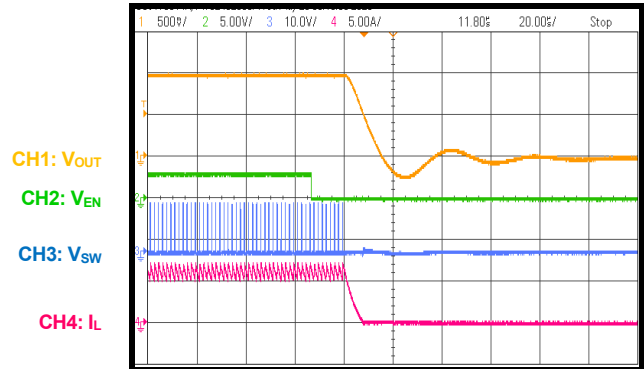
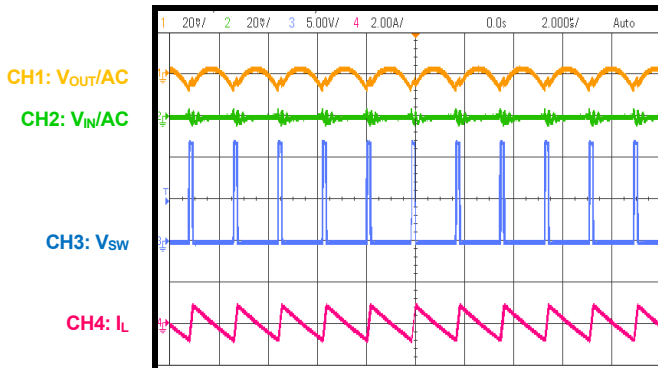
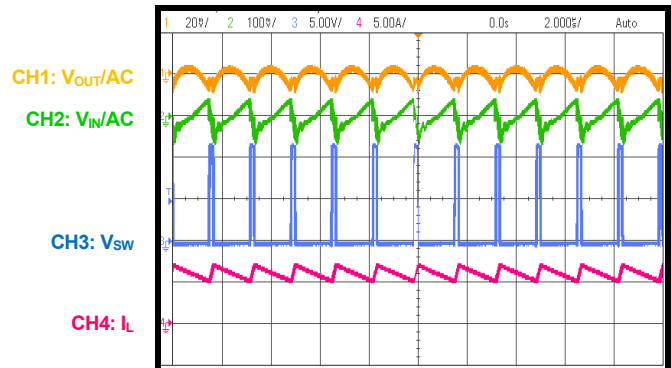
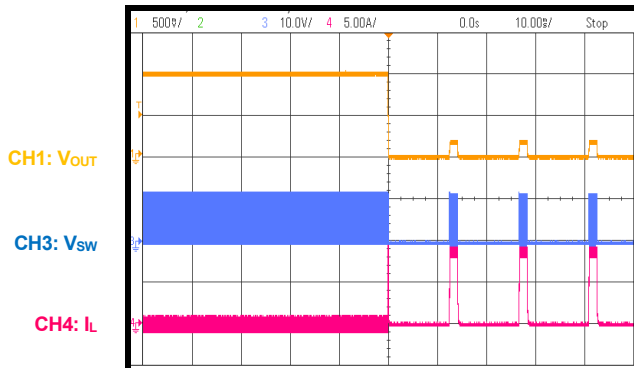
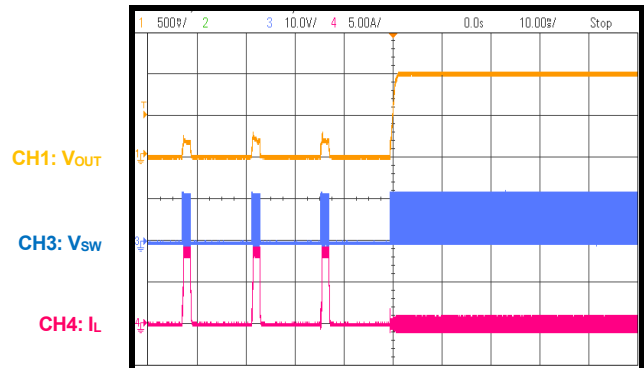
Performance waveforms are tested on the evaluation board from the Design Example section on page 15.  $V_{IN} = 12V$ ,  $V_{OUT} = 1V$ ,  $T_A = 25^{\circ}C$ , unless otherwise noted.

**Start-Up through  $V_{IN}$** 
 $I_{OUT} = 0A$ 

**Shutdown through  $V_{IN}$** 
 $I_{OUT} = 0A$ 

**Start-Up through  $V_{IN}$** 
 $I_{OUT} = 6A$ 

**Shutdown through  $V_{IN}$** 
 $I_{OUT} = 6A$ 

**Start-Up through EN**
 $I_{OUT} = 0A$ 

**Shutdown through EN**
 $I_{OUT} = 0A$ 




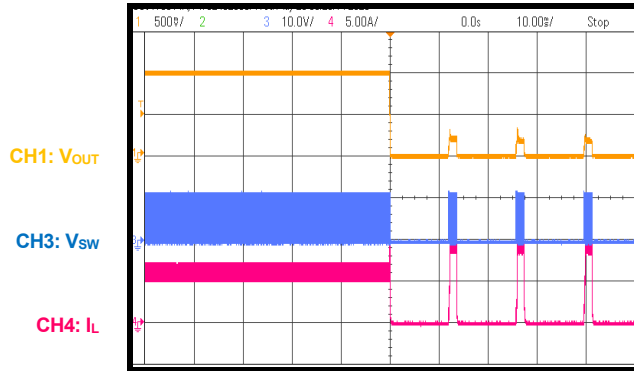
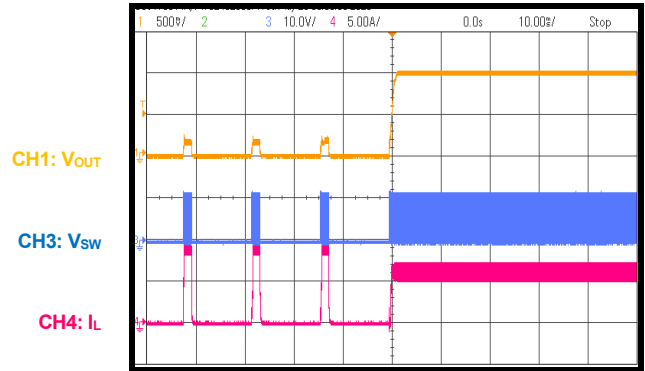
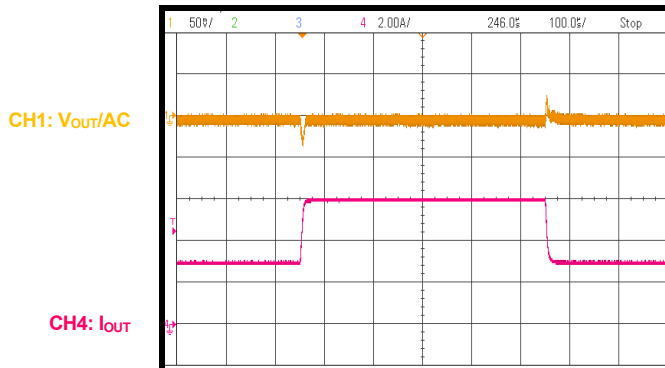
**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

Performance waveforms are tested on the evaluation board from the Design Example section on page 15.  $V_{IN} = 12V$ ,  $V_{OUT} = 1V$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

**Start-Up through EN**
 $I_{OUT} = 6A$ 

**Shutdown through EN**
 $I_{OUT} = 6A$ 

**Input and Output Ripple**
 $I_{OUT} = 0A$ 

**Input and Output Ripple**
 $I_{OUT} = 6A$ 

**Short-Circuit Entry**
 $I_{OUT} = 0A$ 

**Short-Circuit Recovery**
 $I_{OUT} = 0A$ 


**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

Performance waveforms are tested on the evaluation board from the Design Example section on page 15.  $V_{IN} = 12V$ ,  $V_{OUT} = 1V$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

**Short-Circuit Entry**
 $I_{OUT} = 6A$ 

**Short-Circuit Recovery**
 $I_{OUT} = 6A$ 

**Transient Response**
 $I_{OUT} = 3A$  to  $6A$ , slew rate =  $2.5A/\mu s$  by e-load


### FUNCTIONAL BLOCK DIAGRAM

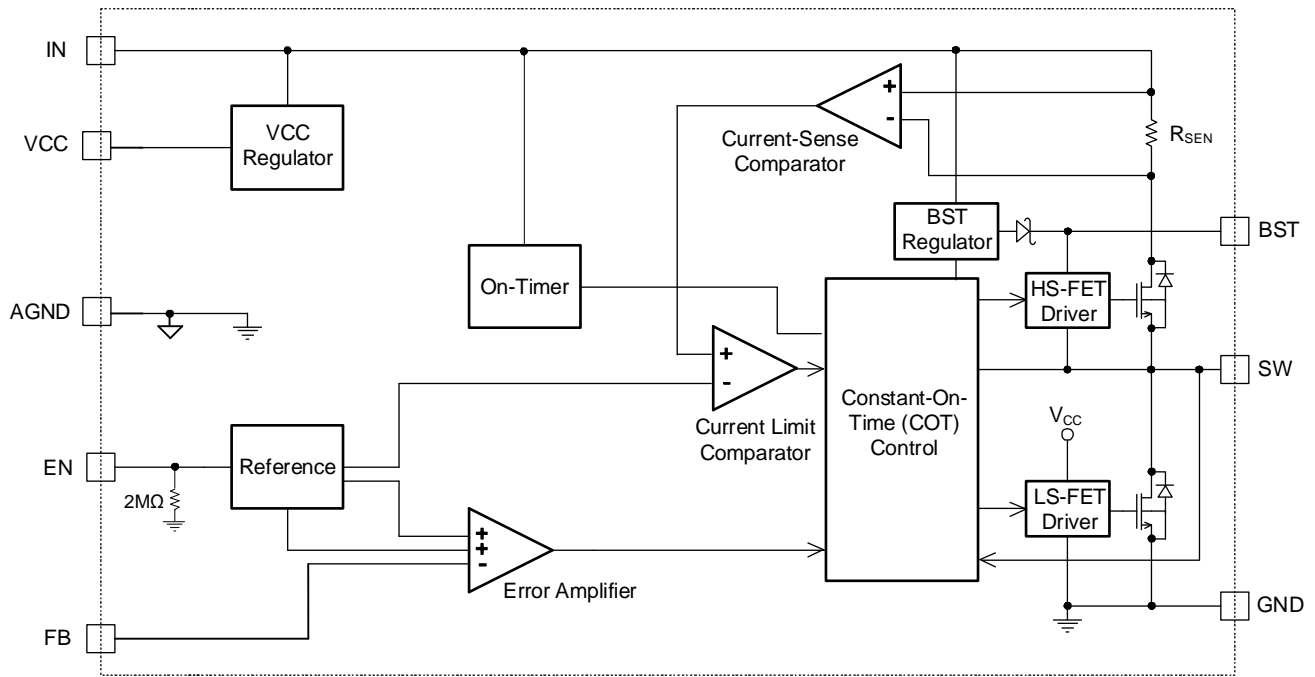
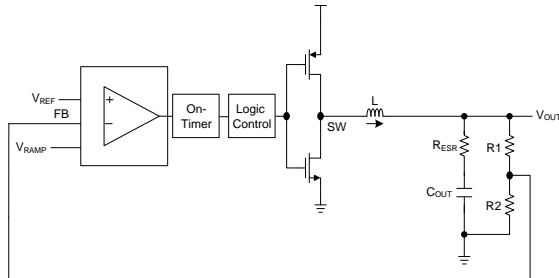


Figure 1: Functional Block Diagram

## OPERATION

The MP2236C is a fully integrated, synchronous, rectified, step-down, switch-mode converter. The device uses constant-on-time (COT) control to provide fast transient response and ease loop stabilization. Figure 2 shows the simplified ramp compensation block in the MP2236C.



**Figure 2: Simplified Compensation Block**

At the beginning of each cycle, the high-side MOSFET (HS-FET) turns on whenever the ramp voltage ( $V_{RAMP}$ ) is below the error amplifier (EA)'s output voltage ( $V_{EAO}$ ), which indicates an insufficient output voltage ( $V_{OUT}$ ). The on period is determined by both  $V_{OUT}$  and the input voltage ( $V_{IN}$ ) to make the switching frequency ( $f_{SW}$ ) fairly constant across the entire  $V_{IN}$  range.

After the on period elapses, the HS-FET turns off. By cycling the HS-FET on and off, the converter regulates  $V_{OUT}$ . The integrated low-side MOSFET (LS-FET) turns on when the HS-FET is off to minimize conduction loss.

If the HS-FET and LS-FET are turned on at the same time, a dead short occurs between the input and GND; this is called shoot-through. To avoid significantly reduced efficiency from shoot-through, the MP2236C generates a dead time (DT) internally between the HS-FET off period and LS-FET on period, and vice versa.

### Error Amplifier (EA)

The EA compares the FB voltage ( $V_{FB}$ ) against the internal 0.6V reference voltage ( $V_{REF}$ ) and outputs a pulse-width modulation (PWM) signal. The optimized internal ramp compensation minimizes the external component count and simplifies control loop design.

### Enable (EN)

EN is a digital control pin that turns the regulator on and off. Pull EN high to turn on the regulator. Pull EN low to turn off the regulator. An internal  $2M\Omega$  resistor is connected from EN to ground. EN can operate with a 20V  $V_{IN}$ , which allows EN to be connected directly to  $V_{IN}$  for automatic start-up.

### Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating with an insufficient supply voltage. The MP2236C's UVLO comparator monitors  $V_{IN}$ . The MP2236C is active when  $V_{IN}$  exceeds the UVLO rising threshold.

### Soft Start (SS) and Pre-Biased Start-Up

Soft start (SS) prevents the converter's  $V_{OUT}$  from overshooting during start-up. When the chip starts up, the internal circuitry generates a soft-start voltage ( $V_{SS}$ ) that ramps up from 0V to the internal  $V_{CC}$ . When  $V_{SS}$  is below  $V_{REF}$ , the EA uses  $V_{SS}$  as the reference. When  $V_{SS}$  exceeds  $V_{REF}$ ,  $V_{REF}$  takes over as the reference.

The soft-start time ( $t_{SS}$ ) is set to 1ms internally. If the MP2236C's output is pre-biased to a certain voltage during start-up, the IC disables the HS-FET and LS-FET switching until the voltage on the internal SS capacitor ( $C_{SS}$ ) exceeds the sensed  $V_{OUT}$  at FB.

### Low-Dropout (LDO) Operation

To improve dropout, the MP2236C is designed to extend its on time if the duty cycle exceeds 85%. When the HS-FET on time is extended, the frequency drops. The typical minimum frequency ( $f_{SW\_MIN}$ ) is 260kHz. When the frequency drops to 260kHz, it cannot reduce any further and the HS-FET off time begins decreasing. The duty cycle reaches its maximum ( $D_{MAX}$ ) when the off time is at its minimum value. If  $V_{IN}$  drops, the MP2236C operates at  $D_{MAX}$  and  $V_{OUT}$  drops.

The typical  $D_{MAX}$  can be calculated using Equation (1):

$$D_{MAX} = 1 - t_{OFF\_MIN} \times f_{SW\_MIN} \quad (1)$$

Where the minimum off time ( $t_{OFF\_MIN}$ ) is 170ns, and  $f_{SW\_MIN}$  is 260kHz.

### Over-Current Protection (OCP) and Hiccup Mode

The MP2236C offers cycle-by-cycle, over-current (OC) limiting control. The current-limit circuit employs a low-side (LS) valley current-sensing algorithm. The MP2236C uses the LS-FET on resistance ( $R_{DS(ON)}$ ) as a current-sensing element for valley-current limiting. When the LS-FET turns on, the inductor current ( $I_L$ ) is monitored by the voltage between GND and SW. As the positive current-sensing node, GND must be connected to the bottom MOSFET's source terminal. PWM cannot initiate a new cycle until  $I_L$  falls to the valley threshold.

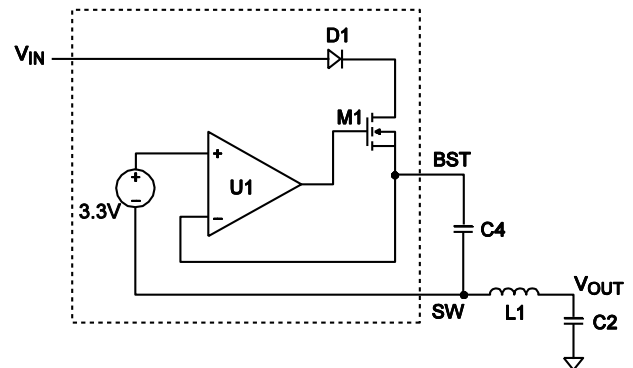
After the cycle-by-cycle OC limit is reached,  $V_{OUT}$  drops until it is below the under-voltage (UV) threshold. There are two UV thresholds: UV1 (80%) and UV2 (60%). Once UV1 and OC are both triggered, the MP2236C waits for 30 cycles. If OC exits after 31 cycles, then the MP2236C enters hiccup mode to periodically restart the part with a 12.5% duty cycle. If UV2 and OC are triggered, then the MP2236C enters hiccup mode after three cycles. This protection mode is especially useful when the output is dead-shortened to ground. The average short-circuit current is greatly reduced to alleviate thermal issues and protect the regulator. Once the OC condition is removed, the MP2236C exits hiccup mode and resumes normal operation.

### Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. If the silicon die temperature exceeds 150°C, the entire chip shuts down. Once the temperature drops below its lower threshold (typically 130°C), the chip is enabled again.

### Floating Driver and Bootstrap (BST) Charging

An external bootstrap (BST) capacitor ( $C_{BST}$ ) powers the floating power MOSFET driver, which has its own UVLO protection. The UVLO rising threshold is 1.2V, with a 150mV hysteresis. The  $C_{BST}$  voltage is regulated internally by  $V_{IN}$  through D1, M1, C4, L1, and C2 (see Figure 3).



**Figure 3: Internal BST Charging Circuit**

If  $V_{IN} - V_{SW}$  exceeds 3.3V, then U1 regulates M1 to maintain a 3.3V BST voltage across C4.

### Start-Up and Shutdown

If both  $V_{IN}$  and EN exceed their respective thresholds, the chip starts up. The reference block starts first, generating a stable  $V_{REF}$  and current, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Three events can shut down the chip: EN low,  $V_{IN}$  low, and thermal shutdown. During the shutdown procedure, the signaling path is blocked first to avoid any fault triggering. Then the internal supply rail is pulled down.

## APPLICATION INFORMATION

### Setting the Output Voltage ( $V_{OUT}$ )

An external resistor divider can set  $V_{OUT}$  through FB. R1 and R2 can be calculated using Equation (2):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.6V} - 1} \quad (2)$$

Table 1 lists the recommended feedback (FB) resistor values for common output voltages.

**Table 1: Resistor Selection for Common Output Voltages**

$V_{OUT}$ (V)	R1 (k $\Omega$ )	R2 (k $\Omega$ )
1.0	28.7	43
1.8	86.6	43
2.5	100	31.6
3.3	100	22.1
5	100	13.7

### Selecting the Inductor

**Optimized Performance with  
MPS Inductor MPL-AL6050 Series**

For most applications, it is recommended use a 0.47 $\mu$ H to 10 $\mu$ H inductor with a DC current rating at least 25% above the maximum load current. For the highest efficiency, use an inductor with a DC resistance below 15m $\Omega$ . For most designs, the inductance ( $L_1$ ) can be derived using Equation (3):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{SW}} \quad (3)$$

Where  $\Delta I_L$  is the inductor ripple current.

Set the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current ( $I_{L(MAX)}$ ) can be calculated using Equation (4):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (4)$$

Use a larger-value inductor for improved efficiency under light-load conditions below 100mA.

MPS inductors are optimized and tested for use with a complete line of integrated circuits.

Table 2 lists our power inductor recommendations. Select a part number based on the design requirements.

**Table 2: Power Inductor Selection**

Part Number	Inductance	Manufacturer
MPL-AL6050-3R3	3.3 $\mu$ H	MPS
MPL-AL6050-2R2	2.2 $\mu$ H	MPS
MPL-AL6050-1R5	1.5 $\mu$ H	MPS
MPL-AL6050-1R0	1.0 $\mu$ H	MPS

Visit [MonolithicPower.com](http://MonolithicPower.com) under Products > Inductors for more information.

### Selecting the Input Capacitor ( $C_{IN}$ )

The step-down converter has a discontinuous input current ( $I_{IN}$ ), and requires a capacitor to supply AC current while maintaining the DC  $V_{IN}$ . Use low-ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are recommended because of their low ESR and small temperature coefficients. For most applications, use two 22 $\mu$ F capacitors.

Since  $C_1$  absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in  $C_{IN}$  ( $I_{C1}$ ) can be estimated using Equation (5):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (5)$$

The worst-case condition occurs at  $V_{IN} = 2 \times V_{OUT}$ , which can be calculated with Equation (6):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (6)$$

For simplification, choose a  $C_{IN}$  with an RMS current rating that exceeds half of the maximum load current.

$C_{IN}$  can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1 $\mu$ F) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input.

The input voltage ripple ( $\Delta V_{IN}$ ) caused by the capacitance can be estimated using Equation (7):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

### Selecting the Output Capacitor ( $C_{OUT}$ )

The traditional COT control scheme is intrinsically unstable if the output capacitor's ( $C_{OUT}$ ) ESR is not high enough to act as an effective current-sense resistor. The MP2236C uses built-in, internal ramp compensation to ensure that the system is stable even without the help of  $C_{OUT}$ 's ESR. A pure ceramic capacitor solution can reduce the output ripple, total BOM cost, and board area significantly.

$C_{OUT}$  maintains the DC  $V_{OUT}$ . Use ceramic, tantalum, or low-ESR electrolytic capacitors. For the best results, use low-ESR capacitors to keep the output voltage ripple low. The output voltage ripple ( $\Delta V_{OUT}$ ) can be estimated using Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C2}\right) \quad (8)$$

Where  $L_1$  is the inductance,  $R_{ESR}$  is  $C_{OUT}$ 's ESR value, and  $C2$  is  $C_{OUT}$ .

For ceramic capacitors, the capacitance dominates the impedance at  $f_{SW}$  and causes the majority of  $\Delta V_{OUT}$ . For simplification,  $\Delta V_{OUT}$  can be estimated using Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (9)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at  $f_{SW}$ . For simplification,  $\Delta V_{OUT}$  can be approximated using Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (10)$$

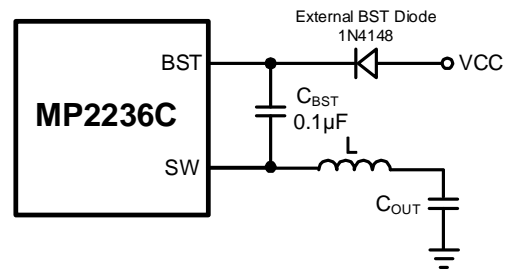
The  $C_{OUT}$  characteristics also affect the stability of the regulation system. The MP2236C can be optimized for a wide range of capacitances and ESR values.

### External Bootstrap (BST) Diode

An external BST diode can enhance the efficiency of the regulator, given the following conditions:

- $V_{IN}$  is below 5V
- $V_{OUT}$  is 3.3V
- Duty cycle is high:  $D = \frac{V_{OUT}}{V_{IN}} > 65\%$

If these conditions are met, add an external BST diode from VCC to BST (see Figure 4).



**Figure 4: Optional External BST Diode to Enhance Efficiency**

The recommended external BST diode is 1N4148, and the recommended  $C_{BST}$  value is 0.1µF.

### Design Example

Table 3 shows a design example following the application guidelines for the specifications below.

**Table 2: Design Example**

$V_{IN}$	$V_{OUT}$	$I_{OUT}$
12V	1V	6A

For the detailed application schematics, see Figure 6, Figure 7, Figure 8, Figure 9, and Figure 10 on pages 17 and 18. For the typical performance and circuit waveforms, see the Typical Performance Characteristics section on page 8. For more device applications, refer to the related evaluation board datasheets.

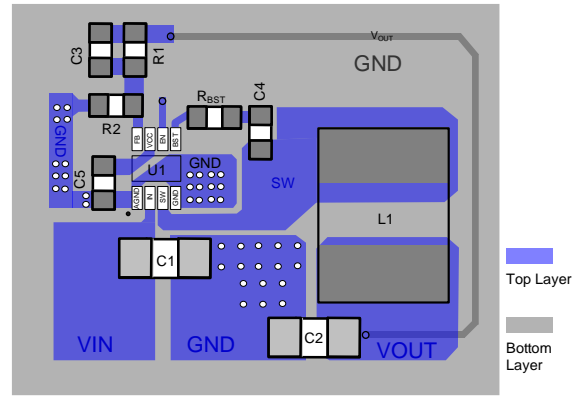
**PCB Layout Guidelines** <sup>(9)</sup>

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 5 and follow the guidelines below:

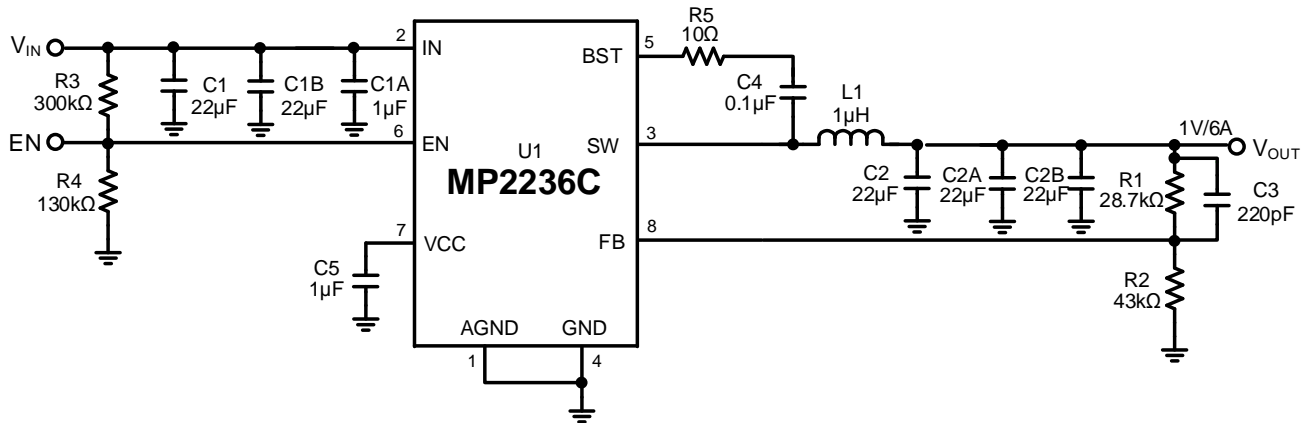
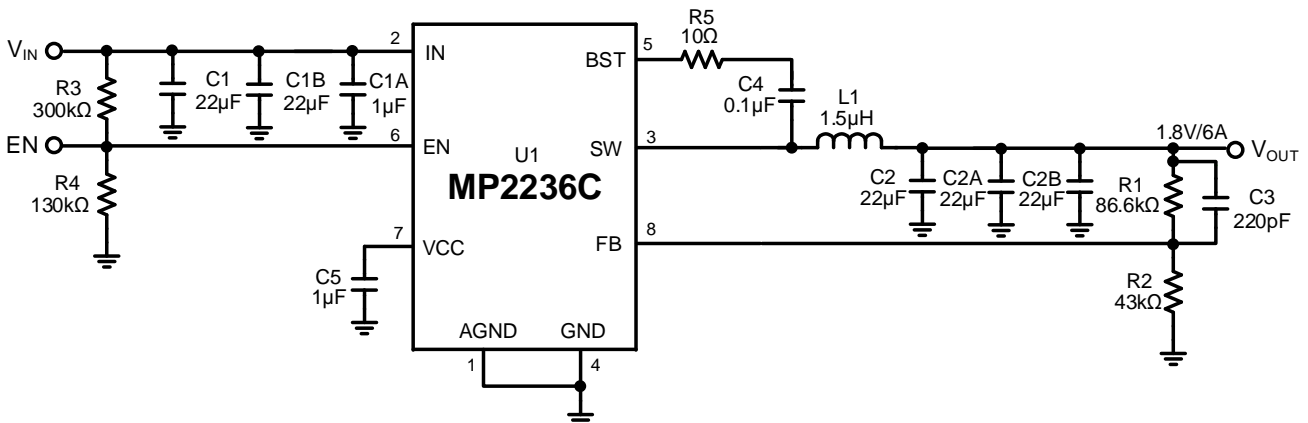
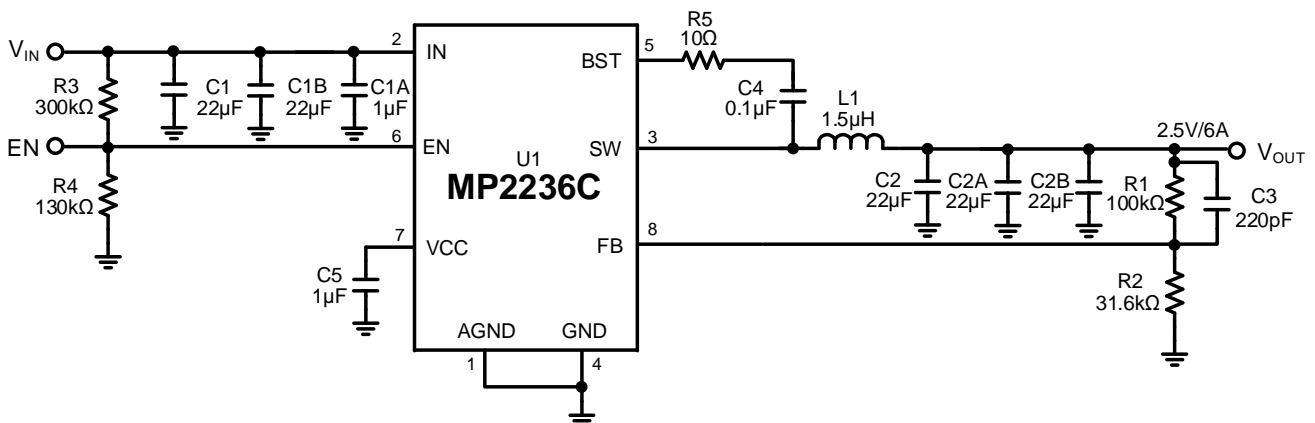
1. Connect the input ground to GND using the shortest and widest trace possible.
2. Connect  $C_{IN}$  to IN using the shortest and widest trace possible.
3. Ensure that all FB connections are short and direct.
4. Place the FB resistors and compensation components as close to the chip as possible.
5. Route SW away from sensitive analog areas, such as VOUT.
6. Connect AGND to PGND using the shortest and widest trace possible.

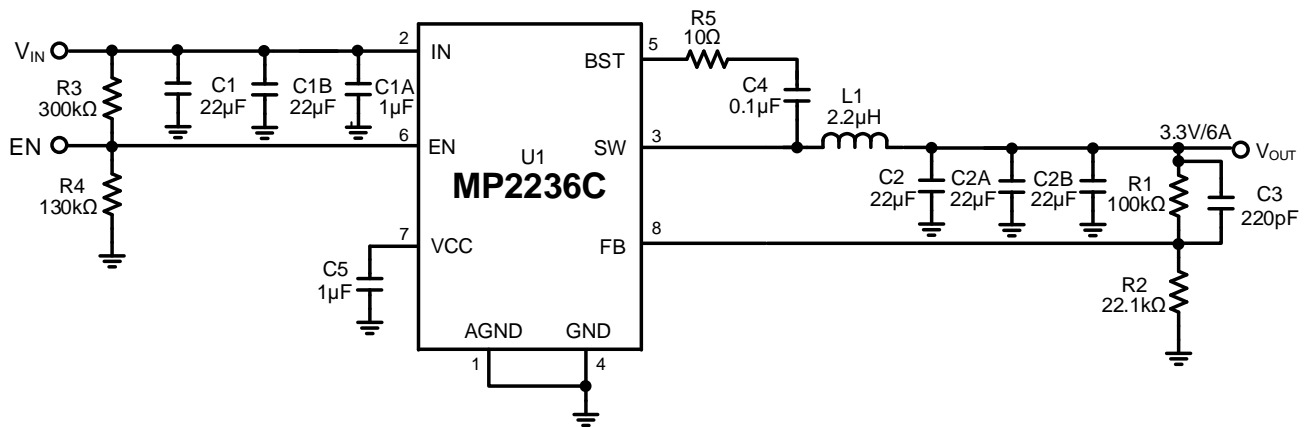
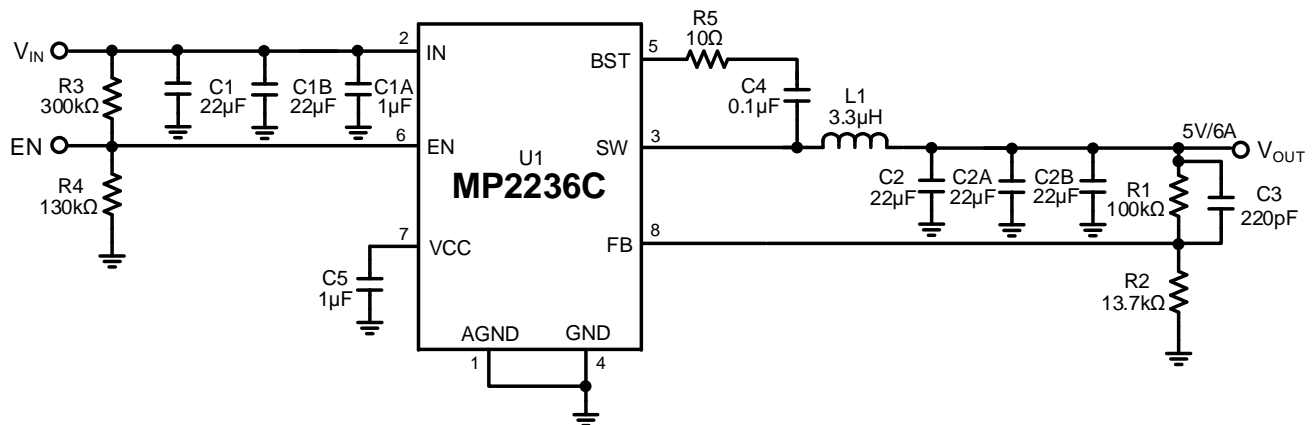
**Note:**

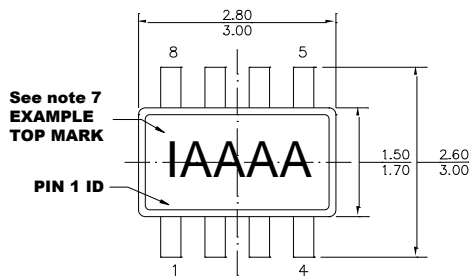
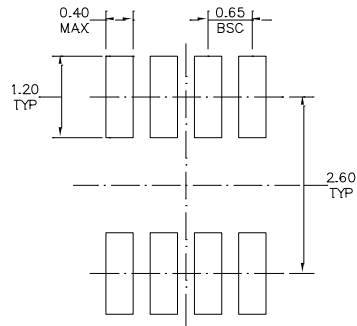
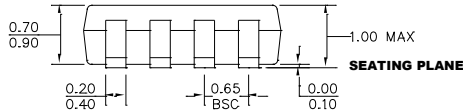
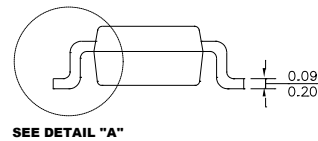
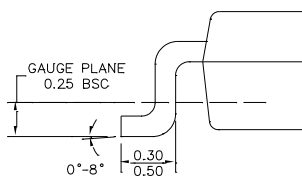
- 9) The recommended layout is based on the Typical Application Circuits shown in Figure 6, Figure 7, Figure 8, Figure 9, and Figure 10 on pages 17 and 18.


**Figure 5: Recommended PCB Layout**

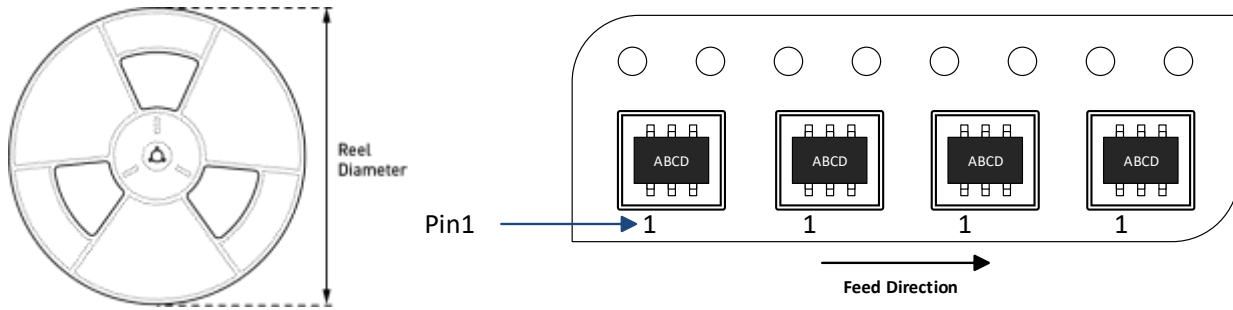


**TYPICAL APPLICATION CIRCUITS**

**Figure 6: Typical Application Circuit (12V  $V_{IN}$ , 1V/6A Output)**

**Figure 7: Typical Application Circuit (12V  $V_{IN}$ , 1.8V/6A Output)**

**Figure 8: Typical Application Circuit (12V  $V_{IN}$ , 2.5V/6A Output)**

**TYPICAL APPLICATION CIRCUITS (continued)**

**Figure 9: Typical Application Circuit (12V  $V_{IN}$ , 3.3V/6A Output)**

**Figure 10: Typical Application Circuit (12V  $V_{IN}$ , 5V/6A Output)**

**PACKAGE INFORMATION**
**TSOT23-8**

**TOP VIEW**

**RECOMMENDED LAND PATTERN**

**FRONT VIEW**

**SIDE VIEW**

**DETAIL "A"**
**NOTE:**

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
- 5) JEDEC REFERENCE IS MO-193, VARIATION BA.
- 6) DRAWING IS NOT TO SCALE.
- 7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

**CARRIER INFORMATION**


Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP2236CGJ-Z	TSOT23-8	3000	N/A	N/A	7in	8mm	4mm

## REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	3/16/2022	Initial Release	-

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