MPQ2169A

6V, Dual 1.4A/1.4A or 2A/0.8A, Low I_Q, Synchronous Buck with PG and SS, AEC-Q100 Qualified

DESCRIPTION

The MPQ2169A is an internally compensated, dual, PWM, synchronous, step-down regulator that operates from a 2.7V to 6V input and generates an output voltage as low as 0.6V. The MPQ2169A can be configured as a 1.4A/1.4A or 2A/0.8A output current regulator, and is ideal for powering portable equipment that runs on a single-cell Li-ion battery due to its low 65µA quiescent current.

The MPQ2169A integrates dual, 60mΩ high-side switches and 25mΩ synchronous rectifiers to achieve high efficiency without an external Schottky diode. The MPQ2169A offers peak current mode control and internal compensation, and is capable of low-dropout configurations. Both channels can operate at 100% duty cycle.

Full protection features include cycle-by-cycle current limit and thermal shutdown.

The MPQ2169A requires a minimal number of readily available, standard external components, and is available in a QFN-18 (2.5mmx3.5mm) package.

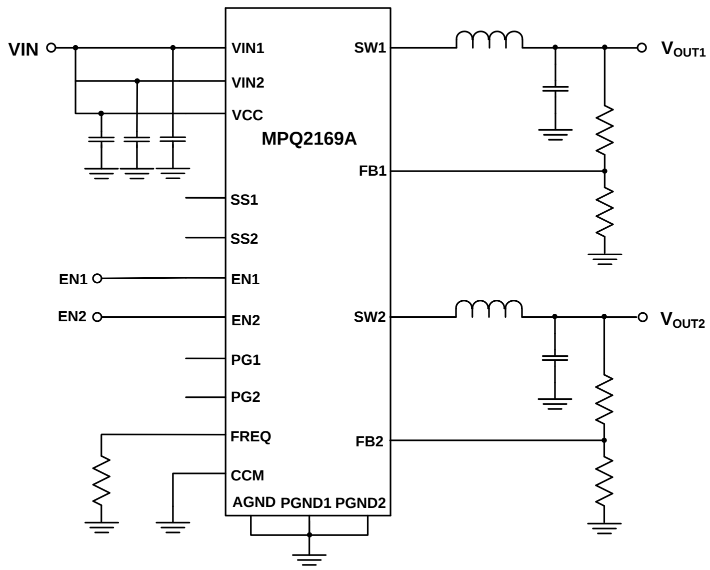
FEATURES

- 2.7V to 6V Operating Input Range
- 1.4A/1.4A or 2A/0.8A Continuous Current
- 60mΩ/25mΩ $R_{DS(ON)}$
- Configured Frequency Up to 3MHz
- External Sync Clock Up to 3MHz
- 180° Phase-Shift Operation
- Power Good (PG) Indicators
- External Soft Start (SS) and Track
- Adjustable Advanced Asynchronous Mode (AAM) or Forced Continuous Conduction Mode (FCCM)
- Peak Efficiency >90%
- Output Adjustable from 0.6V to 5.5V
- 100% Duty Cycle Operation
- 65µA Quiescent Current
- Cycle-by-Cycle Over-Current Protection (OCP)
- Short-Circuit Protection (SCP) with Hiccup Mode and Valley Current Detection
- Thermal Shutdown
- Available in a QFN-18 (2.5mmx3.5mm) Package
- Available in Wettable Flank Package
- Available in AEC-Q100 Grade 1

APPLICATIONS

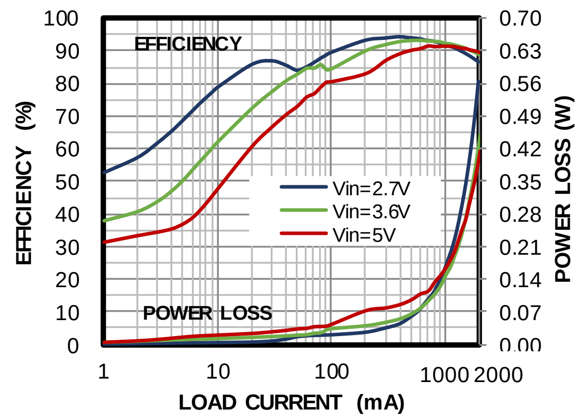
- Automotive Infotainment
- Automotive Clusters
- Automotive Telematics
- Battery-Powered Devices
- Portable Instruments

TYPICAL APPLICATION



Efficiency vs. Load Current vs. Power Loss

V_{OUT1} = 1.8V, L1 = 1.5µH, f_{SW} = 2.25MHz, AAM, one channel on



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating**
MPQ2169AGRHE-AEC1***	QFN-18 (2.5mmx3.5mm)	*See Below*	1

* For Tape & Reel, add suffix –Z (e.g. MPQ2169AGRHE-AEC1–Z).

** Moisture Sensitivity Level Rating

*** Wettable flank.

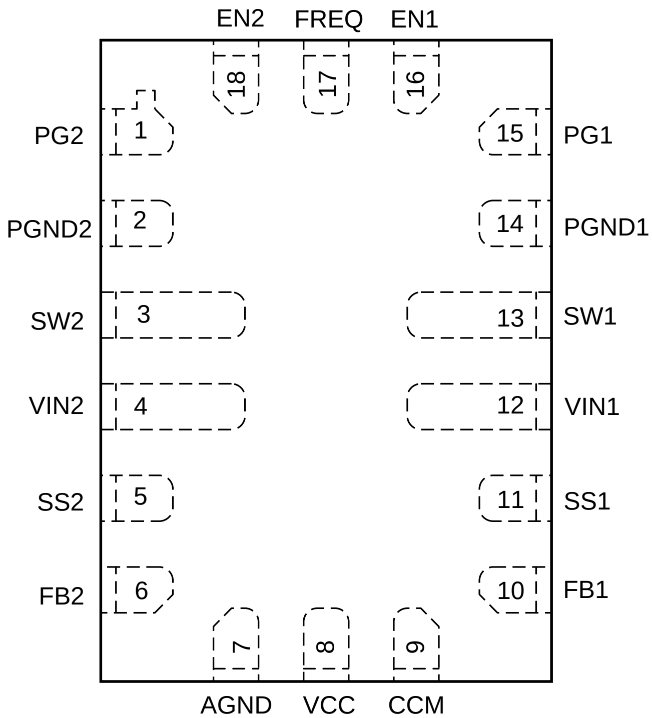
TOP MARKING

BLX
YWW
LLL

BLX: Product code of MPQ2169AGRHE-AEC1
Y: Year code
WW: Week code
LLL: Lot number

PACKAGE REFERENCE

TOP VIEW



QFN-18 (2.5mmx3.5mm)

PIN FUNCTIONS

Pin #	Name	Description
1	PG2	**Channel 2 power good.** The output of PG2 is an open drain. A pull-up resistor to the power source is required if this pin used. PG2 is pulled high when V_{FB2} reaches 90% of V_{REF}, and is pulled low to GND when V_{FB2} drops to 82% of V_{REF}.
2	PGND2	**Channel 2 power ground.** Connect PGND2 with larger copper areas to the negative terminals of the input and output capacitors. PGND2 must be connected to PGND1 externally on the board.
3	SW2	**Switch-node connection to the inductor for channel 2.** SW2 connects to the internal high- and low-side power MOSFET switches of the channel 2 buck.
4	VIN2	**Channel 2 input supply.** Place a decoupling capacitor to ground, close to VIN2, to reduce switching spikes.
5	SS2	**Channel 2 soft start.** Place a capacitor from SS2 to GND to set the soft-start time externally. Floating this pin activates the internal default 0.5ms soft-start setting.
6	FB2	**Channel 2 feedback.** FB2 is the input to the error amplifier of channel 2. An external resistive divider connects FB2 between the output and ground. The voltage on FB2 is compared with the internal 0.6V reference to set the regulation voltage for channel 2.
7	AGND	**Analog ground.** Connect AGND to PGND1 and PGND2 externally on the board.
8	VCC	**Power supply to the internal circuits.** Decouple VCC with a 0.1µF to 1µF capacitor between VCC and AGND. Connect VIN1, VIN2, and VCC together externally. It is not recommended to power them from a separated power supply.
9	CCM	**AAM or FCCM control.** Pull CCM high to enter forced CCM (FCCM) mode. Pull CCM low to enter AAM mode at light load. Do not float CCM.
10	FB1	**Channel 1 feedback.** FB1 is the input to the error amplifier of channel 1. An external resistor divider connects FB1 between the output and GND. The voltage on FB1 is compared with the internal 0.6V reference to set the regulation voltage for channel 1.
11	SS1	**Channel 1 soft start.** Place a capacitor from SS1 to GND to set the soft-start time externally. Floating this pin activates the internal default 0.5ms soft-start setting.
12	VIN1	**Channel 1 input supply.** Place a decoupling capacitor to ground, close to VIN1, to reduce switching spikes.
13	SW1	**Switch-node connection to the inductor for channel 1.** SW1 connects to the internal high- and low-side power MOSFET switches of the channel 1 buck.
14	PGND1	**Channel 1 power ground.** Connect PGND1 to the negative terminals of the input and output capacitors with large copper areas. PGND1 must be connected to PGND2 externally on the board.
15	PG1	**Channel 1 power good.** The output of PG1 is an open drain. A pull-up resistor to the power source is required if this pin used. PG1 is pulled high when V_{FB1} reaches 90% of V_{REF}, and is pulled low to GND if V_{FB1} drops to 82% of V_{REF}.
16	EN1	**Channel 1 enable control.** Pull EN1 below the specified threshold (0.4V) to shut down the chip. Pull EN above the threshold (1.6V) to enable the chip. Do not float EN1.
17	FREQ	**Frequency set.** Connect a resistor to GND to set the switching frequency. The switching frequency can be synchronized by an external clock via FREQ.
18	EN2	**Channel 2 enable control.** Pull EN2 below the specified threshold (0.4V) to shut down the chip. Pull EN above the threshold (1.6V) to enable the chip. Do not float EN2.

ABSOLUTE MAXIMUM RATINGS [1]

Supply voltage (V_{IN}) 6.5V
V_{SW} .... -0.3V to V_{IN} + 0.3V
All other pins .... -0.3V to +6.5V
Junction temperature .... 150°C
Lead temperature .... 260°C
Storage temperature .... -65°C to +150°C
Continuous power dissipation (T_A = 25°C) [2] [5]
QFN-18 (2.5mmx3.5mm) 3.6W

ESD Rating

Human body model (HBM) .... ±2kV
Charged device model (CDM) .... ±750V

Recommended Operating Conditions

Supply voltage (V_{IN}) .... 2.7V to 6V
Output voltage (V_{OUT}) .... 0.6V to 5.5V
Operating junction temp (T_J)........................ .... -40°C to +125°C [3]

Thermal Resistance

	θ_{JA}	θ_{JC}	
QFN-18 (2.5mmx3.5mm)			
JESD51-7 [4]	50	12	°C/W
EV2169A-RH-00A [5]	34.8	2.7	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Operating devices at junction temperatures greater than 125°C is possible; contact MPS for details.
4) Measured on JESD51-7, 4-layer PCB.
5) Measured on MPS standard EVB, 6.35cmx6.35cm, 2oz thick copper, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_J = 25°C.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Quiescent supply current	I_Q	V_{IN} = 5V, V_{EN} = 2V, V_{FB} = 0.65V, no switching		65	90	μA
Shutdown current	I_{SHDN}	V_{EN} = 0V, CCM = GND, T_J = 25°C		0	0.2	μA
		V_{EN} = 0V, CCM=GND, T_J = -40°C to +85°C (6)		0	5	μA
		V_{EN} = 0V, CCM = GND, T_J = 85°C to 125°C			8	μA
Input under-voltage lockout threshold	V_{UVLO}	VIN1, VIN2, VCC rising		2.4	2.55	V
Input under-voltage lockout hysteresis	V_{UVLO_HYS}	VIN1, VIN2, VCC UVLO Hysteresis		230		mV
Regulated FB voltage	V_{FB}	T_J = 25°C	0.593	0.600	0.607	V
		T_J = -40°C to +125°C	0.588	0.600	0.612	V
FB input current	I_{FB}	V_{FB} = 0.65V		0	50	nA
EN high threshold	V_{EN_H}		1.6			V
EN low threshold	V_{EN_L}				0.4	V
EN input current	I_{EN}	V_{EN} = 2V		0	0.1	μA
		V_{EN} = 0V		0	0.1	
HS switch on resistance	R_{DSON_P}	V_{IN} = 5V		60	90	mΩ
LS switch on resistance	R_{DSON_N}	V_{IN} = 5V		25	45	mΩ
SW leakage current	I_{SW_LK}	V_{EN} = 0V, V_{IN} = 6V, V_{SW} = 0V and 6V, T_J = 25°C	-1	0	+1	μA
HS switch current limit (6)	I_{HS_LIMIT}	Sourcing	3.0	4.0	6.2	A
LS valley current limit (6)	I_{VALLEY}			3.4		A
LS switch current limit	I_{LS_LIMIT}	Sinking, CCM	1			A
Oscillator frequency accuracy	f_{SW}	R_{FREQ} = 665kΩ	298	350	402	kHz
		R_{FREQ} = 200kΩ	850	1000	1150	kHz
		R_{FREQ} = 51kΩ	2700	3000	3300	kHz
Sync frequency range	f_{SYNC}		0.35		3	MHz
Phase shift				180		°
Minimum on time (6)	t_{ON_MIN}			55		ns
Minimum off time (6)	t_{OFF_MIN}			50		ns
Maximum duty cycle	D_{MAX}			100		%
Thermal shutdown threshold (6)	T_D			175		°C
Thermal shutdown hysteresis (6)	T_{D_HYS}			40		°C
Soft-start charging current	I_{SS}	V_{SS} = 0V	2	3.2	5	μA
Power good rising threshold	$PGOOD_{VTH-HI}$		0.85	0.9	0.95	V_{FB}
Power good falling threshold	$PGOOD_{VTH-LO}$		0.77	0.82	0.87	V_{FB}
Power good threshold hystersis	$PGOOD_{Vth-Hys}$			0.08		V_{FB}
Power good rising delay	t_{PGOOD_R}			30		μs
Power good falling delay	t_{PGOOD_F}			40		μs
CCM on threshold			1.6			V
CCM off threshold					0.4	V

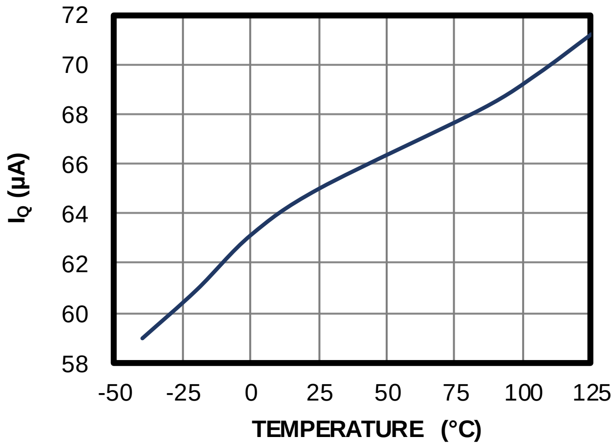
Note:

6) Not tested in production. Guaranteed by design and characterization.

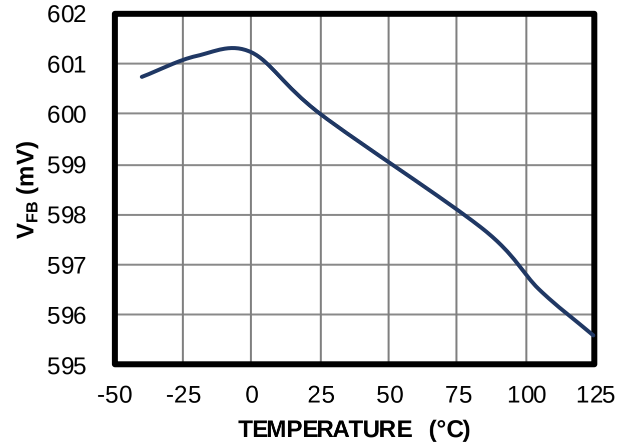
TYPICAL CHARACTERISTICS

V_{IN} = 5V, T_J = 25°C, unless otherwise noted.

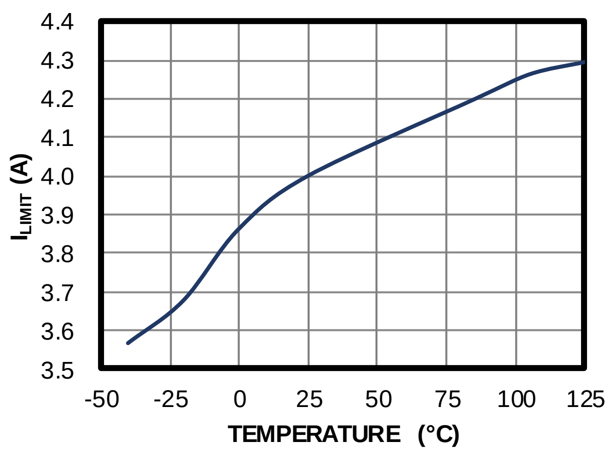
I_Q vs. Temperature



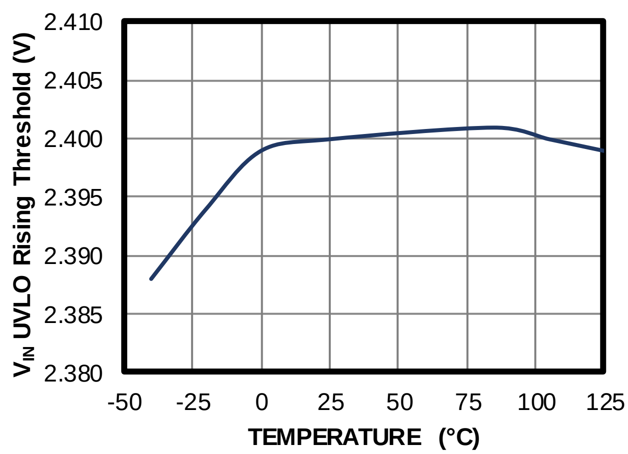
V_{FB} vs. Temperature



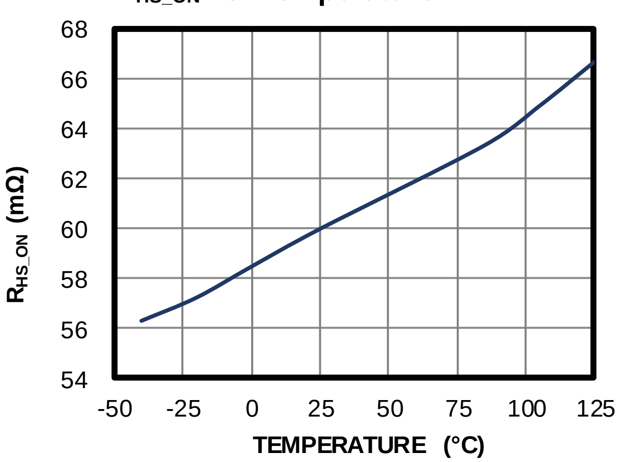
I_{LIMIT} vs. Temperature



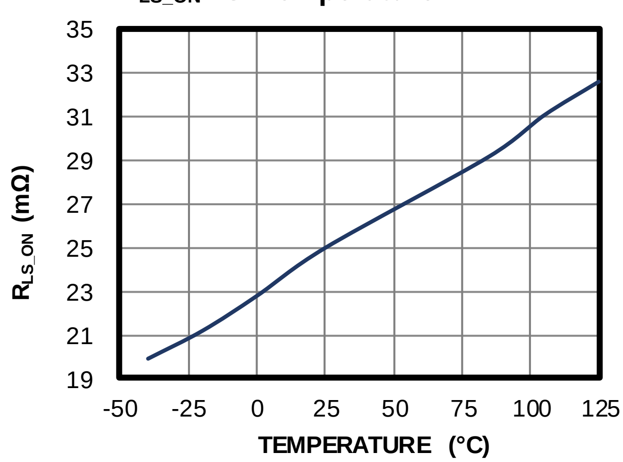
V_{IN} UVLO Rising Threshold vs. Temperature



R_{HS_ON} vs. Temperature



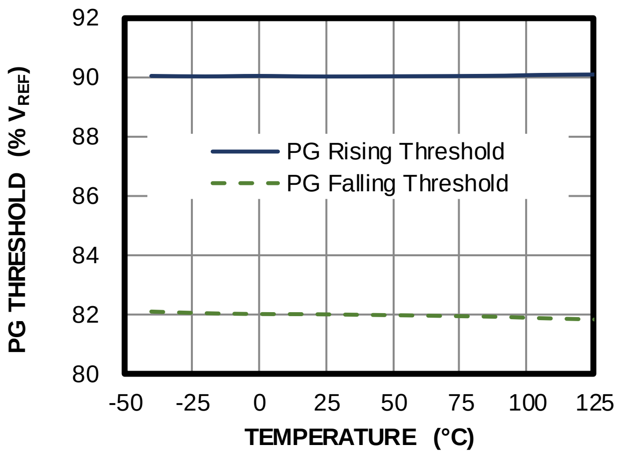
R_{LS_ON} vs. Temperature



TYPICAL CHARACTERISTICS *(continued)*

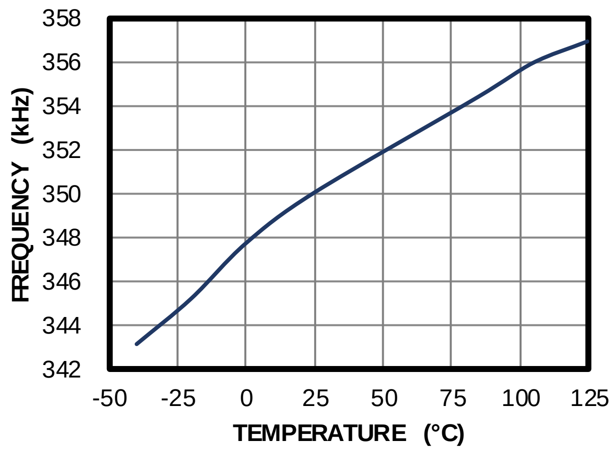
V_{IN} = 5V, T_J = 25°C, unless otherwise noted.

PG Rising/Falling Threshold vs. Temperature



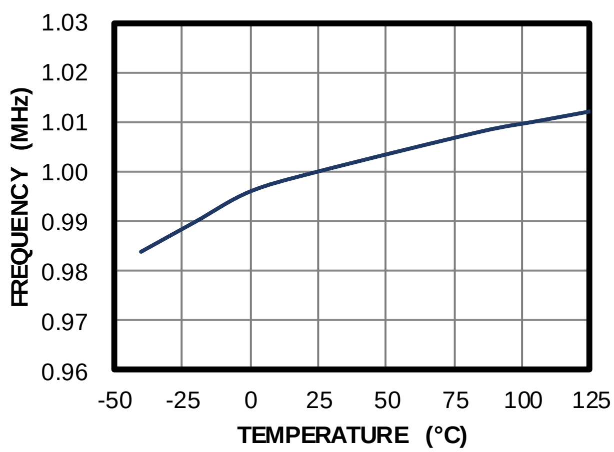
Frequency vs. Temperature

f_{SW} = 350kHz



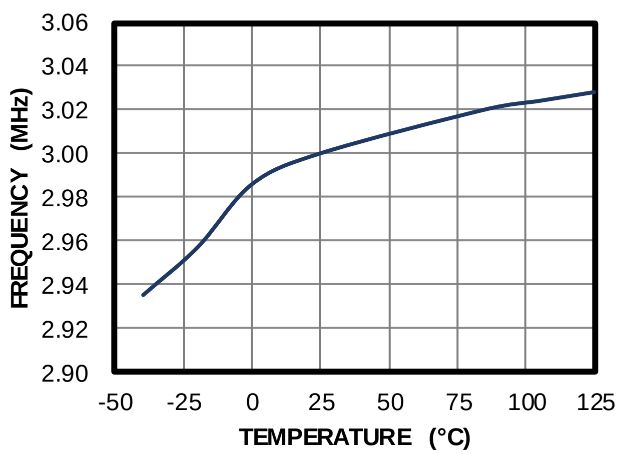
Frequency vs. Temperature

f_{SW} = 1MHz



Frequency vs. Temperature

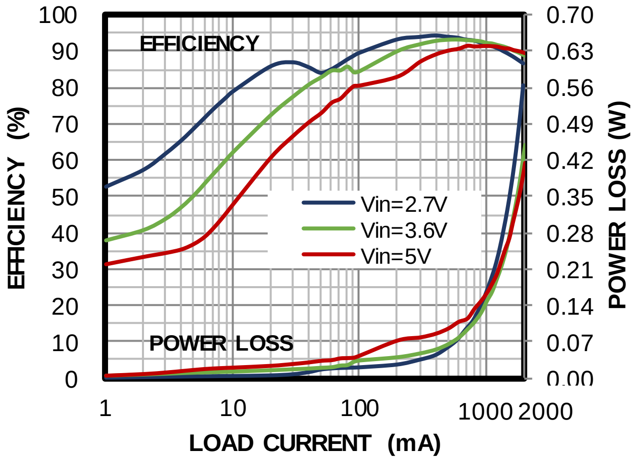
f_{SW} = 3MHz



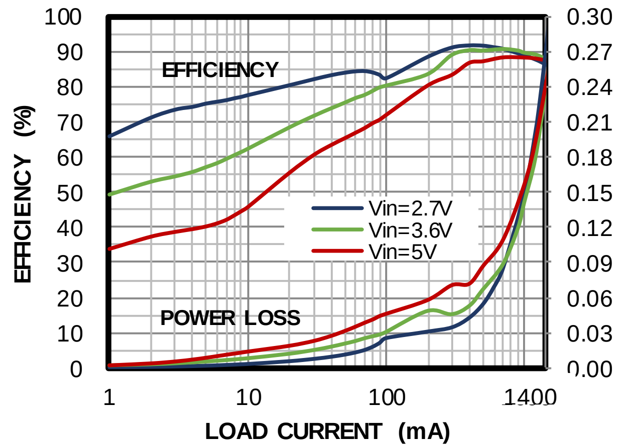
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L1 = L2 = 1.5µH, f_{SW} = 2.25MHz, T_A = 25°C, unless otherwise noted.

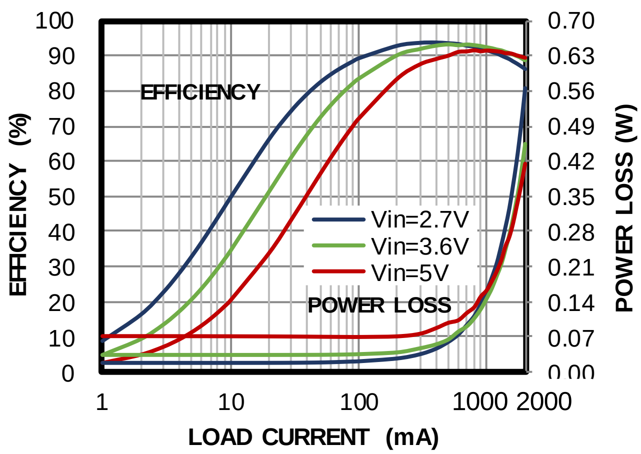
Efficiency vs. Load Current
V_{OUT1} = 1.8V, AAM, one channel on



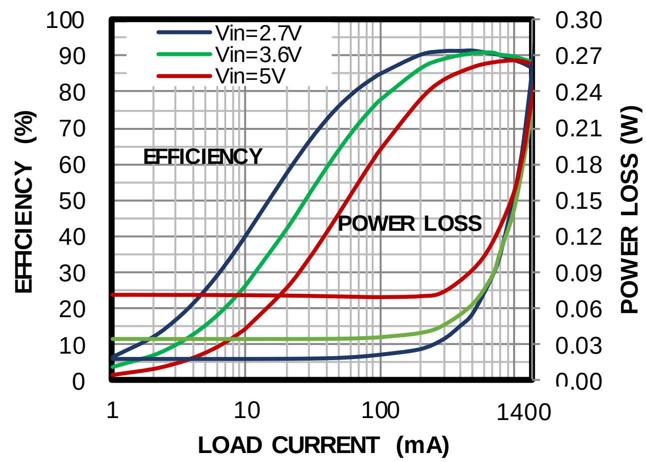
Efficiency vs. Load Current
V_{OUT2} = 1.2V, AAM, one channel on



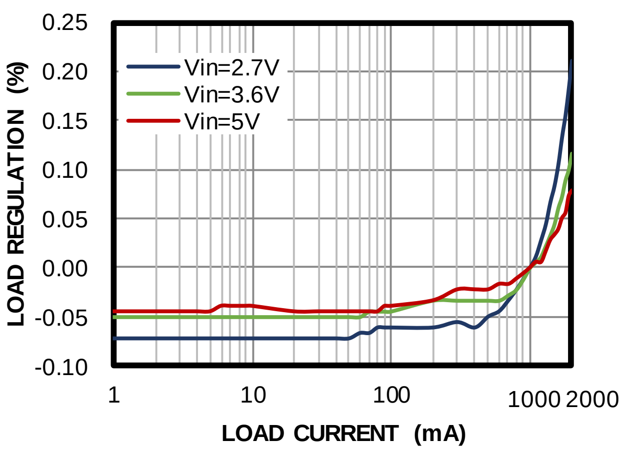
Efficiency vs. Load Current
V_{OUT1} = 1.8V, FCCM, one channel on



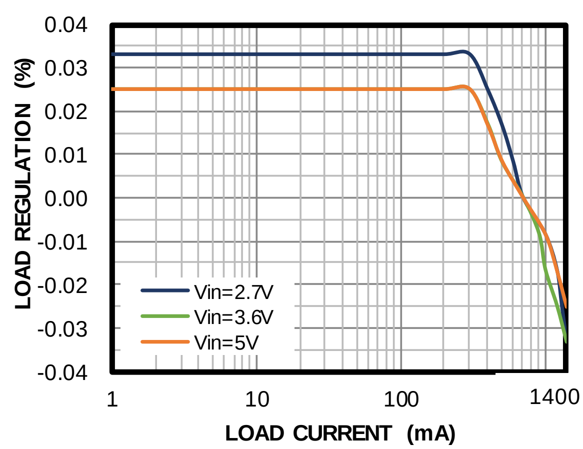
Efficiency vs. Load Current
V_{OUT2} = 1.2V, FCCM, one channel on



Load Regulation
V_{OUT1} = 1.8V, AAM, one channel on



Load Regulation
V_{OUT2} = 1.2V, AAM, one channel on

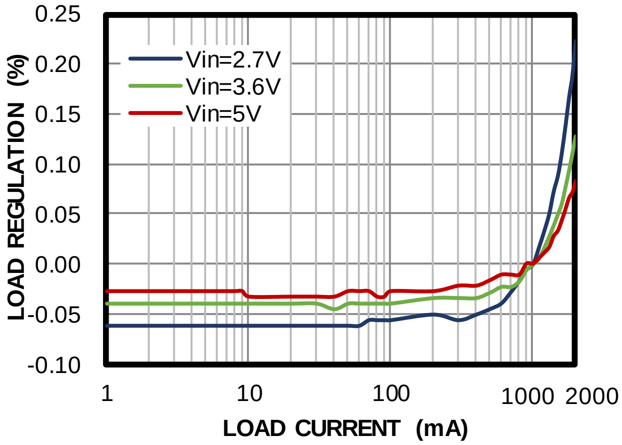


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L1 = L2 = 1.5µH, f_{SW} = 2.25MHz, T_A = 25°C, unless otherwise noted.

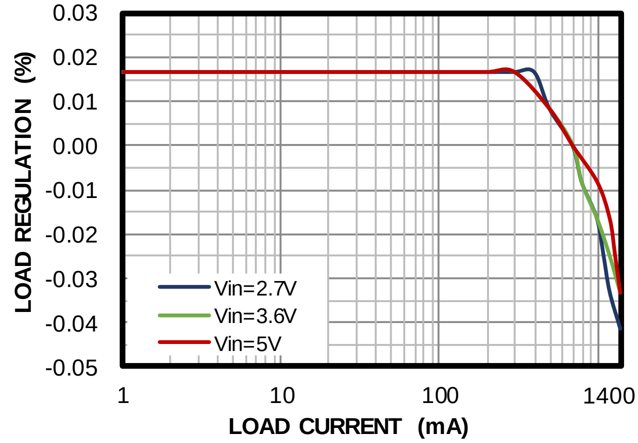
Load Regulation

V_{OUT1} = 1.8V, FCCM, one channel on



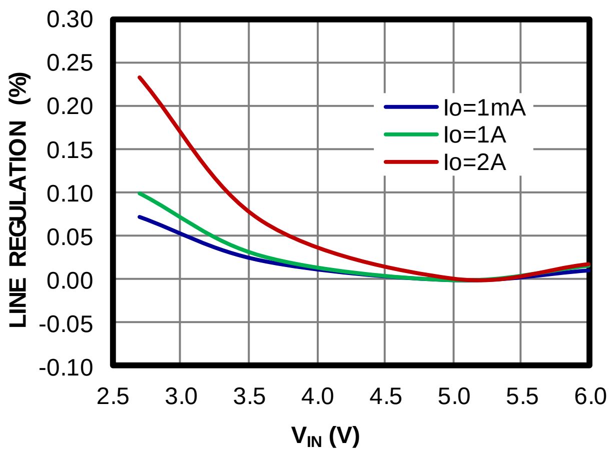
Load Regulation

V_{OUT2} = 1.2V, FCCM, one channel on



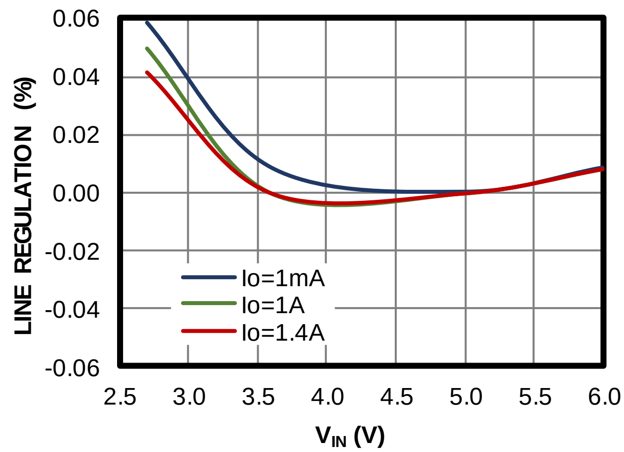
Line Regulation

V_{OUT1} = 1.8V, AAM, one channel on



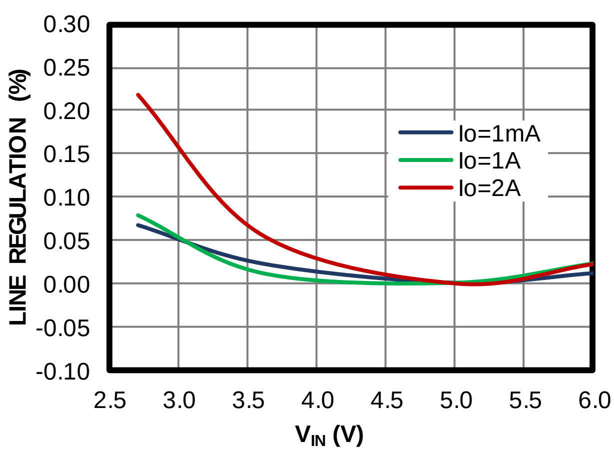
Line Regulation

V_{OUT2} = 1.2V, AAM, one channel on



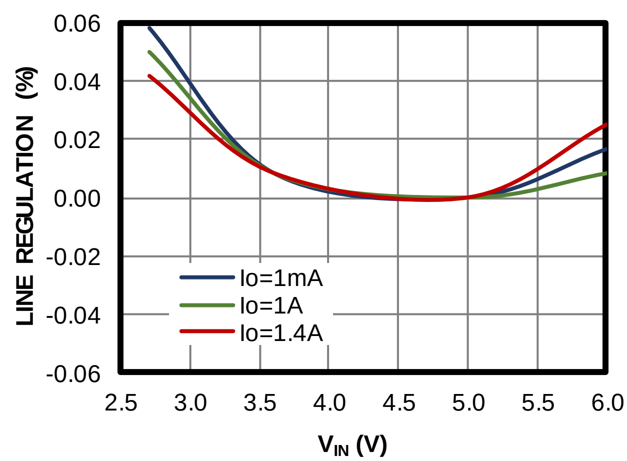
Line Regulation

V_{OUT1} = 1.8V, FCCM, one channel on



Line Regulation

V_{OUT2} = 1.2V, FCCM, one channel on

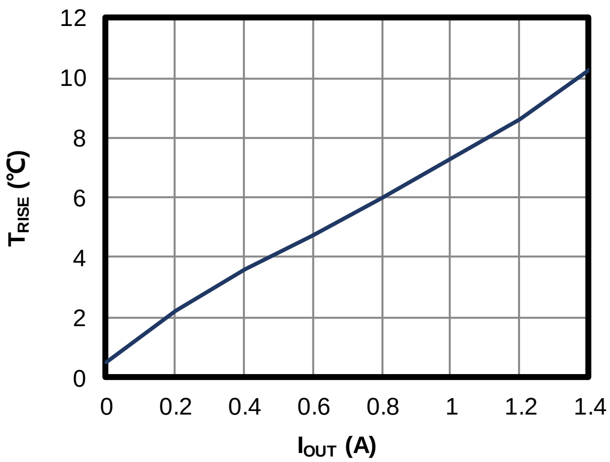


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L1 = L2 = 1.5µH, f_{SW} = 2.25MHz, T_A = 25°C, unless otherwise noted.

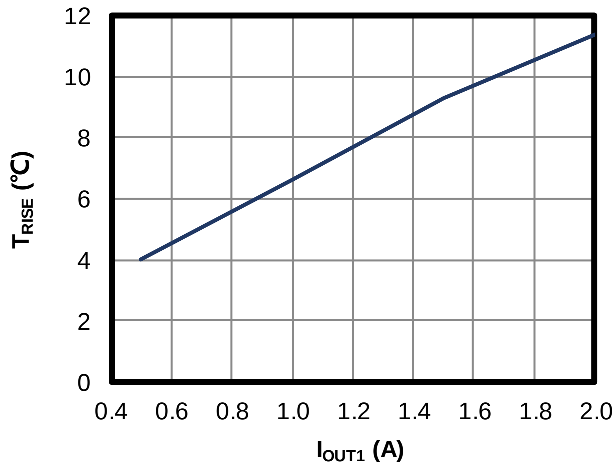
Case Thermal Rise

V_{IN} = 5V, I_{OUT1} = I_{OUT2} = 0A to 1.4A, AAM, both channels on



Case Thermal Rise

V_{IN} = 5V, I_{OUT1} = 0.5A to 2A, I_{OUT2} = 0.8A, AAM, both channels on

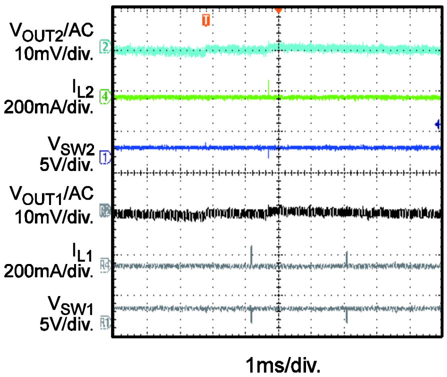


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L1 = L2 = 1.5μH, f_{SW} = 2.25MHz, T_A = 25°C, unless otherwise noted.

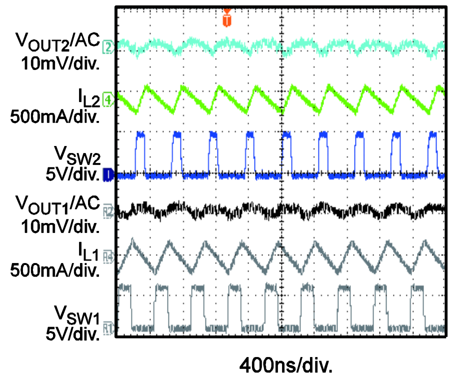
Steady State

I_{OUT1} = I_{OUT2} = 0A, AAM



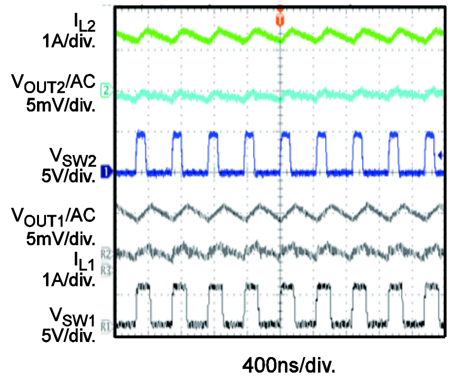
Steady State

I_{OUT1} = I_{OUT2} = 0A, forced CCM



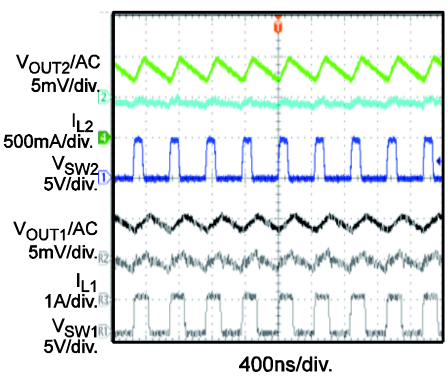
Steady State

I_{OUT1} = I_{OUT2} = 1.4A



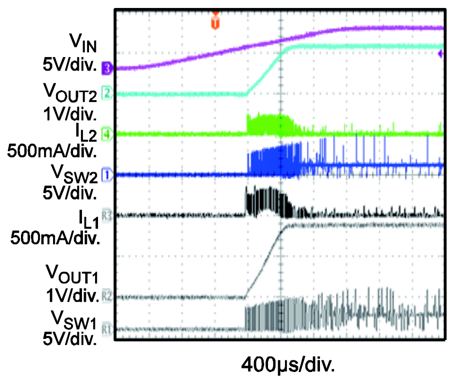
Steady State

I_{OUT1} = 2A, I_{OUT2} = 0.8A



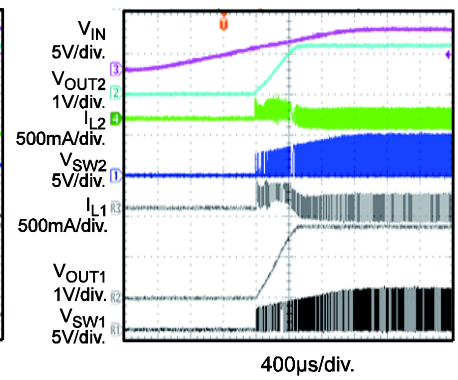
Start-Up through VIN

I_{OUT1} = I_{OUT2} = 0A, AAM



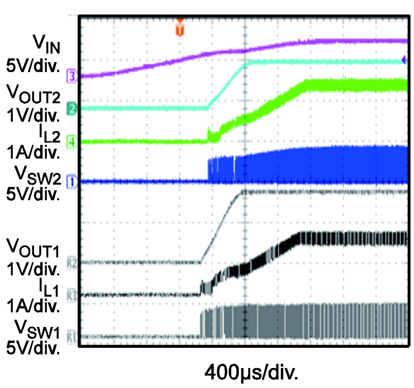
Start-Up through VIN

I_{OUT1} = I_{OUT2} = 0A, CCM



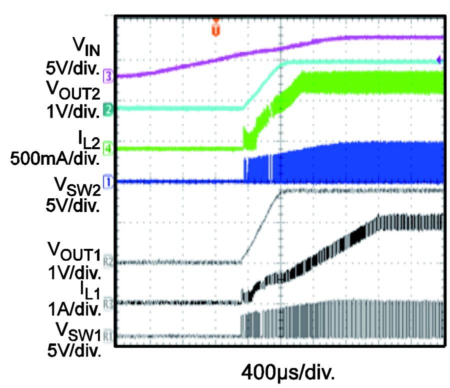
Start-Up through VIN

I_{OUT1} = I_{OUT2} = 1.4A



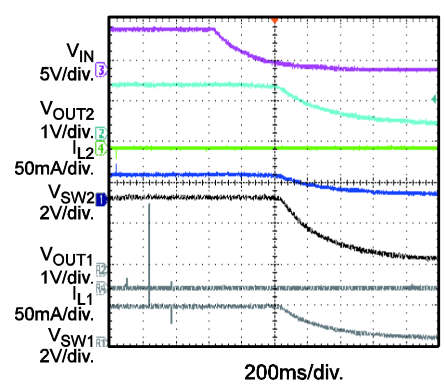
Start-Up through VIN

I_{OUT1} = 2A, I_{OUT2} = 0.8A



Shutdown through VIN

I_{OUT1} = I_{OUT2} = 0A, AAM

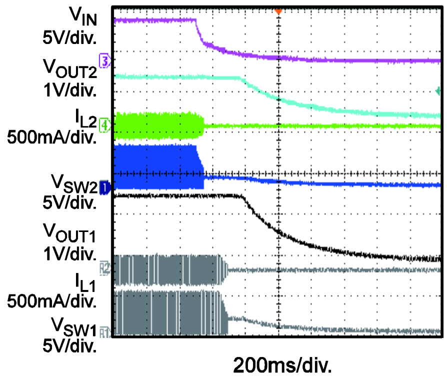


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L1 = L2 = 1.5µH, f_{SW} = 2.25MHz, T_A = 25°C, unless otherwise noted.

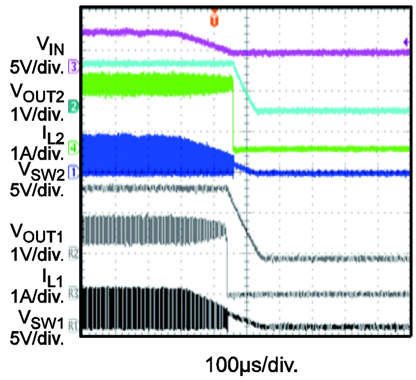
Shutdown through VIN

I_{OUT1} = I_{OUT2} = 0A, forced CCM



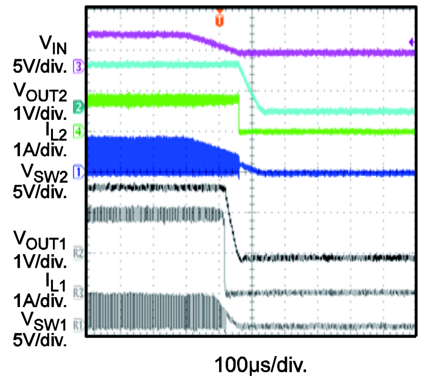
Shutdown through VIN

I_{OUT1} = I_{OUT2} = 1.4A



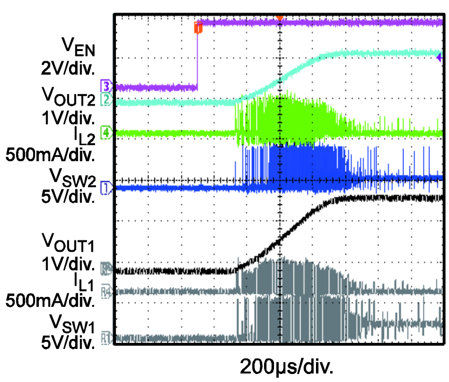
Shutdown through VIN

I_{OUT1} = 2A, I_{OUT2} = 0.8A



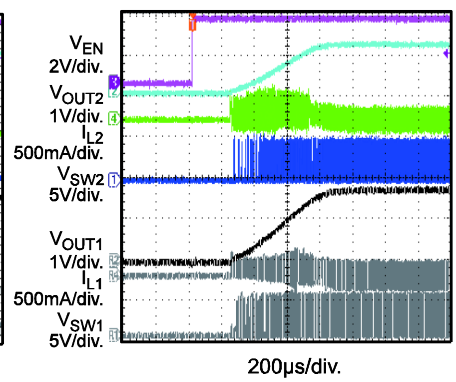
Start-Up through EN

I_{OUT1} = I_{OUT2} = 0A, AAM



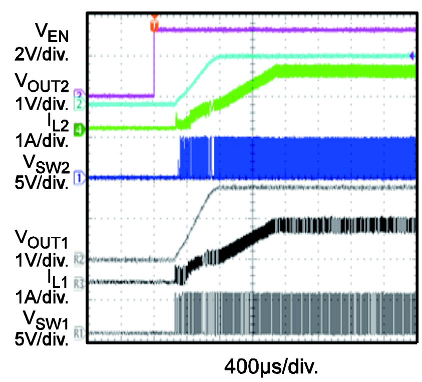
Start-Up through EN

I_{OUT1} = I_{OUT2} = 0A, forced CCM



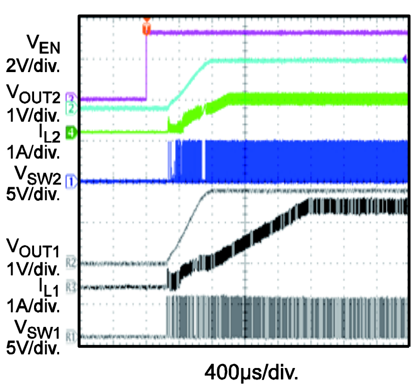
Start-Up through EN

I_{OUT1}= I_{OUT2} = 1.4A



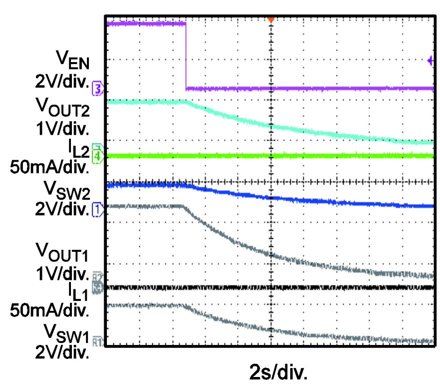
Start-Up through EN

I_{OUT1} = 2A, I_{OUT2} = 0.8A



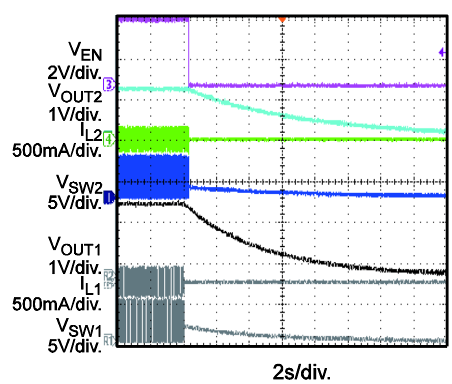
Shutdown through EN

I_{OUT1} = I_{OUT2} = 0A, AAM



Shutdown through EN

I_{OUT1} = I_{OUT2} = 0A, forced CCM

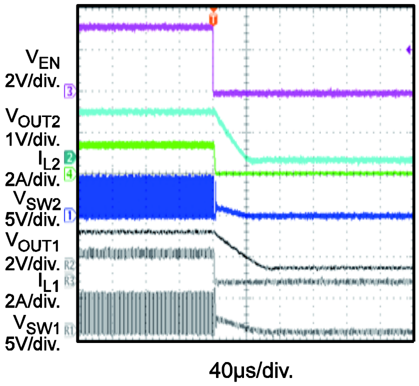


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L1 = L2 = 1.5µH, f_{SW} = 2.25MHz, T_A = 25°C, unless otherwise noted.

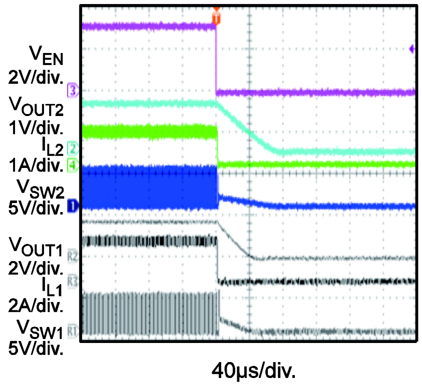
Shutdown through EN

$I_{OUT1} = I_{OUT2}$ = 1.4A



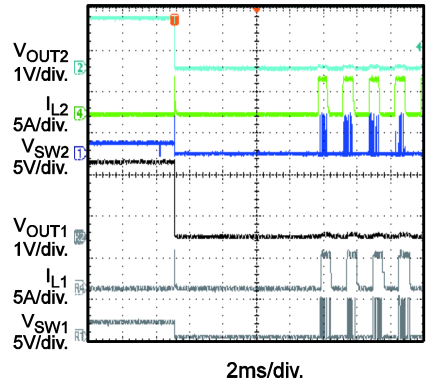
Shutdown through EN

I_{OUT1} = 2A, I_{OUT2} = 0.8A



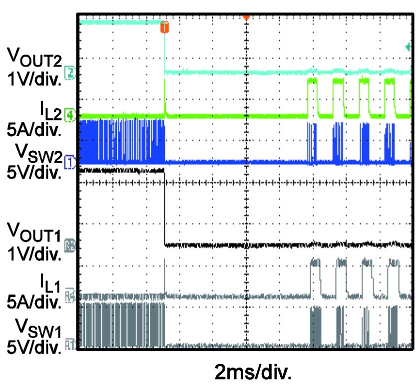
SCP Entry

$I_{OUT1} = I_{OUT2}$ = 0A, AAM



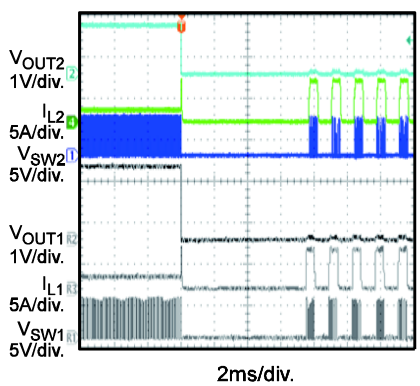
SCP Entry

$I_{OUT1} = I_{OUT2}$ = 0A, forced CCM



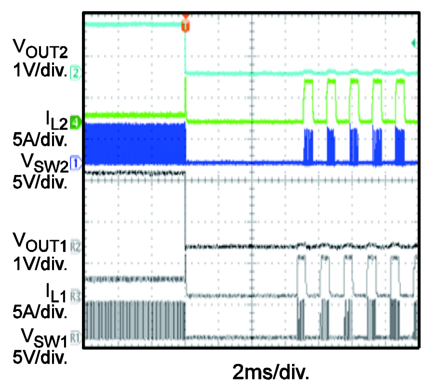
SCP Entry

$I_{OUT1} = I_{OUT2}$ = 1.4A



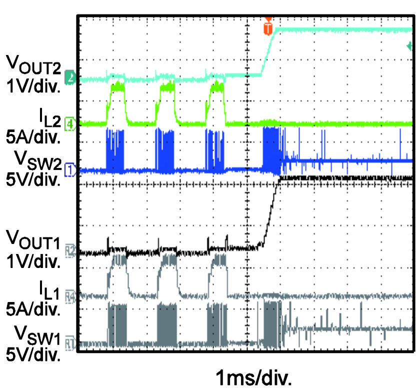
SCP Entry

I_{OUT1} = 2A, I_{OUT2} = 0.8A



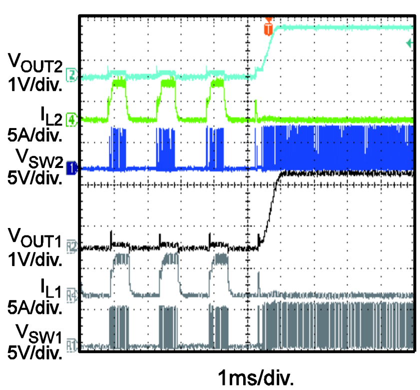
SCP Recovery

$I_{OUT1} = I_{OUT2}$ = 0A, AAM



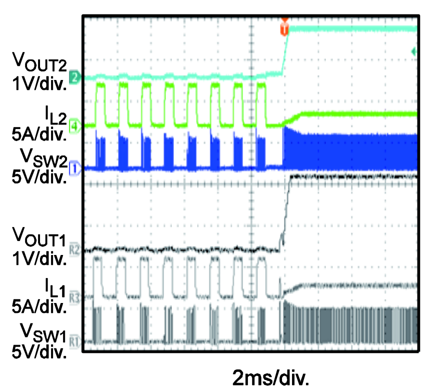
SCP Recovery

$I_{OUT1} = I_{OUT2}$ = 0A, forced CCM



SCP Recovery

$I_{OUT1} = I_{OUT2}$ = 1.4A

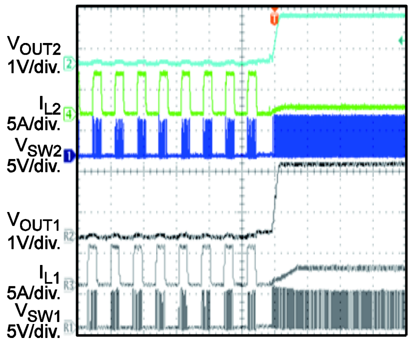


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L1 = L2 = 1.5μH, f_{SW} = 2.25MHz, T_A = 25°C, unless otherwise noted.

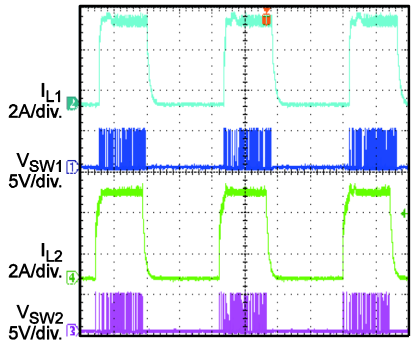
SCP Recovery

I_{OUT1} = 2A, I_{OUT2} = 0.8A



2ms/div.

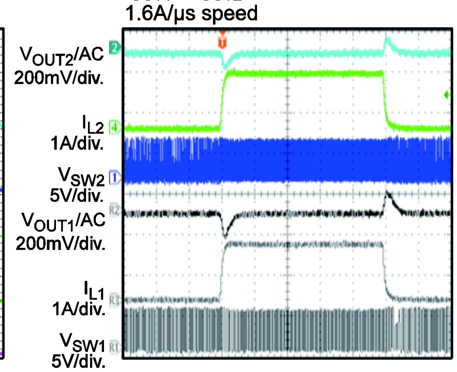
SCP Steady State



400μs/div.

Load Transient

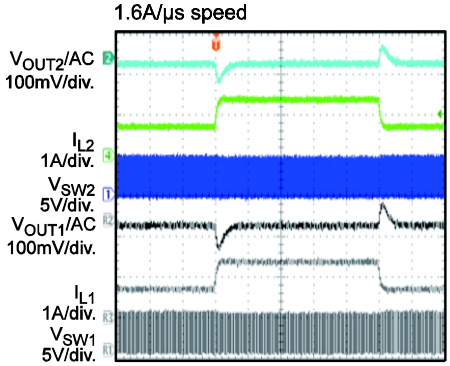
I_{OUT1} = I_{OUT2} = 0 to 1.4A, AAM 1.6A/μs speed



100μs/div.

Load Transient

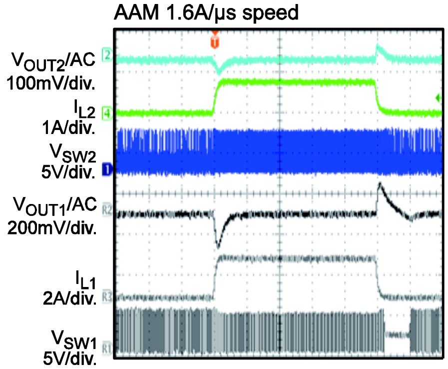
I_{OUT1} = I_{OUT2} = 0.7 to 1.4A, 1.6A/μs speed



100μs/div.

Load Transient

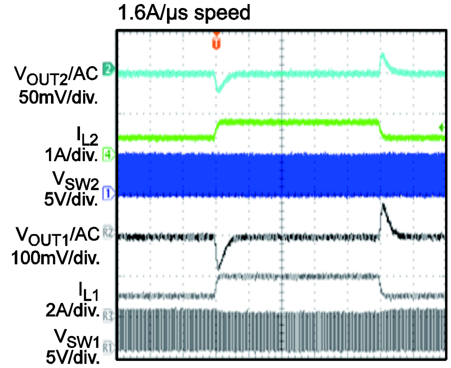
I_{OUT1} = 0 to 2A, I_{OUT2} = 0 to 0.8A, AAM 1.6A/μs speed



100μs/div.

Load Transient

I_{OUT1} = 1 to 2A, I_{OUT2} = 0.4 to 0.8A, 1.6A/μs speed

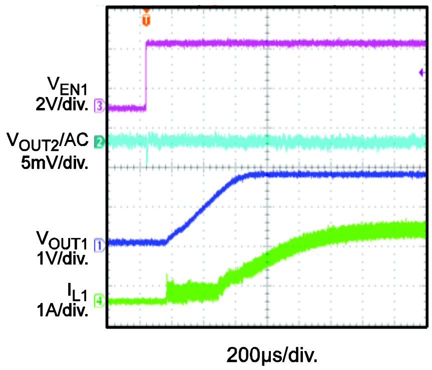


100μs/div.

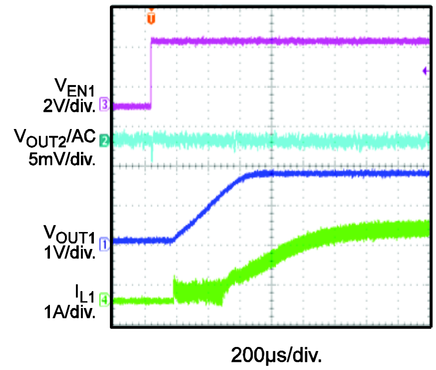
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L1 = L2 = 1.5µH, f_{SW} = 2.25MHz, T_A = 25°C, unless otherwise noted.

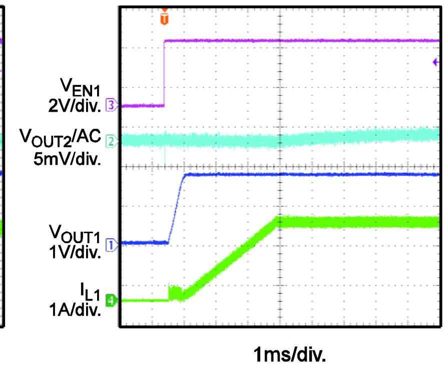
CH1 EN On, CH2 Steady State
I_{OUT1} = 1.4A, I_{OUT2} = 0A, FCCM



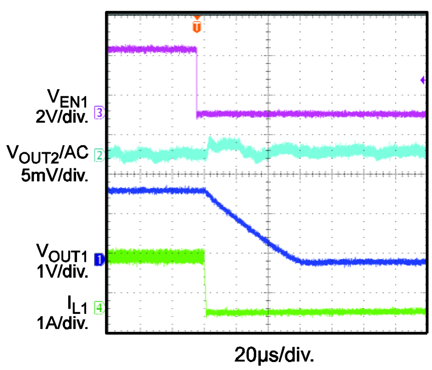
CH1 EN On, CH2 Steady State
I_{OUT1} = 1.4A, I_{OUT2} = 1.4A



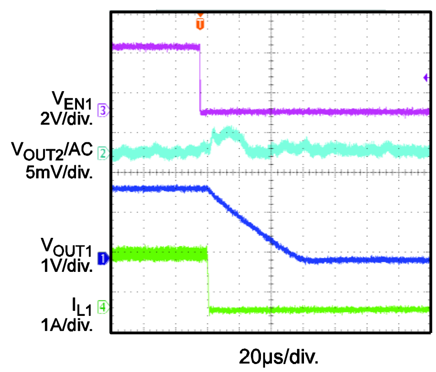
CH1 EN On, CH2 Steady State
I_{OUT1} = 2A, I_{OUT2} = 0.8A



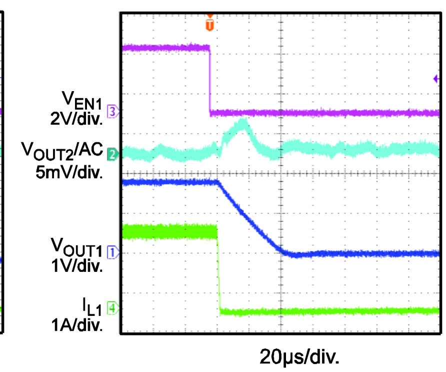
CH1 EN Off, CH2 Steady State
I_{OUT1} = 1.4A, I_{OUT2} = 0A, FCCM



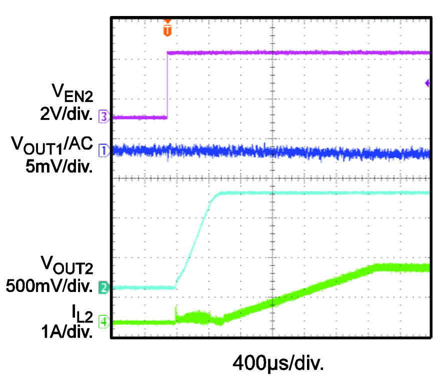
CH1 EN Off, CH2 Steady State
I_{OUT1} = 1.4A, I_{OUT2} = 1.4A



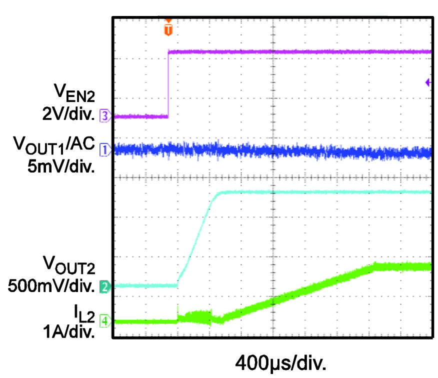
CH1 EN Off, CH2 Steady State
I_{OUT1} = 2A, I_{OUT2} = 0.8A



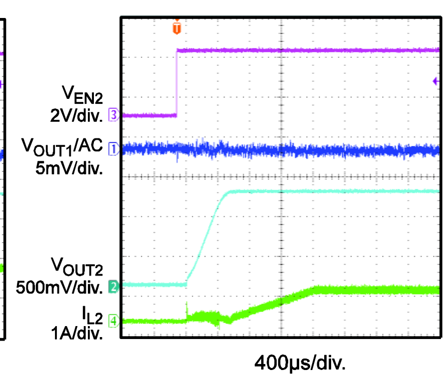
CH1 Steady State, CH2 EN On
I_{OUT1} = 0A, FCCM, I_{OUT2} = 1.4A



CH1 Steady State, CH2 EN On
I_{OUT1} = 1.4A, I_{OUT2} = 1.4A



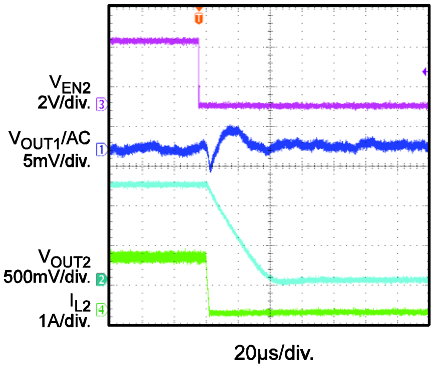
CH1 Steady State, CH2 EN On
I_{OUT1} = 2A, I_{OUT2} = 0.8A



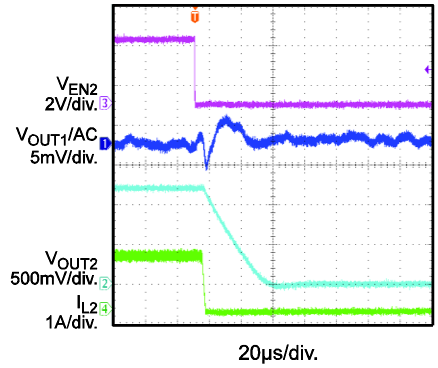
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L1 = L2 = 1.5μH, f_{SW} = 2.25MHz, T_A = 25°C, unless otherwise noted.

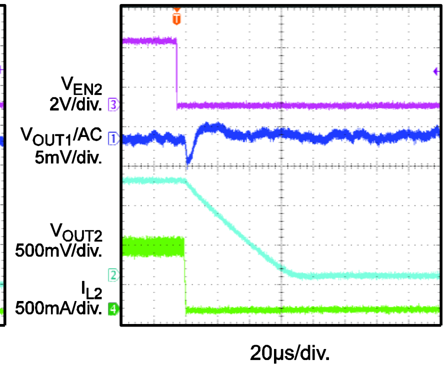
CH1 Steady State, CH2 EN Off
I_{OUT1} = 0A, FCCM, I_{OUT2} = 1.4A



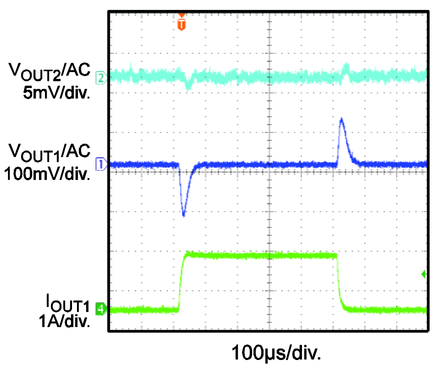
CH1 Steady State, CH2 EN Off
I_{OUT1} = 1.4A, I_{OUT2} = 1.4A



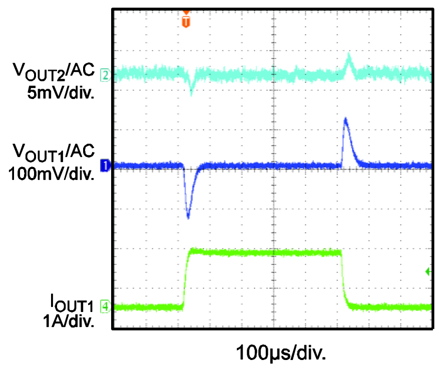
CH1 Steady State, CH2 EN Off
I_{OUT1} = 2A, I_{OUT2} = 0.8A



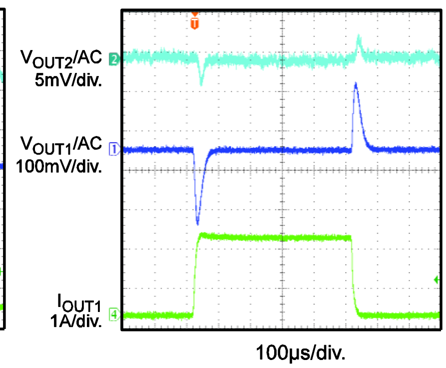
CH1 Load Transient, CH2 Steady State
I_{OUT1} = 0A to 1.4A, 1.6A/μs speed, I_{OUT2} = 0A, FCCM



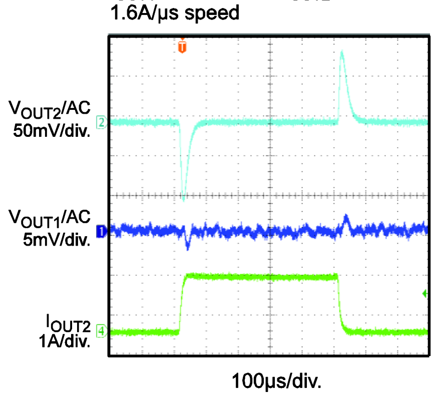
CH1 Load Transient, CH2 Steady State
I_{OUT1} = 0A to 1.4A, 1.6A/μs speed, I_{OUT2} = 1.4A



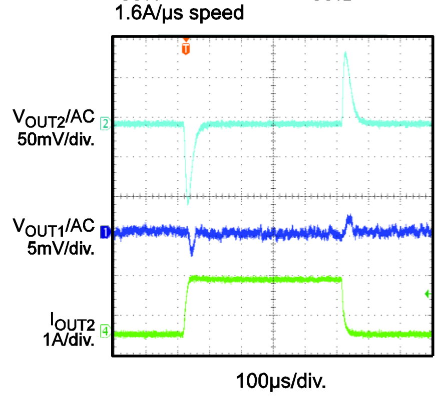
CH1 Load Transient, CH2 Steady State
I_{OUT1} = 0A to 2A, 1.6A/μs speed, I_{OUT2} = 0.8A



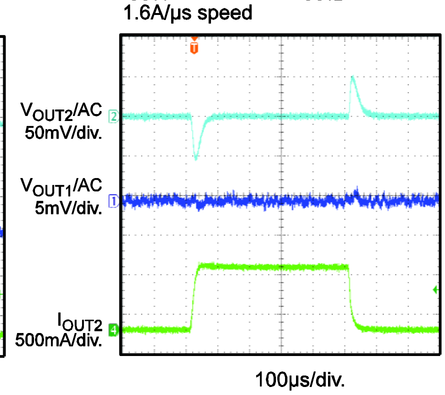
CH1 Steady State, CH2 Load Trasient
I_{OUT1} = 0A, FCCM, I_{OUT2} = 0A to 1.4A, 1.6A/μs speed



CH1 Steady State, CH2 Load Trasient
I_{OUT1} = 1.4A, FCCM, I_{OUT2} = 0A to 1.4A, 1.6A/μs speed



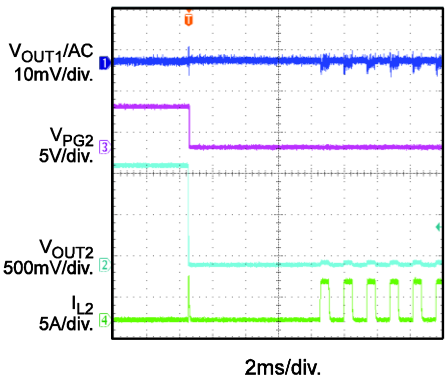
CH1 Steady State, CH2 Load Trasient
I_{OUT1} = 2A, FCCM, I_{OUT2} = 0A to 0.8A, 1.6A/μs speed



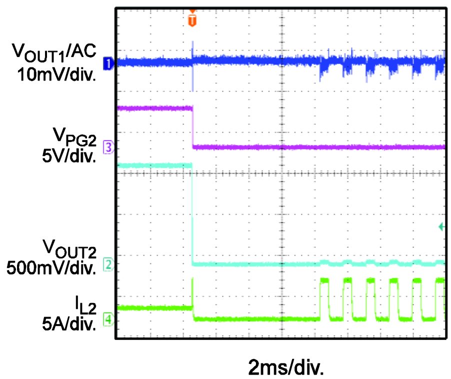
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L1 = L2 = 1.5µH, f_{SW} = 2.25MHz, T_A = 25°C, unless otherwise noted.

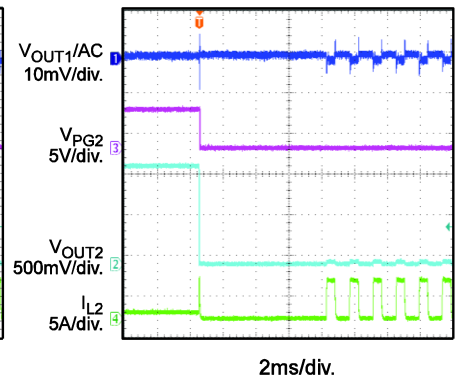
CH1 Steady State, CH2 SCP Entry
I_{OUT1} = I_{OUT2} = 0A, FCCM



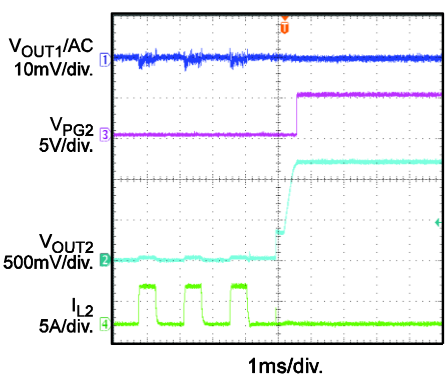
CH1 Steady State, CH2 SCP Entry
I_{OUT1} = I_{OUT2} = 1.4A



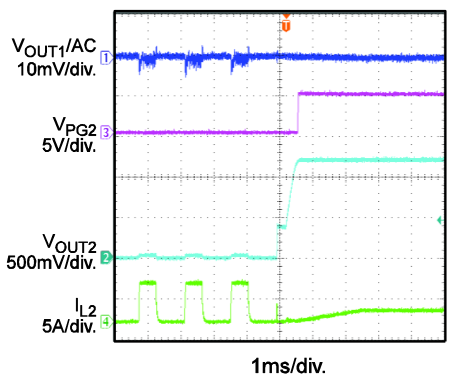
CH1 Steady State, CH2 SCP Entry
I_{OUT1} = 2A, I_{OUT2} = 0.8A



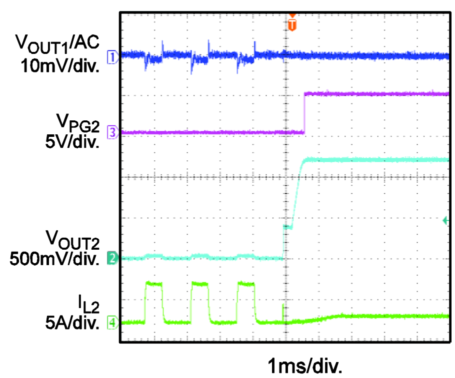
CH1 Steady State, CH2 SCP Recovery
I_{OUT1} = I_{OUT2} = 0A, FCCM



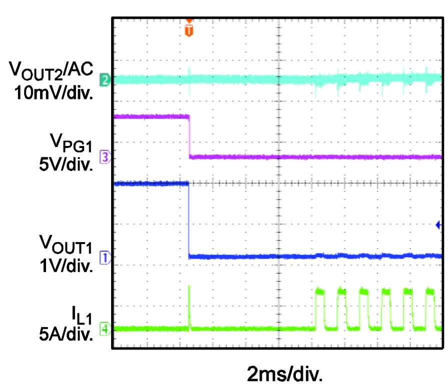
CH1 Steady State, CH2 SCP Recovery
I_{OUT1} = I_{OUT2} = 1.4A



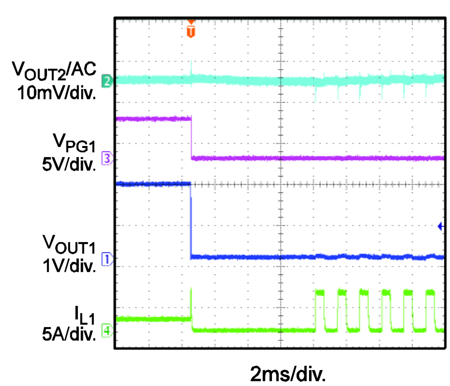
CH1 Steady State, CH2 SCP Recovery
I_{OUT1} = 2A, I_{OUT2} = 0.8A



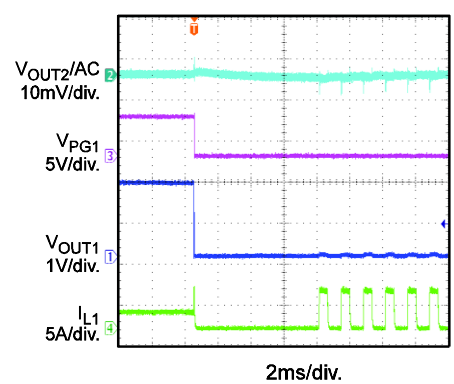
CH1 SCP Entry, CH2 Steady State
I_{OUT1} = I_{OUT2} = 0A, FCCM



CH1 SCP Entry, CH2 Steady State
I_{OUT1} = I_{OUT2} = 1.4A



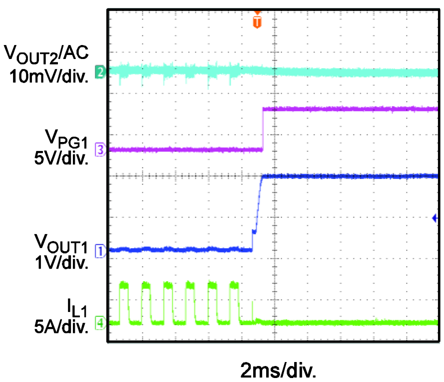
CH1 SCP Entry, CH2 Steady State
I_{OUT1} = 2A, I_{OUT2} = 0.8A



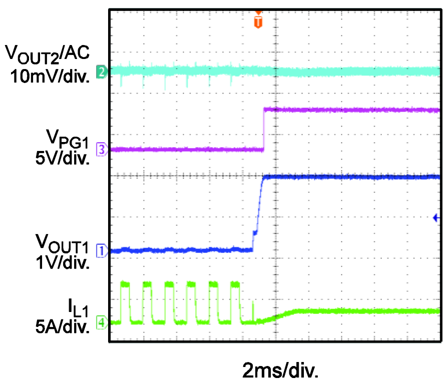
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L1 = L2 = 1.5μH, f_{SW} = 2.25MHz, T_A = 25°C, unless otherwise noted.

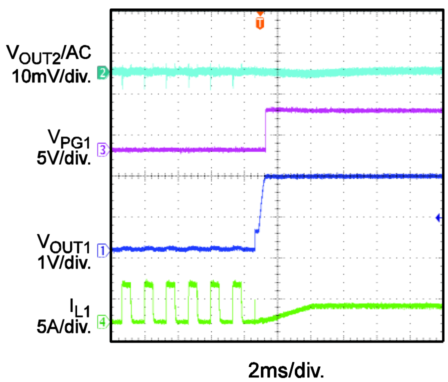
CH1 SCP Recovery, CH2 Steady State
I_{OUT1} = I_{OUT2} = 0A, FCCM



CH1 SCP Recovery, CH2 Steady State
I_{OUT1} = I_{OUT2} = 1.4A



CH1 SCP Recovery, CH2 Steady State
I_{OUT1} = 2A, I_{OUT2} = 0.8A



FUNCTIONAL BLOCK DIAGRAM

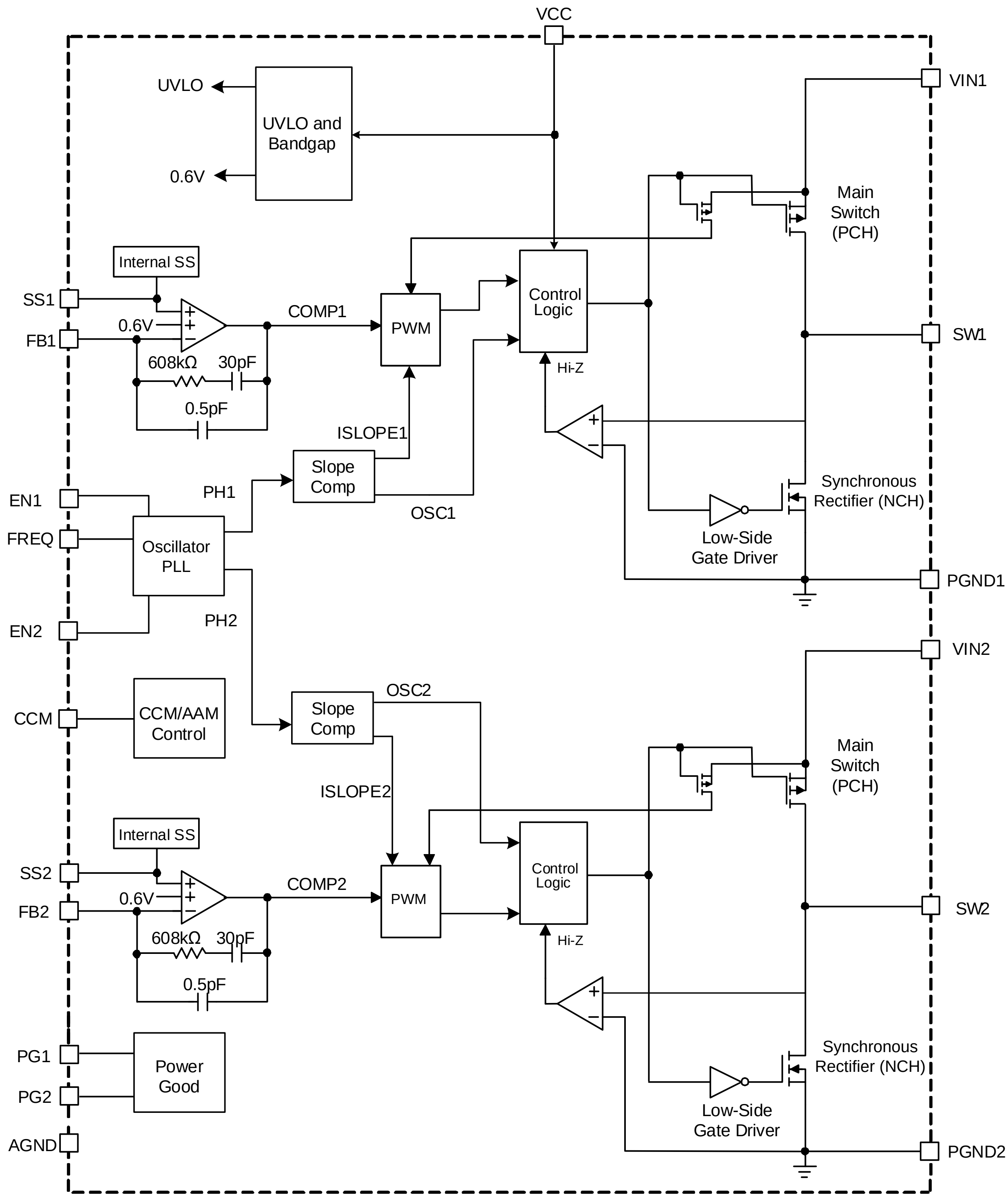


Figure 1: Functional Block Diagram

OPERATION

The MPQ2169A is a fully integrated, dual-channel, synchronous step-down regulator. Both channels use peak current mode control with internal compensation for fast transient response and cycle-by-cycle current limiting.

The MPQ2169A is optimized for low-voltage, portable applications where efficiency and small size are critical.

180° Out-of-Phase Operation

The MPQ2169A operates the two channels in 180° out-of-phase operation to reduce input current ripple. This allows for a smaller input bypass capacitor to be used. If both channels operate in forced continuous conduction mode (FCCM), two internal clocks are used (see Figure 2). The high-side MOSFET (HS-FET) turns on at the clock's rising edge of the corresponding channel.

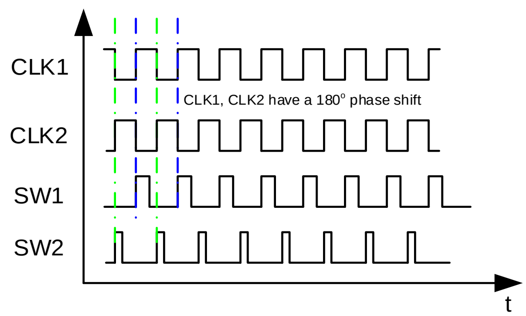


Figure 2: 180° Out-of-Phase Operation

If the switching frequency is stretched out for each channel during low-dropout mode, the MPQ2169A runs with a fixed off time and an independent switching frequency. After the input voltage rises high again, frequency stretch mode ends. Then PWM mode resumes and synchronizes with the master oscillator for out-of-phase operation.

Light-Load Operation

Under light-load conditions, the MPQ2169A can work in two different operating modes by setting the CCM pin to different statuses.

The MPQ2169A works in forced continuous conduction mode (FCCM) when the CCM pin is pulled above 1.6V. In FCCM, the MPQ2169A works with a fixed frequency from no load to full load. The advantages of FCCM are its controllable frequency and lower output ripple under light-load conditions.

The MPQ2169A enters advanced asynchronous mode (AAM) when the CCM pin is pulled below 0.4V. AAM is used to optimize efficiency during light-load and no-load conditions.

When AAM is enabled, the MPQ2169A first enters nonsynchronous operation as the inductor current approaches zero at light-load. If the load decreases further or there is no load, this makes the internal COMP voltage (V_{COMP}) decrease to the set value. Then the MPQ2169A enters AAM. In AAM, the internal clock is reset whenever V_{COMP} crosses over the set threshold, and the crossover time is used as the benchmark of the next clock. When the load increases and V_{COMP} exceeds the set value, the operation mode is in FCCM or discontinuous conduction mode (DCM), which both have a constant switching frequency.

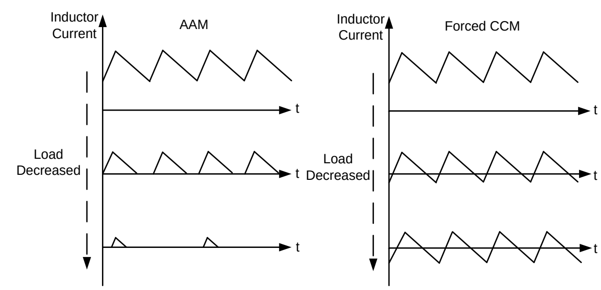


Figure 3: AAM and Forced CCM

Enable (EN)

EN is a digital control pin that turns the regulator on and off.

When EN is pulled below the falling threshold voltage (about 0.4V), the chip shuts down. Forcing EN above the rising threshold voltage (about 1.6V) turns on the part. Do not float the EN pin, since there is no internal resistor from EN to GND. If EN is floated, the part's status is uncertain, which may lead to unexpected behavior.

Soft Start (SS)

The MPQ2169A has a built-in soft start (SS) that ramps up the output voltage at a controlled slew rate, preventing overshoot at start-up. The soft-start time is about 0.5ms.

The SS time (t_{SS}) can also be configured by an external capacitor connected to the SS pin. The default SS time can be calculated with Equation (1):

$$t_{SS}(ms) = \frac{C_{SS}(nF) \times V_{REF}(V)}{I_{SS}(\mu A)} \qquad (1)$$

Where C_{SS} is the external SS capacitor, V_{REF} is the internal reference voltage (0.6V), and I_{SS} is the 3.2μA SS charge current.

Oscillator and SYNC Function

The internal oscillator frequency is set by a single external resistor (R_{FREQ}) connected between FREQ and ground. The frequency-setting resistor should be placed close to the device. Figure 4 shows the relationship between the oscillator frequency (f_{SW}) and R_{FREQ}.

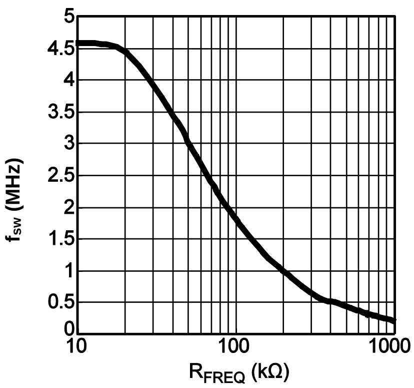


Figure 4: f_{SW} vs. R_{FREQ}

FREQ can also be used to synchronize the internal oscillator to an external clock. The rising edge of the channel 1 clock is synchronized to the external clock's rising edge, while the channel 2 clock remains 180° out-of-phase from channel 1. The recommended external SYNC frequency is in the range of 350kHz to 3MHz. While there is no pulse width requirement, there is always parasitic capacitance on the pad. Therefore, if the pulse width is too short, a clear rising and falling edge may not be seen. It is recommended to make the pulse longer than 100ns.

Add the external SYNC clock (350kHz to 3MHz) before the device starts up, and ensure that the clock stays on until the device is off. Constant high, constant low, and high/low transitions for the SYNC signal are all not allowed during operation.

Power Good (PG)

The MPQ2169A has one power good (PG) output to indicate normal operation after the soft-start time. PG is the open drain of an internal MOSFET. It should be connected to VIN, VCC, or an external voltage source through a resistor (e.g. 100kΩ). After the input voltage is applied, the MOSFET turns on, and PG is pulled to GND before SS is ready. After the FB voltage (V_{FB}) reaches 90% of the reference voltage (V_{REF}), the MOSFET turns off and PG is pulled high by an external voltage source. If V_{FB} drops below 82% of V_{REF}, the PG voltage is pulled to GND to indicate an output failure.

Current Limit and Short Circuit

Each channel of the MPQ2169A has a typical 4A current limit for the HS-FET. Once the inductor current reaches the current limit, the HS-FET turns off immediately. Then the low-side MOSFET (LS-FET) turns on to discharge the energy, and the inductor current decreases. The HS-FET does not turn on again until the inductor current drops below a specified current threshold (called the valley current limit). This protection prevents the inductor current from running away and damaging the components.

If V_{FB} drops below 60% of V_{REF} and soft start has finished, the MPQ2169A treats this as a short fault and attempts to recover with hiccup mode.

In hiccup mode, the MPQ2169A disables the output power stage, slowly discharges the soft-start capacitor, and soft starts automatically. If the short-circuit condition still remains, the MPQ2169A repeats this operation cycle until the short circuit is removed and the output rises back to regulation levels.

LS Current Limit Protection

The MPQ2169A has a -1A low-side (negative) current limit. Once the inductor current reaches the current limit, the LS-FET immediately turns off, and the HS-FET turns on. The current limit prevents the negative current from dropping too low and possibly damaging the components.

Low-Dropout Mode

The MPQ2169A allows the HS-FET to remain on for more than one switching cycle, and increases the duty cycle while the input voltage drops down to the output voltage. When the duty cycle reaches 100%, the HS-FET turns on to deliver current to the output up to its current limit. The output voltage is then the difference between the input voltage, the voltage drop across the main switch, and the inductor.

Thermal Shutdown

The MPQ2169A employs thermal protection by internally monitoring the IC temperature. This function prevents the chip from operating at exceedingly high temperatures. If the junction temperature exceeds the threshold value (typically 175°C), the whole chip shuts down. There is a 40°C hysteresis. Once the junction temperature drops to about 135°C, the device resumes normal operation by initiating a soft start. This is a non-latch protection.

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets the output voltage. The feedback resistor (R1) also sets the feedback loop bandwidth with the internal compensation. The T-type network is recommended (see Figure 5).

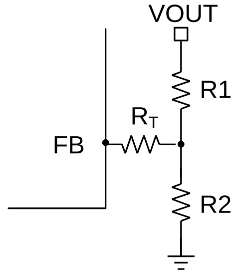


Figure 5: T-Type Feedback Network

R_T and R1 are used to set the loop bandwidth. A lower R_T + R1 value means a higher bandwidth. However, a high bandwidth may cause an insufficient phase margin, resulting in loop instability. Therefore, a proper R_T value is required to make a tradeoff between the bandwidth and phase margin. Table 1 lists the recommended feedback resistor and R_T values for output voltages.

Table 1: Resistor Selection vs. Output Voltage Setting

V_{OUT} (V)	R_T (kΩ)	R1 (kΩ)	R2 (kΩ)
1.2V	100	100	100
1.5V	100	100	66.5
1.8V	100	100	49.9
2.5V	100	100	31.6
3.3V	100	100	22.1

If R1 is estimated to be 100kΩ, R2 can then be calculated with Equation (2):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.6V} - 1} \quad (2)$$

If ceramic capacitors are used as output capacitors (C_O), the feedback loop bandwidth (f_C) should not exceed 1/10 of the switching frequency for optimal transient performance and good phase margin. If an electrolytic capacitor is used, f_C should not exceed 1/4 of the ESR zero frequency (f_{ESR}).

f_{ESR} can be calculated with Equation (3):

$$f_{ESR} = \frac{1}{2\pi \times R_{ESR} \times C_O} \quad (3)$$

For example, choose f_C = 80kHz with a ceramic capacitor when C_O = 22µF.

Selecting the Inductor

An inductor with a DC current rating at least 25% greater than the maximum load current is recommended for most applications. For the best efficiency, the inductor DC resistance should be below 20mΩ. For most designs, the inductance value can be estimated with Equation (4):

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{SW}} \quad (4)$$

Where ΔI_L is inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (5):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (5)$$

Selecting the Input Capacitor

The input capacitor reduces the surge current drawn from the input and the switching noise from the device. The input capacitor impedance at the switching frequency should be less than the input source impedance to prevent high-frequency switching current from passing to the input source. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 22µF capacitor is sufficient.

Selecting the Output Capacitor

The output capacitor (C_O) keeps the output voltage ripple small and ensures a stable regulation loop. The output capacitor impedance should be low at the switching frequency. It is recommended to use ceramic capacitors with X5R or X7R dielectrics. If an electrolytic capacitor is used, pay close attention to the output ripple voltage, extra heating, and the selection of the upper feedback resistor because of the large ESR of electrolytic capacitor (see the Setting the Output Voltage section on page 24). The output voltage ripple (ΔV_{OUT}) can be calculated with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times L \times f_{SW}} \times (ESR + \frac{1}{8 \times f_{SW} \times Co}) \quad (6)$$

Power Dissipation

IC power dissipation is important in circuit design, not only because of efficiency concerns, but also because of the chip's thermal requirements. Several parameters influence power dissipation, such as conduction loss (P_{COND}), dead time (P_{DT}), switching loss (P_{SW}), MOSFET driver current (P_{DR}), and supply current (P_S).

Based on these parameters, the total power loss can be estimated with Equation (7):

$$P_{LOSS} = P_{COND} + P_{DT} + P_{SW} + P_{DR} + P_S \quad (7)$$

Thermal Regulation

Changes in IC temperature can change the electrical characteristics, especially when the temperature exceeds the IC's recommended operating range. Managing the IC's temperature requires additional considerations to ensure that the IC runs within the maximum allowable junction temperature.

Specific layout designs can improve the thermal profile while limiting losses to both efficiency and the device's operating range.

For the MPQ2169A, connect the ground pin on the package to a ground plane on top of the PCB, and use this plane as a heatsink. Connect this ground plane to the ground planes beneath the IC using vias to improve heat dissipation. However, given that these ground planes can introduce unwanted EMI noise and occupy valuable PCB space, design their size and shape to match the thermal resistance requirement.

Connecting the ground pin to a heatsink does not guarantee that the IC will not exceed its recommended temperature limits (e.g. the ambient temperature may exceed the IC's temperature limits). If the ambient air temperature approaches the IC's temperature limit, the IC can be derated to operate using less power, which helps prevent thermal damage and unwanted electrical characteristics.

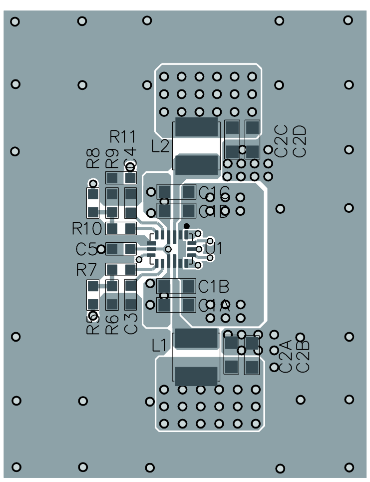
PCB Layout Guidelines [7]

Efficient PCB layout is critical for stable operation. A 4-layer layout is strongly recommended to improve thermal performance. For the best results, refer to Figure 6 and follow the guidelines below:

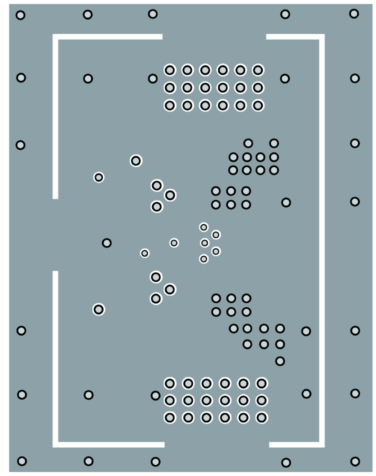
1. Connect PGND1 and PGND2 together at PGND.
2. Place the high-current paths (PGND, VIN, and SW) very close to the device with short, direct, and wide traces.
3. Place input capacitors on both sides of VIN, as close to VIN and PGND as possible.
4. Place the decoupling capacitor as close to VCC and AGND as possible.
5. Keep the switching node (SW) short, and route it away from the feedback network.
6. Place the external feedback resistors next to FB.
7. Do not place vias on the FB trace.
8. Connect PGND to a large copper area to improve thermal performance.
9. Connect PGND1, PGND2, and AGND must be together externally on the board.

Note:

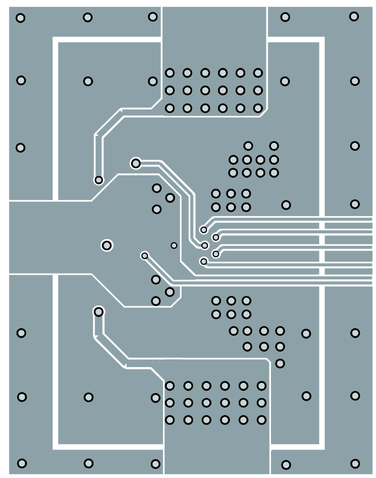
7) The recommended PCB layout is based on Figure 7.



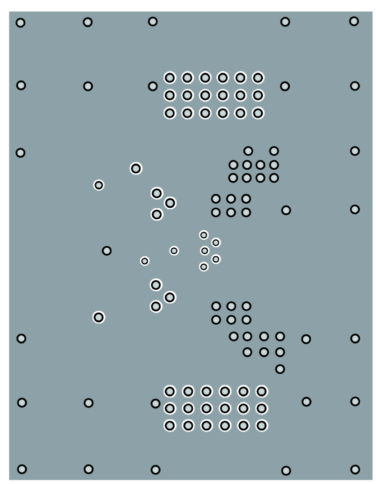
Top Layer



Inner Layer 1



Inner Layer 2



Bottom Layer

Figure 6: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

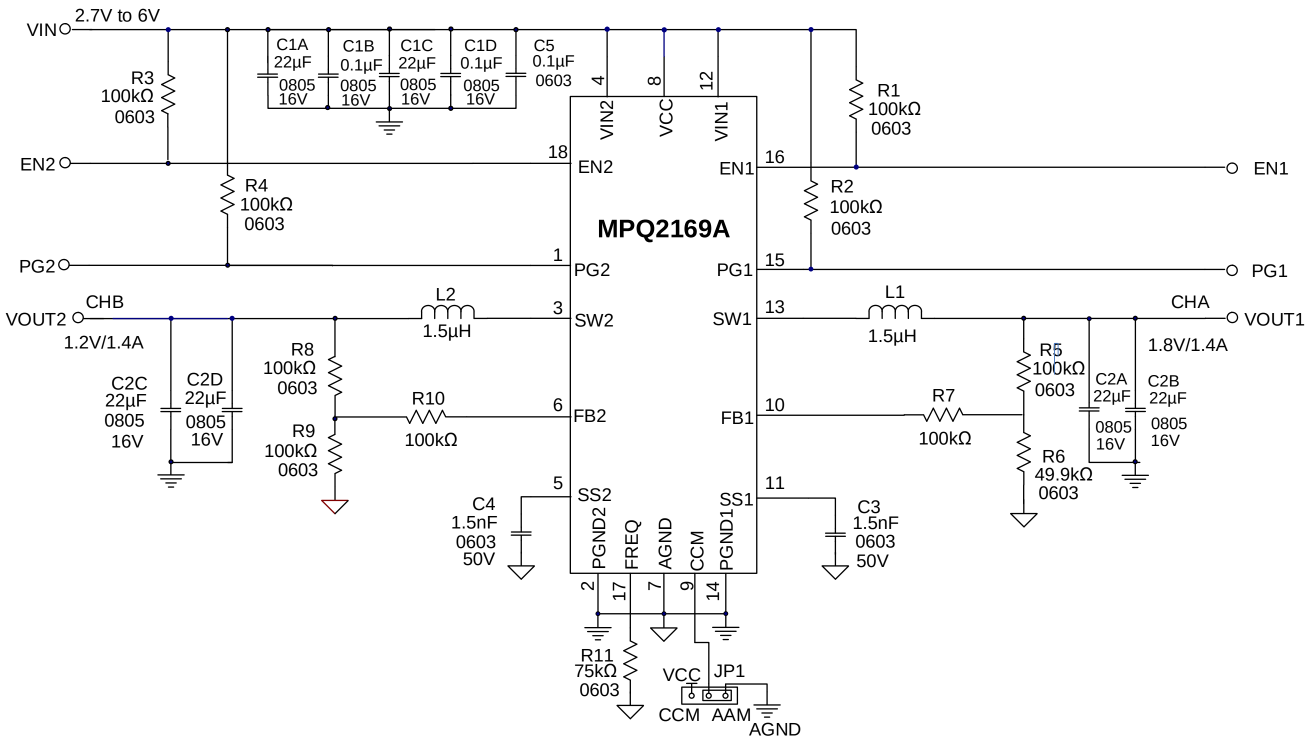


Figure 7: 1.4A/1.4A Application Circuit

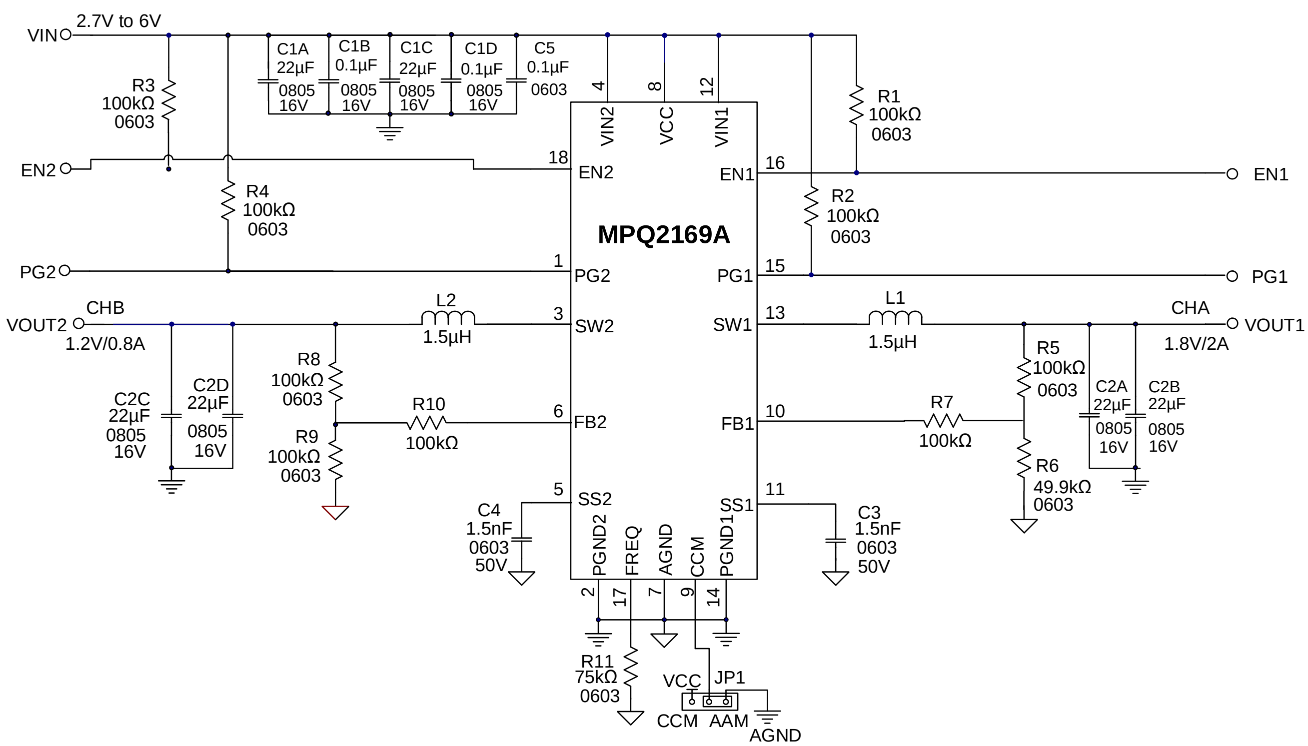
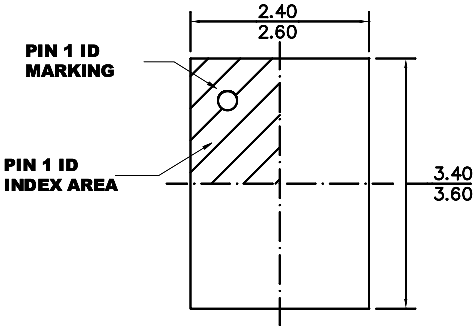


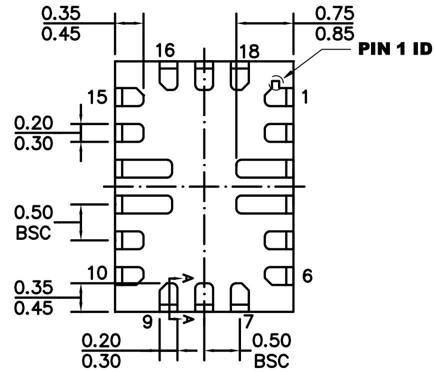
Figure 8: 2A/0.8A Application Circuit

PACKAGE INFORMATION

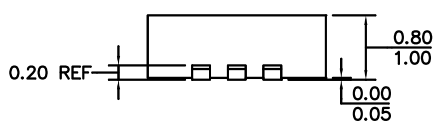
QFN-18 (2.5mmx3.5mm)
Wettable Flank



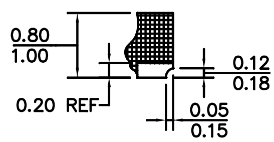
TOP VIEW



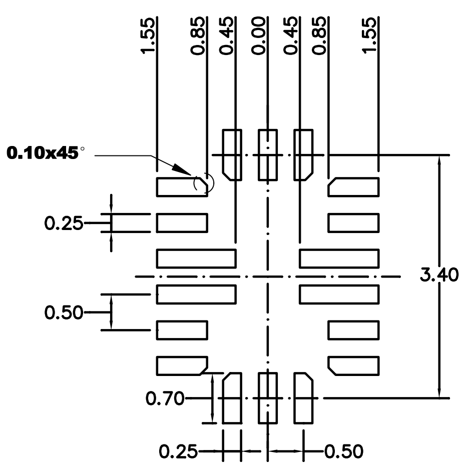
BOTTOM VIEW



SIDE VIEW



SECTION A-A

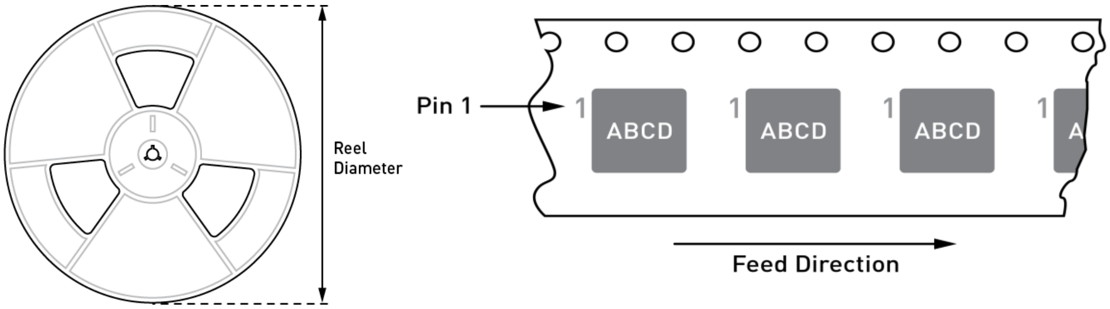


RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) LAND PATTERNS OF PINS 3, 4, 12, AND 13 HAVE THE SAME LENGTH AND WIDTH.
3) ALL DIMENSIONS ARE IN MILLIMETERS.
4) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-220.
6) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube (8)	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ2169AGRHE-AEC1–Z	QFN-18 (2.5mmx3.5mm)	5000	N/A	13in	12mm	8mm

Note:

8) N/A indicates “not available” in tubes. For 500-piece tape and reel prototype quantities, contact MPS. (The order code for a 500-piece partial reel is “–P.” Tape and reel dimensions are the same as the full reel.)

Revision History

Revision #	Revision Date	Description	Pages Updated
1.0	5/14/2020	Initial Release	-