

### DESCRIPTION

The MP4050 is a constant current LED driver integrated with an internal 500V MOSFET. It is specifically designed for energy efficient and low cost LED bulk replacement applications.

MP4050 is designed to drive high-brightness LEDs from an 85V<sub>AC</sub> to 265V<sub>AC</sub> line. It is also useable under DC input voltage. The accurate output LED current is achieved by an averaging internal current feedback loop. Constant LED current is delivered quietly by switching the internal MOSFET at a frequency regulated above 22kHz.

MP4050 can be directly powered by the high input voltage. An internal high voltage current source regulates supply voltage without external circuitry. MP4050 features various protections like Thermal Shutdown (TSD), VCC Under Voltage Lockout (UVLO), Open Lamp Protection and Short Lamp Protection. All of these features make MP4050 an ideal solution for simple, off-line and non-isolated LED applications.

MP4050 is available in the TSOT23-5 and SOIC8 packages.

### FEATURES

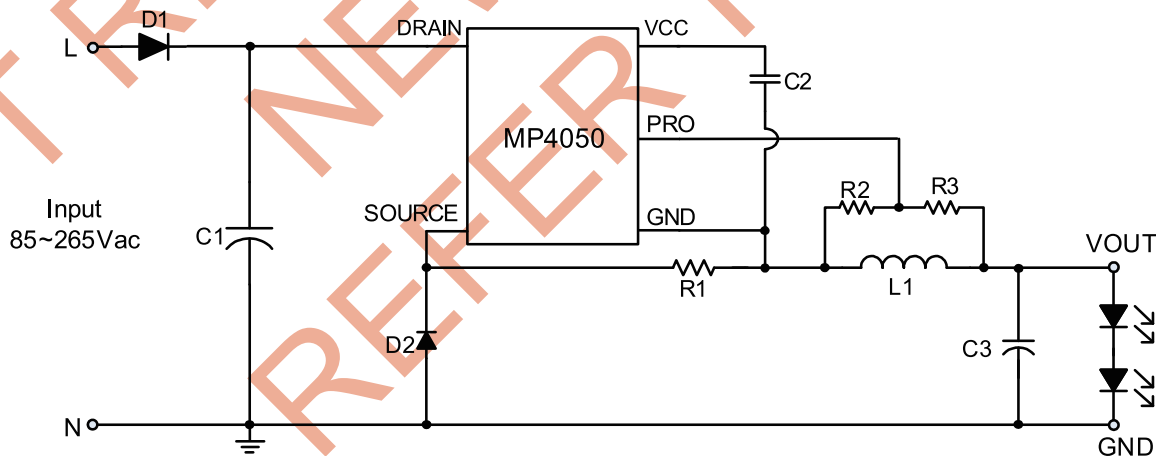
- Constant Current LED Driver
- 500V/7.2Ω MOSFET integrated
- Low Vcc Operating Current
- Maximum frequency limit
- Audible noise restrain
- Internal High Voltage Current Source
- Internal 200ns Leading Edge Blanking
- Thermal Shutdown (auto restart with Hysteresis)
- VCC Under Voltage Lockout with Hysteresis (UVLO)
- Open Lamp Protection
- Short Lamp Protection

### APPLICATIONS

- AC/DC or DC/DC LED driver application
- General Illumination
- Industrial Lighting
- Automotive/Decorative LED Lighting

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### TYPICAL APPLICATION

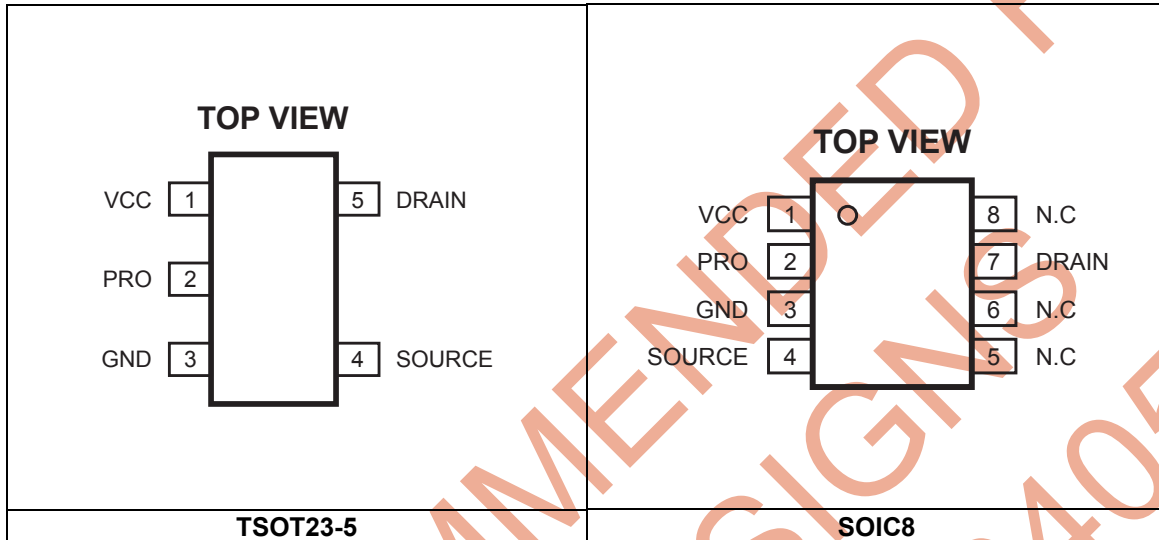


**ORDERING INFORMATION**

Part Number	Package	Top Marking
MP4050GJ*	TSOT23-5	AGN
MP4050GS**	SOIC8	MP4050

\*For Tape & Reel, add suffix -Z (e.g. MP4050GJ-Z);

\*\* For Tape & Reel, add suffix -Z (e.g. MP4050GS-Z);

**PACKAGE REFERENCE**

**ABSOLUTE MAXIMUM RATINGS** <sup>(1)</sup>

Drain to SOURCE .....	-0.3V to 500V
VCC, SOURCE to GND ... ..	-0.3V to 6.5V
PRO to GND .....	-0.7V to 6.5V
Source Current on PRO .....	4mA
Continuous Power Dissipation (T <sub>A</sub> = +25°C) <sup>(2)</sup>	
--TSOT23-5, T <sub>A</sub> =25°C .....	1W
--SOIC8, T <sub>A</sub> =25°C .....	1W
Junction Temperature .....	150°C
Lead Temperature .....	260°C
Storage Temperature .....	-60°C to +150°C
ESD Capability Human Body Mode .....	2.0kV
ESD Capability Machine Mode .....	200V

**Recommended Operating Conditions** <sup>(3)</sup>

Operating Junction Temp. (T <sub>J</sub> )..	-40°C to +125°C
Operating VCC range .....	4.5V to 4.7V

**Thermal Resistance** <sup>(4)</sup>

	$\theta_{JA}$	$\theta_{JC}$
TSOT23-5 .....	100	55 ... °C/W
SOIC8.....	96	45 ... °C/W

**Notes:**

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature T<sub>J</sub> (MAX), the junction-to-ambient thermal resistance  $\theta_{JA}$ , and the ambient temperature T<sub>A</sub>. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P<sub>D</sub> (MAX) = (T<sub>J</sub> (MAX)-T<sub>A</sub>)/ $\theta_{JA}$ . Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- The device is not guaranteed to function outside of its operating conditions.
- Measured on JESD51-7, 4-layer PCB.

**ELECTRICAL CHARACTERISTICS**
**V<sub>CC</sub> = 4.7V, T<sub>A</sub> = 25°C, unless otherwise noted.**

Parameter	Symbol	Condition	Min	Typ	Max	Units
<b>Start-up Current Source (Drain Pin)</b>						
Internal regulator supply current	I <sub>Regulator</sub>	V <sub>CC</sub> =4.5V; V <sub>Drain</sub> =100V	4.5	5	6	mA
Leakage Current from Pin Drain	I <sub>Leak</sub>	V <sub>CC</sub> =6V; V <sub>drain</sub> =400V		14	20	μA
<b>Supply Voltage Management (VCC Pin)</b>						
VCC Increasing Level at which the internal regulator stops	V <sub>CCOFF</sub>		4.45	4.65	4.85	V
VCC Decreasing Level at which the internal regulator Turns-On	V <sub>CCON</sub>		4.2	4.4	4.6	V
VCC Hysteresis between regulator ON/OFF	V <sub>CCOFF-ON</sub>		0.18	0.24	0.3	V
VCC Decreasing level at which the IC stops working	V <sub>CCSTOP</sub>		3.17	3.27	3.37	V
VCC Hysteresis between regulator OFF to VCC stop	V <sub>CCOFF-STOP</sub>		1.23	1.38	1.52	V
VCC Decreasing Level at which the protection Phase Ends	V <sub>CCPRO</sub>		2.10	2.35	2.60	V
Internal IC Consumption	I <sub>CC</sub>	V <sub>CC</sub> =4.3V, F <sub>s</sub> =33kHz, D=84%		350	400	μA
Internal IC Consumption, Latch off Phase	I <sub>CCLATCH</sub>	V <sub>CC</sub> =5V		18	21	μA
<b>Internal MOSFET (Drain Pin)</b>						
Break Down Voltage	V <sub>BRDSS</sub>		500			V
On-State resistance	R <sub>ON</sub>	I <sub>D</sub> =10mA, T <sub>j</sub> =25°C		7.2	10	Ω
<b>Current Sampling Management (Source Pin)</b>						
Peak Current Limit	V <sub>Limit</sub>		0.42	0.45	0.49	V
Leading edge blanking	T <sub>LEB</sub>			200		ns
Feedback Threshold to turn on the primary MOSFET	V <sub>FB</sub>		0.188	0.194	0.200	V
Minimum OFF time limitation	T <sub>OFF_MIN</sub>		3.5	4.7	5.9	μs
Maximum ON time limitation	T <sub>ON_MAX</sub>		18	25	33	μs

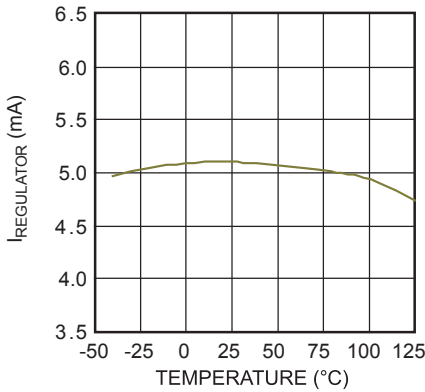
**ELECTRICAL CHARACTERISTICS (continued)**
**V<sub>CC</sub> = 4.7V, T<sub>A</sub> = 25°C, unless otherwise noted.**

Parameter	Symbol	Condition	Min	Typ	Max	Units
<b>Protection input (PRO Pin)</b>						
Threshold to trigger the OVP	V <sub>OVP</sub>		1.9	2.0	2.1	V
Time Constraint on the OVP Comparator	T <sub>OVP</sub>			21	28	μs
Threshold to trigger the UVP	V <sub>UVP</sub>		0.35	0.39	0.43	V
<b>Thermal Shutdown</b>						
Thermal shutdown threshold				150		°C
Thermal shutdown recovery hysteresis				60		°C

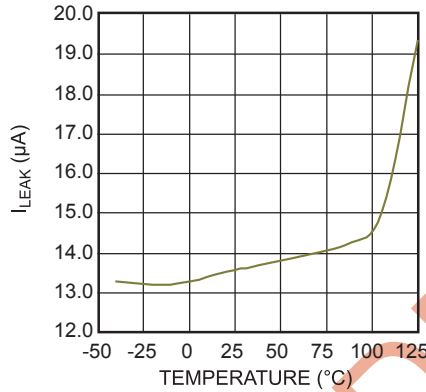
NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP4050A

TYPICAL CHARACTERISTICS

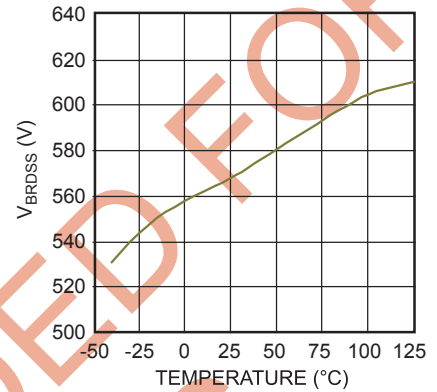
Internal Regulation Current vs. Junction Temperature



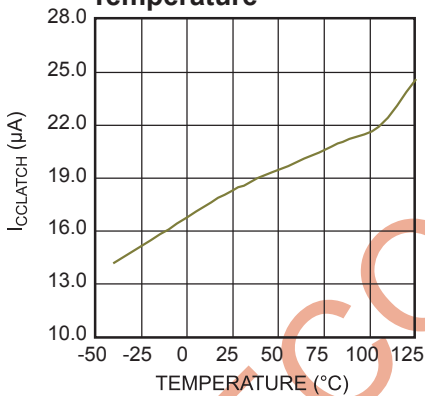
Leakage Current vs. Junction Temperature



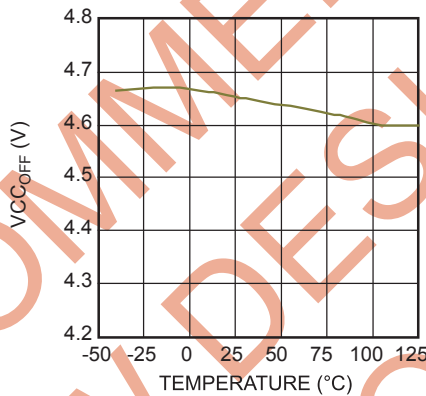
Break Down Voltage vs. Junction Temperature



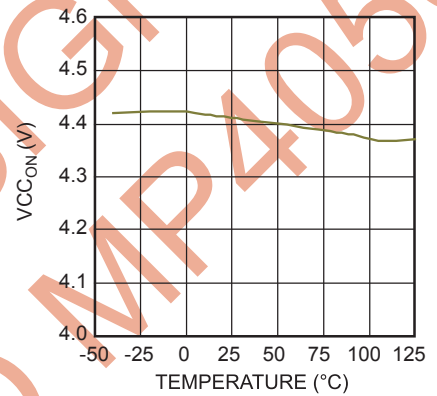
VCC Current In Latch Phase vs. Junction Temperature



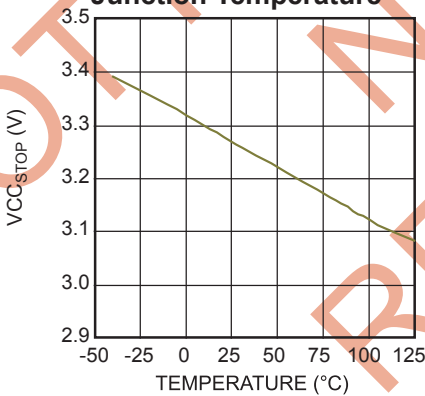
VCC OFF Threshold vs. Junction Temperature



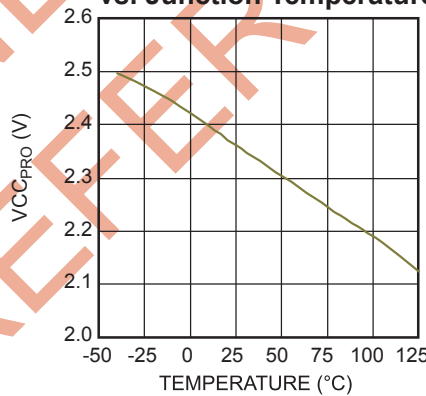
VCC ON Threshold vs. Junction Temperature



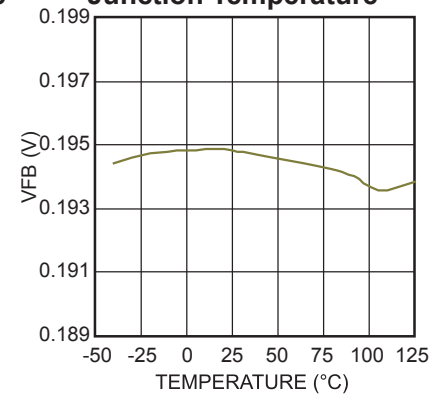
VCC Stop Threshold vs. Junction Temperature



VCC Protection Threshold vs. Junction Temperature

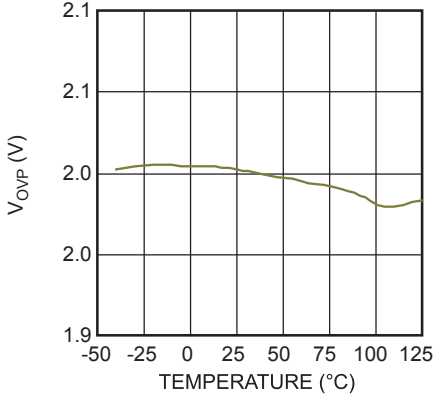


Feedback Reference vs. Junction Temperature

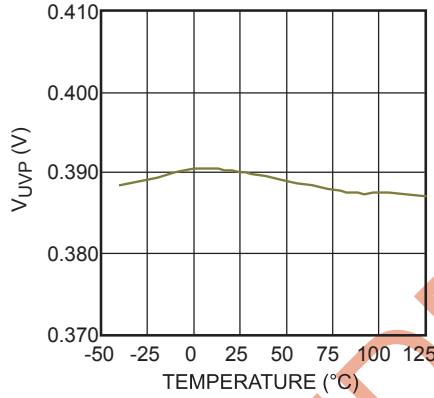


**TYPICAL CHARACTERISTICS** *(continued)*

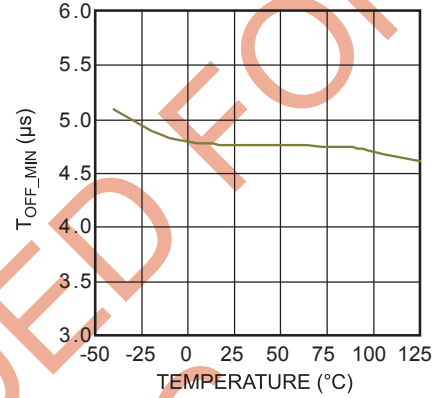
**Over Voltage Protection Reference vs. Junction Temperature**



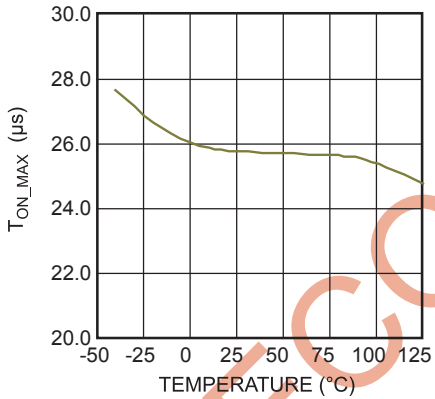
**Under Voltage Protection Reference vs. Junction Temperature**



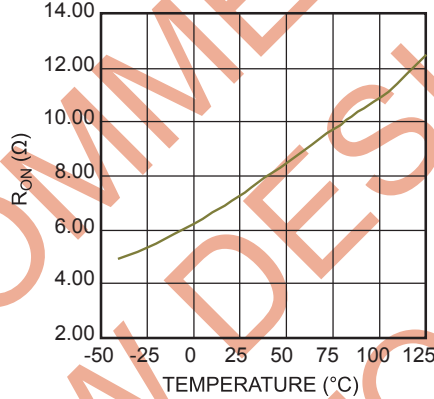
**Minimum OFF Time vs. Junction Temperature**



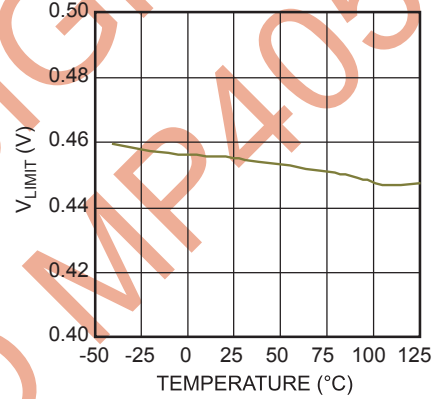
**Minimum ON Time vs. Junction Temperature**



**On-State Resistance vs. Junction Temperature**

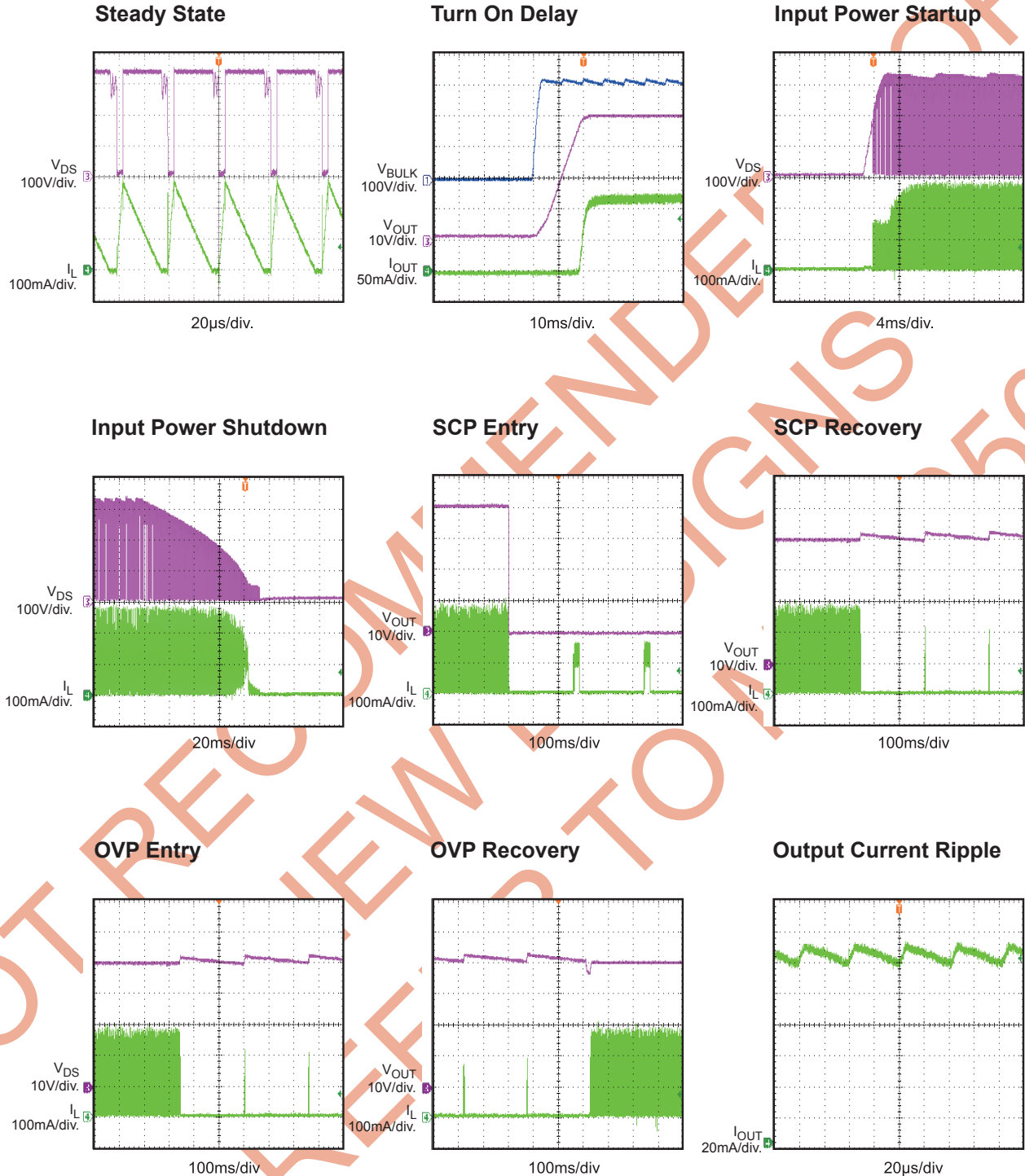


**Peak Current Limit vs. Junction Temperature**



## TYPICAL PERFORMANCE CHARACTERISTICS

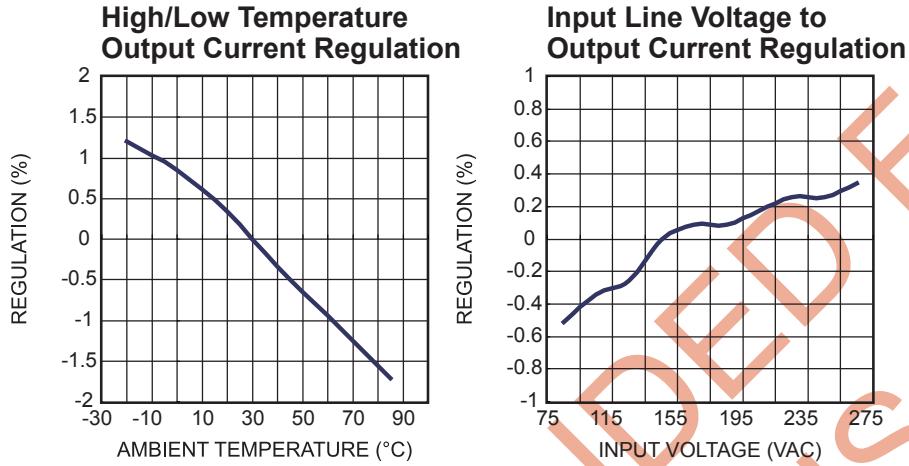
Performance waveforms are tested on the evaluation board of the Design Example section.  
 $V_{IN} = 230V_{ac}$ ,  $V_{OUT} = 40V$ ,  $I_{OUT} = 115mA$ ,  $L = 4.7mH$ ,  $C_{OUT} = 47\mu F$ ,  $T_A = 25^\circ C$ , unless otherwise noted.



**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

Performance waveforms are tested on the evaluation board of the Design Example section.

$V_{IN} = 230V_{ac}$ ,  $V_{OUT} = 40V$ ,  $I_{OUT} = 115mA$ ,  $L = 4.7mH$ ,  $C_{OUT} = 47\mu F$ ,  $T_A = 25^\circ C$ , unless otherwise noted.



NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP4050A

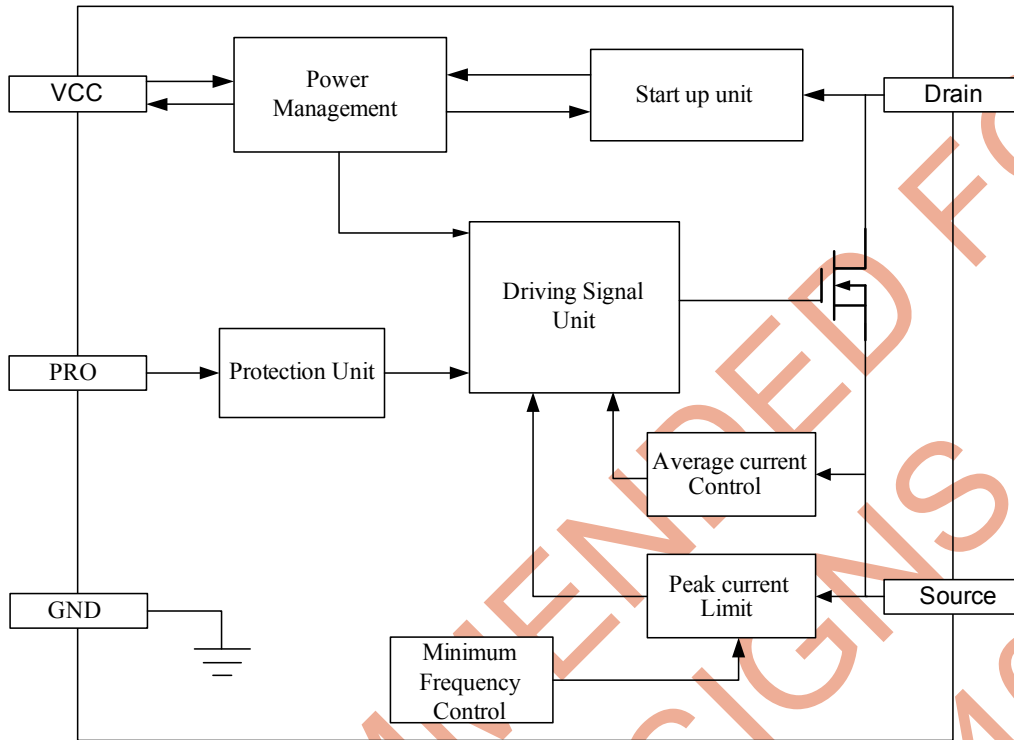


**PIN FUNCTIONS**

Pin # TSOT23-5	Pin # SOIC8	Name	Description
1	1	VCC	Power supply for all the control circuits.
2	2	PRO	Open lamp protection if the voltage is higher than $V_{OVP}$ , Short Lamp protection if the voltage is lower than $V_{UVP}$ .
3	3	GND	Ground of the IC
4	4	SOURCE	Source of internal power MOSFET. Internal peak current limit is 0.45V (typical value). Output current sample.
5	7	DRAIN	Drain of internal power MOSFET. Input of high voltage current source.
	5,6,8	N.C	Not Connected.

NOT RECOMMENDED FOR  
 NEW DESIGNS  
 REFER TO MP4050A

**FUNCTION BLOCK DIAGRAM**



**Figure 1: Functional Block Diagram**

## OPERATION

MP4050 is a non-isolated, cost-effective, high efficiency converter designed to drive high-brightness light emitting diodes (LEDs) from an 85Vac to 265 Vac line, or a DC input. As shown in the typical application diagram, the regulator is designed to operate with a minimum number of external components. It incorporates the following features:

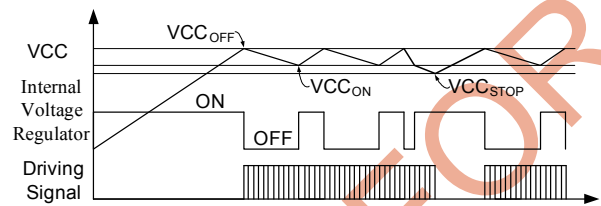
### Start-up and Under Voltage Lock-out (UVLO)

The IC is self supplied by the internal high voltage regulator which is drawn from the Drain pin. The IC starts switching and the internal high voltage regulator turns off as soon as the voltage on pin  $V_{CC}$  reaches  $V_{CCOFF}$ . When the voltage on Pin  $V_{CC}$  decreases below  $V_{CCON}$ , the internal high voltage regulator turns on again to charge the external  $V_{CC}$  capacitor. A small capacitor such as several  $\mu F$  capacitor is enough to hold on the voltage of  $V_{CC}$  and a smaller capacitor also reduce component cost. When the voltage on Pin  $V_{CC}$  drops below  $V_{CCSTOP}$ , the IC stops working, the internal high voltage regulator recharges the  $V_{CC}$  capacitor.

When fault conditions happen, such as Short Lamp Protection, Open Lamp Protection and Over Temperature Protection (OTP), MP4050 stops working and a 18uA internal current source discharges the  $V_{CC}$  capacitor. After the  $V_{CC}$  drops below  $V_{CCPRO}$ , the internal high voltage regulator recharges the  $V_{CC}$  capacitor again. The restart time can be calculated by the following equation,

$$t_{\text{restart}} = C_{V_{CC}} \times \frac{V_{CC} - 2.37V}{18\mu A} + C_{V_{CC}} \times \frac{4.65V - 2.37V}{5mA}$$

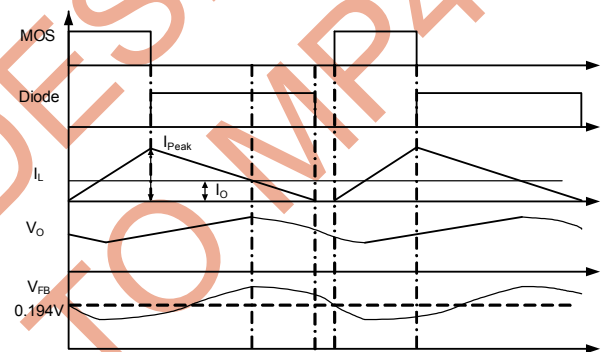
Figure 2 shows the typical waveform with  $V_{CC}$  under voltage lock out.



**Figure 2:  $V_{CC}$  Under-Voltage Lock Out (UVLO)**

### Constant Current Operation

MP4050 is a fully integrated regulator, the internal feedback logic responds to the internal sample and hold circuit to achieve constant output current regulation. The voltage of the internal sampling capacitor ( $V_{FB}$ ) is compared to the internal reference 0.194V, when the sampling capacitor voltage ( $V_{FB}$ ) falls below the reference voltage, which indicates insufficient output current, the integrated MOSFET is turned ON. The ON period is determined by the peak current limit. After the ON period elapses, the integrated MOSFET is turned OFF. The detail operation is shown as Figure 3.



**Figure 3:  $V_{FB}$  vs  $I_{out}$**

Thus by monitoring the internal sampling capacitor voltage, the output current can be regulated and the output current is determined by the following equation:

$$I_o = \frac{0.194V}{R1}$$

The peak current can be obtained as follow:

$$I_{Peak} = \frac{0.45V}{R1}$$

R1 is the sense resistor.

### Minimum Operating Frequency Limit

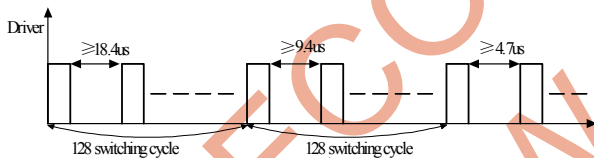
MP4050 incorporates minimum operating frequency (22kHz) to eliminate the audible noise when frequency is less than 20kHz.

When operating frequency is less than 22kHz, the internal peak current regulator will decrease the peak current value to keep the operating frequency constant about 22kHz.

If the inductance value is too large to make the operating frequency reach the minimum operating frequency, the converter will enter the CCM. And the converter works in DCM when operating frequency is larger than 22kHz.

### Minimum Off Time Limit

A minimum off time limit is implemented. During the normal operation, the minimum off time limit is 4.7us, and during the start up period, the minimum off time limit is shortened gradually from 18.8us, 9.4us to 4.7us (Shown as Figure 4). Each minimum off time keeps 128 switching cycle. This soft start function enables safe start-up.



**Figure 4:  $t_{minoff}$  at start-up**

### Thermal Shutdown (TSD)

To prevent MP4050 from any thermal damage, MP4050 shuts down switching cycle when the junction temperature exceeds 150°C. As soon as the junction temperature drops below 90°C, the power supply resumes operation. During the thermal shutdown (TSD), the  $V_{CC}$  is discharged to  $V_{CCPRO}$ , and then is re-charged by the internal high voltage regulator.

### Open Lamp Protection

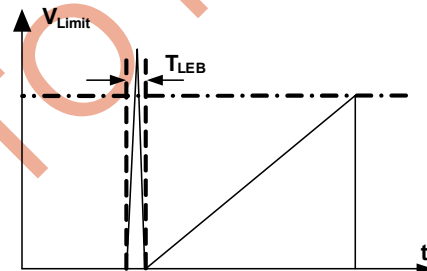
If the PRO pin voltage ( $V_{PRO}$ ) is higher than  $V_{OVP}$  when MOSFET turns off, MP4050 stops working and a re-start cycle begins. Open lamp protection is hiccup mode. MP4050 monitors the PRO pin voltage continuously and the VCC voltage discharges and charges repeatedly. MP4050 resumes work until the fault disappears.

### Short Lamp Protection

If the PRO pin voltage ( $V_{PRO}$ ) is lower than  $V_{UVP}$  when MOSFET turns off, MP4050 stops working and a re-start cycle begins. Short lamp protection is hiccup mode. MP4050 monitors the PRO pin voltage continuously and the VCC voltage discharges and charges repeatedly. MP4050 resumes work until the fault disappears.

### Leading Edge Blanking

There are parasitic capacitances in the circuit which can cause high current spike during the turn-on of the internal MOSFET. In order to avoid the premature termination of the switching pulse, an internal Leading Edge Blanking (LEB) unit is employed. During the blanking time, the current comparator is disabled and blocked from turning off the internal MOSFET. Figure 5 shows the leading edge blanking.



**Figure 5: Leading Edge Blanking (LED)**

## APPLICATION INFORMATION

### Component Selection

#### Input Capacitor

The input capacitor is used to supply the DC input voltage for the converter. Figure 6 shows the typical DC bus voltage waveform of full bridge rectifier.

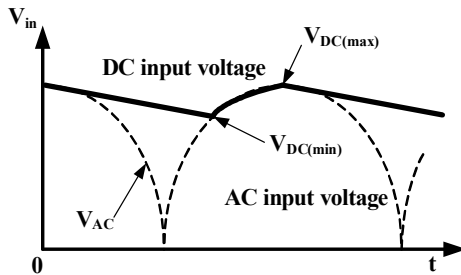


Figure 6: Input voltage waveform

When the full-bridge rectifier is used, the input capacitor is usually set as  $2\mu\text{F}/\text{W}$  for the universal input condition. And when small power output, the half-bridge rectifier could also be used with a bigger capacitor.

Very low DC input voltage could cause thermal problem in LED application in Buck topology application. The minimum DC voltage is limited by the maximum duty cycle of MP4050 as following expression:

$$V_{\text{DC}(\text{min})} > \frac{V_{\text{O}} \cdot (t_{\text{ON\_MAX}} + t_{\text{OFF\_MIN}})}{t_{\text{ON\_MAX}}}$$

#### Inductor

MP4050 has a minimum off time limit and maximum on time limit. Both time limits affect the inductance value. The maximum inductance value and minimum inductance value can be obtained as follows:

$$L_{\text{m}} < L_{\text{MAX}} = \frac{(V_{\text{DC}(\text{min})} - V_{\text{O}}) \cdot t_{\text{ON\_MAX}}}{I_{\text{Peak}}}$$

$$L_{\text{m}} > L_{\text{MIN}} = \frac{V_{\text{O}} \cdot t_{\text{OFF\_MIN}}}{I_{\text{Peak}}}$$

If the inductance value is too large, the converter enters CCM when the frequency reaches the minimum operating frequency. In such case, the reverse recovery of freewheeling diode results more power loss. Normally, it's

better to make the converter operate in DCM. The following expression shows the limit of the minimum operating frequency.

$$L_{\text{m}} < \frac{2 \cdot I_{\text{O}}}{f_{\text{SMIN}} \cdot \left( \frac{1}{V_{\text{DC}(\text{min})} - V_{\text{O}}} + \frac{1}{V_{\text{O}}} \right) \cdot I_{\text{Peak}}^2}$$

#### Freewheeling Diode

The diode should have a maximum reverse voltage rating which is greater than the maximum input voltage. The current rating of diode is determined by the output current which should be larger than 1.5~2 times output current.

Slow diodes cause excessive leading edge current spikes during start-up which is not acceptable. Long reverse recovery time of freewheeling diode can also affect the efficiency and the circuit operation. So ultrafast diode ( $T_{\text{rr}} < 75\text{ns}$ ) such as WUGC10JH or EGC10GH are recommended.

#### Output Capacitor

The output capacitor is required to filter the inductance current and maintain the DC output voltage.

The output current ripple is reduced by using a bigger output capacitor. A low ESR capacitor is necessary in low temperature application.

If the output voltage ripple is limited, the ceramic, tantalum or low ESR electrolytic capacitors are recommended to use. The output voltage ripple can be estimated by:

$$V_{\text{CCM\_Ripple}} = \frac{\Delta i}{8f_{\text{s}}C_{\text{O}}} + \Delta i \cdot R_{\text{ESR}} \quad \text{CCM}$$

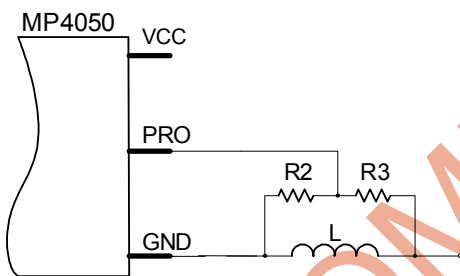
$$V_{\text{DCM\_Ripple}} = \frac{I_{\text{O}}}{f_{\text{s}}C_{\text{O}}} \cdot \left( \frac{I_{\text{Peak}} - I_{\text{O}}}{I_{\text{Peak}}} \right)^2 + I_{\text{Peak}} \cdot R_{\text{ESR}} \quad \text{DCM}$$

### Sense Resistor

The sense resistor needs to choose properly for better output current regulation. The right resistor guarantees stable output current regulation in high temperature and low temperature conditions. The sense resistor should have 1% tolerance. It is even better to parallel two 1% tolerance resistors to decrease the resistance value error further. Sense resistor with  $\pm 400\text{PPM}/^\circ\text{C}$  temperature coefficient can be used for better output current regulation in high temperature and low temperature.

### Feedback Resistor

Feedback resistor is used to detect the fault operation mode such as open lamp or short lamp conditions. Figure 7 shows the feedback resistors connection.



**Figure 7: Feedback resistor connection**

MP4050 is integrated with open lamp protection and the over voltage protection point can be designed as following function.

$$V_{\text{OVP}} = V_{\text{PRO}} \cdot \left(1 + \frac{R2 + R3}{R2}\right) - V_D$$

$V_D$  is the freewheeling diode forward voltage drop.

The upper feedback resistor (R3) is suggested to be larger than  $100\text{k}\Omega$  to avoid the efficiency reduction in application. And the 1% tolerance type is recommended to use as feedback resistor to achieve accurate protection such over voltage protection when open lamp.

The feedback resistor R2 could be sized down to SMD 0603 package. Considering the dielectric withstanding voltage, R3 is recommended to have a minimum size of SMD 1206 package.

### Dummy Load

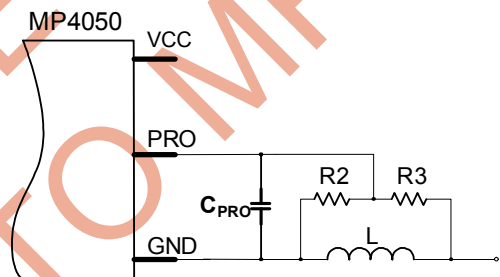
Dummy load is recommended to regulate the output voltage low than over voltage protection point when open lamp condition. The dummy load is used to consume the power transferred to output capacitor when hiccup mode without any power consumption.

Normally less than 1mA dummy load is suggested which not deteriorate the system efficiency and also guarantees the normal open lamp protection.

### PRO Decoupling Capacitor

One decoupling cap is recommended to parallel between the PRO pin and GND pin. The floating GND pin is sensitive to the voltage noise spike in high side Buck solution. One ceramic capacitor is suggested to use as decoupling capacitor to decouple the voltage noise for more stable operation.

Around 30pF PRO decoupling capacitor could be used in SOIC8 package application and as for smaller package TSOT23-5, no less than 100pF decoupling capacitor is recommended. Figure 8 shows the PRO pin decoupling capacitor connection.



**Figure 8: Decoupling capacitor**

### PRO Time Constant

MP4050 detects the PRO pin voltage to judge the fault condition when internal MOSEFET turns off. Long rise time of the PRO pin voltage affects MP4050 normal output voltage sample which can not judge the open lamp immediately. The PRO pin time constant ( $\tau$ ) should satisfy the following expression to guarantee the normal open lamp protection.

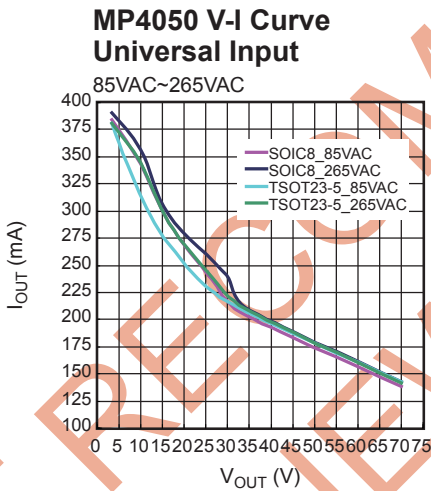
$$\tau = C_{PRO} \cdot \frac{R2 \cdot R3}{R2 + R3} < 1\mu s$$

**Output Power V-I Curve**

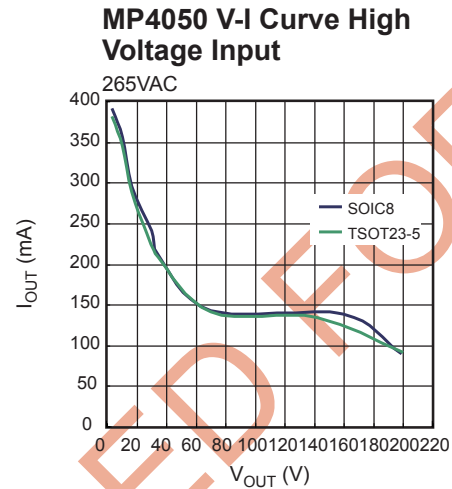
The thermal performance limits the output power of MP4050 in very small size LED application. Different output voltage and output current specification bring about different maximum output power delivered from the MP4050 device.

Figure 9 and Figure 10 separately show the reference V-I curve in universal input voltage and high voltage input under following assumed conditions:

1. Buck topology.
2. Ambient temperature 90°C.
3. Around 30kHz working frequency.
4. No PF required where input capacitor >9uF.
5. Not trigger the thermal shutdown and leave one LED margin.



**Figure 9: Universal input V-I curve (85VAC~265VAC)**



**Figure 10: High voltage input V-I curve (200VAC~265VAC)**

**Power Factor**

MP4050 is mainly used for non-isolated, space constrained and cost sensitive LED driver solution. As for the PF>0.5 when 120VAC input required, MP4050 is also the best choose. The input capacitance is reduced to achieve the highest possible power factor as PF>0.7 when 120VAC and PF>0.5 when 230VAC if the output current regulation is not strict.

**Surge**

Select the appropriate input capacitance to obtain a good surge performance. With the input capacitor C2 (4.7uF) and C3 (4.7uF) as Figure 13, the board can pass 1kV differential input line 1.2/50us surge test (IEC61000-4-5). It is recommended to increase the input capacitor value to suppress above 1kV surge test. As for high PF required application with lower input capacitor value giving a greater voltage rise, a Metal Oxide Varistor (MOV) is typically required to pass the above 1kV or greater surge test.

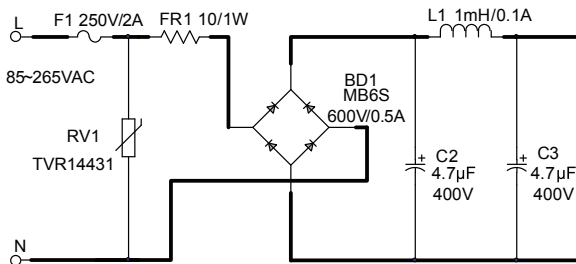
Table 1 shows input capacitor value required for pass the differential surge test.

**Table 1: Recommended input capacitance**

Surge voltage	500V	1000V	1500V	2000V
C2	3.3 $\mu$ F	4.7 $\mu$ F	4.7 $\mu$ F	Show in Figure11
C3	3.3 $\mu$ F	4.7 $\mu$ F	10 $\mu$ F	

The demo board can pass the 2000V differential surge test by adopting below circuit setup.

- (1) Add a MOV RV1(TVR14431)
- (2) Add a fuse F1 (SS-5-2A)


**Figure11: 2kV surge solution**

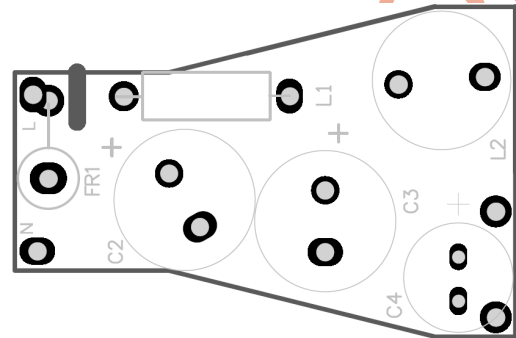
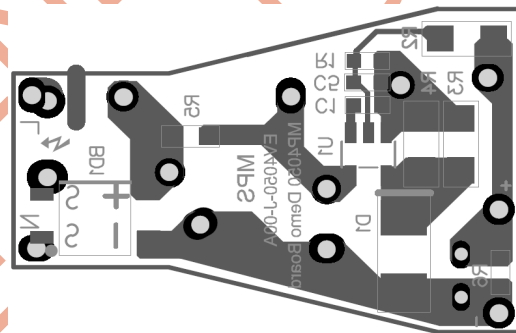
### Layout Guide

PCB layout is very important to achieve reliable operation, good EMI and good thermal performance especially in very small size LED application. The following describe some layout recommendations.

1. The loop formed between the MP4050, inductor, freewheeling diode and output capacitor should be kept as small as possible for better EMI.
2. Put the AC input far away from the switching nodes to minimize the noise coupling that may bypass the input filter.
3. The VCC pin and PRO pin capacitor should be located physically close to the IC and GND.
4. Put the feedback resistor next to the PRO pin as possible and minimize the feedback sampling loop to minimize the noise coupling route.
5. In the buck topology, since the MP4050 SOURCE pin is switching nodes, the copper area connected to SOURCE should be minimize to minimize EMI with the thermal constraints of the design.

6. Since MP4050 DRAIN pin is static node connecting to DC input, the copper area connected to DRAIN could be maximized to improve the heat sinking.

Figure 12 shows a sample layout.


**Top Layer**

**Bottom Layer**
**Figure 12: PCB Layout**

### Design Example

Below is a design example following the application guidelines based on these specifications:

**Table 2: Design Example**

$V_{IN}$	85Vac~265Vac
$V_{OUT}$	40V
$I_{OUT}$	115mA

Figure 13 shows the detailed application schematic. This circuit is used for the typical performance and circuit waveforms. For more device applications, please refer to the related evaluation board datasheets.



TYPICAL APPLICATION CIRCUITS

Figure 13 shows a typical application example of a 40V, 115mA non-isolated buck topology power supply using MP4050.

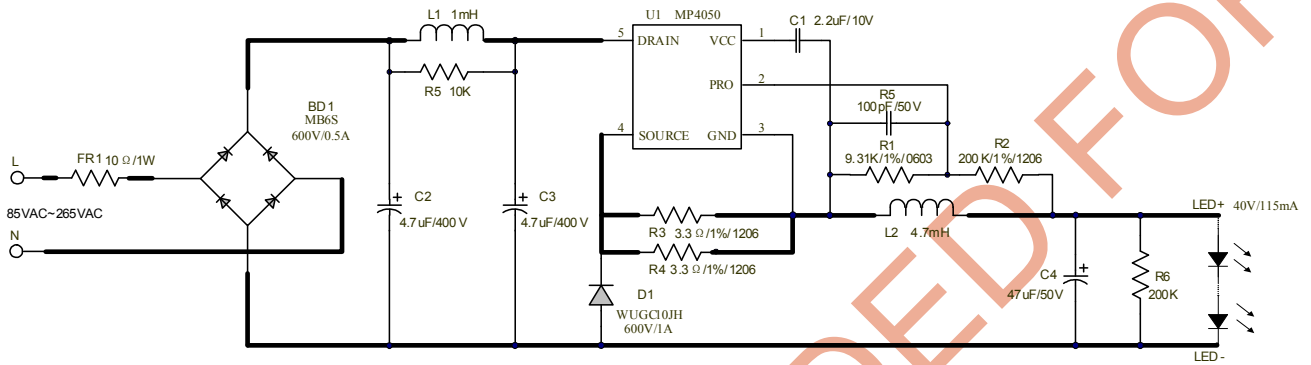
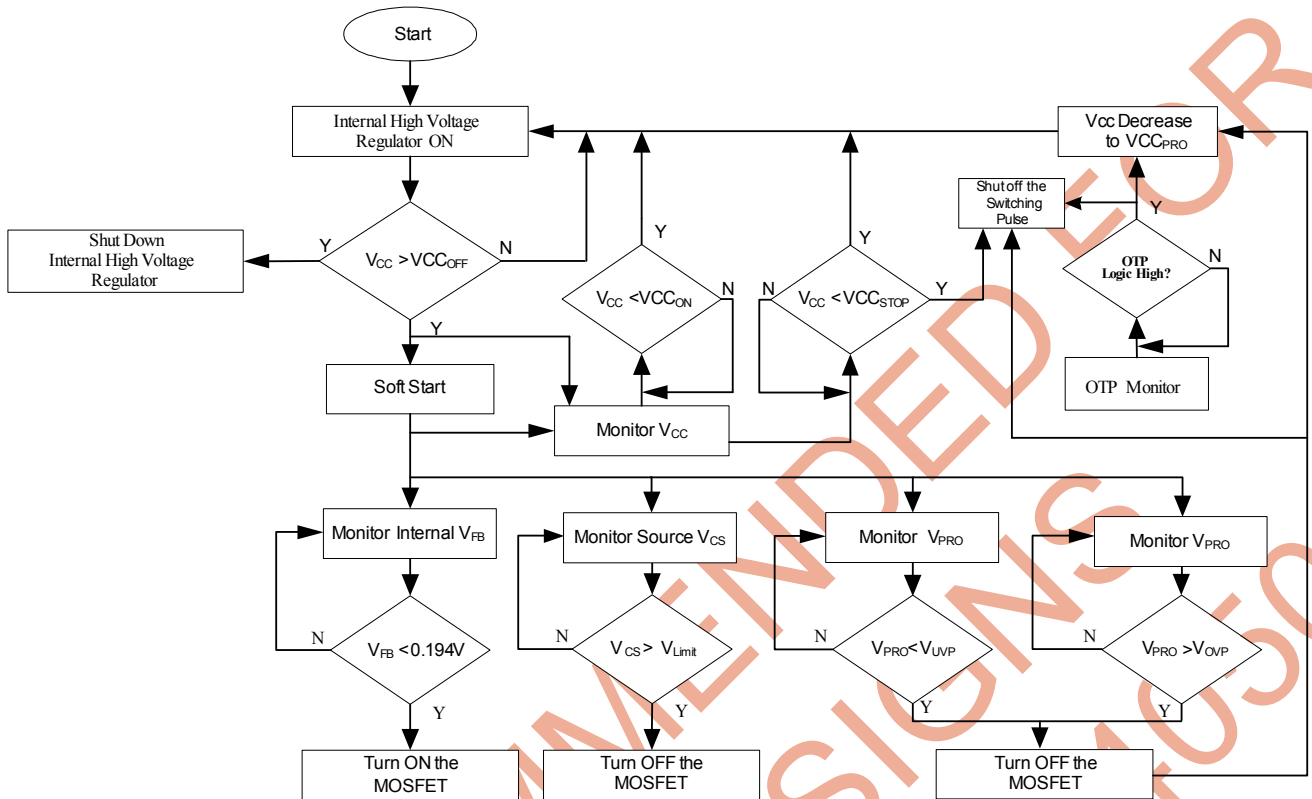


Figure 13: Typical Buck Converter Application

FLOW CHART



UVLO, OTP, Short Lamp Protection, Open Lamp Protection  
All protections are auto restart

Figure 14: Control Flow Chart

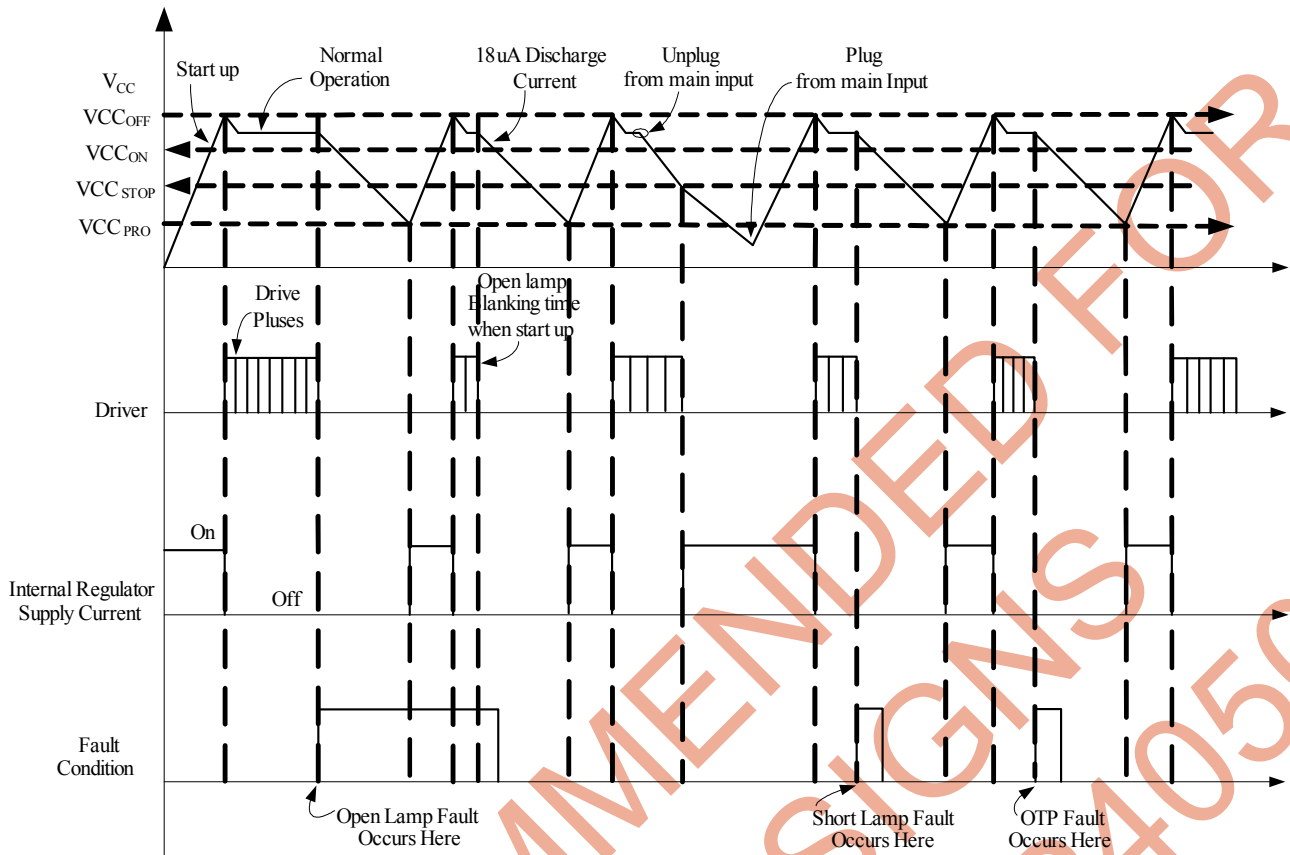
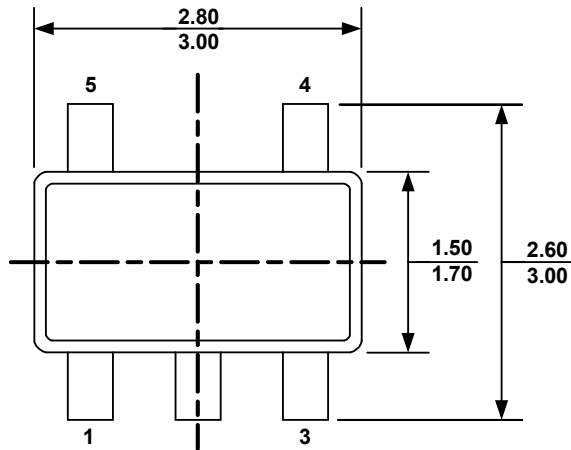


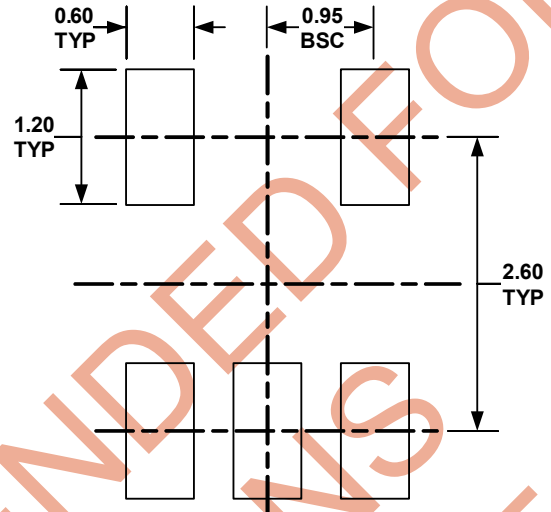
Figure 15: Evolution of the signal in presence of a Fault

## PACKAGE INFORMATION

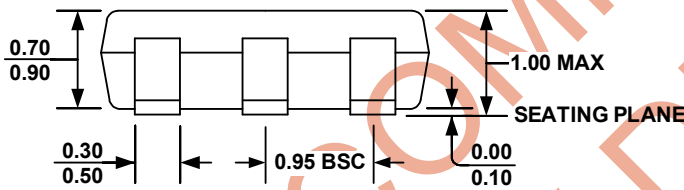
## TSOT23-5



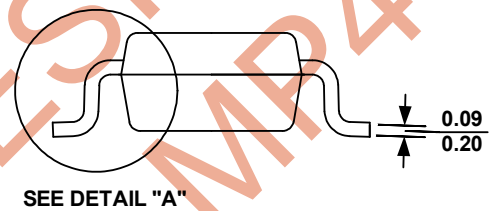
TOP VIEW



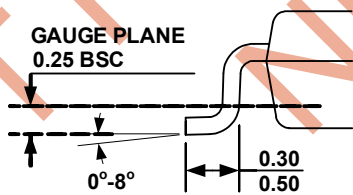
RECOMMENDED LAND PATTERN



FRONT VIEW



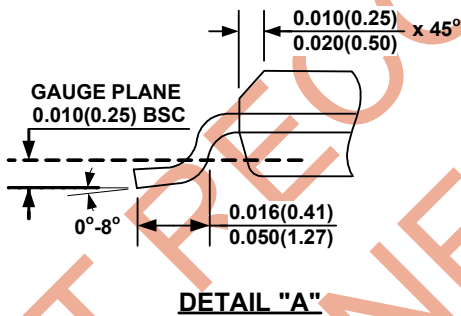
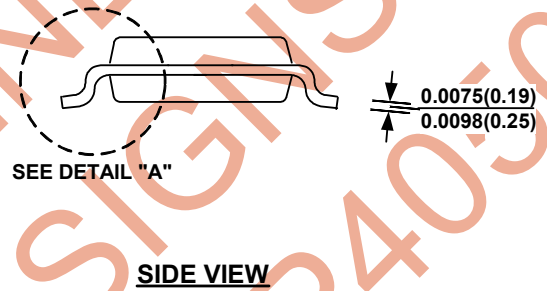
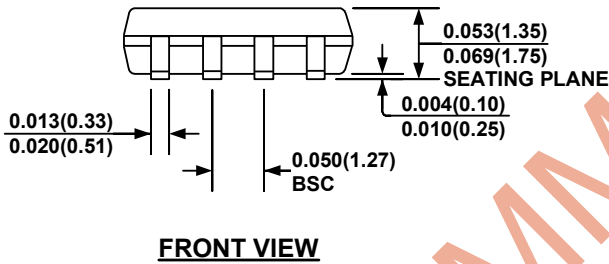
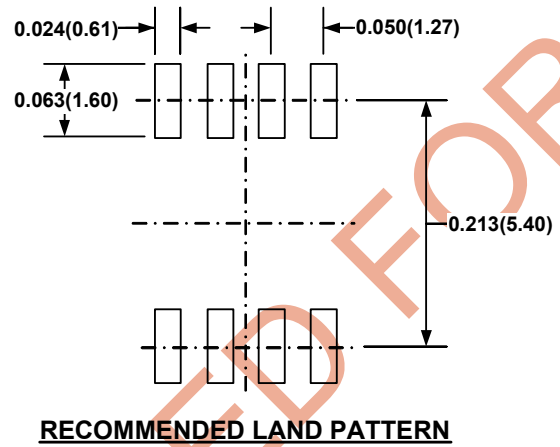
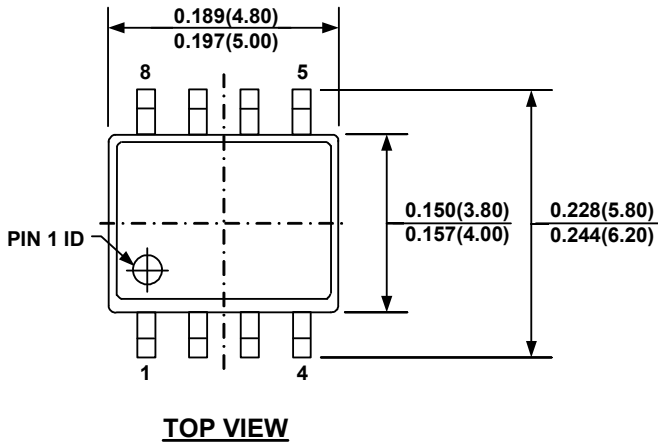
SIDE VIEW



DETAIL "A"

## NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX
- 5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AA
- 6) DRAWING IS NOT TO SCALE

**SOIC8**

**NOTE:**

- 1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
- 5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
- 6) DRAWING IS NOT TO SCALE.

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