MP28163

High Efficiency Single Inductor Buck-Boost Converter with 2.9A Switches

The Future of Analog IC Technology

DESCRIPTION

The MP28163 is a highly efficient, low quiescent current Buck-Boost converter, which operates from input voltage above, below and equal to the output voltage. The device provides power solution for products powered by a one-cell Lithium-Ion or multi-cell alkaline battery applications where the output voltage is within battery voltage range.

The MP28163 uses a current mode, fixed frequency PWM control for optimal stability and transient response. The fixed 1.1MHz switching frequency and integrated low $R_{DS(ON)}$ N-channel and P-channel MOSFETs minimize the solution footprint while maintaining high efficiency.

To ensure the longest battery life MP28163 has an optional pulse skipping mode that reduces switching frequency under light load conditions. For other low noise applications where variable frequency power save mode may cause interference, the logic control input MODE pin forces fixed frequency PWM operation under all load conditions.

The MP28163 operates with input voltage from 2V to 5.5V to provide adjustable output voltage (1.5V to 5V). With an input from 2.7V to 5.5V, it can supply a maximum 1.3A current to load at 3.3V output voltage. The MP28163 is available in small QFN10-3x3mm package.

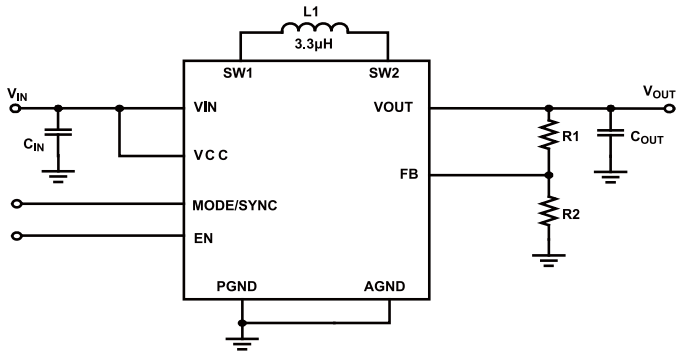
FEATURES

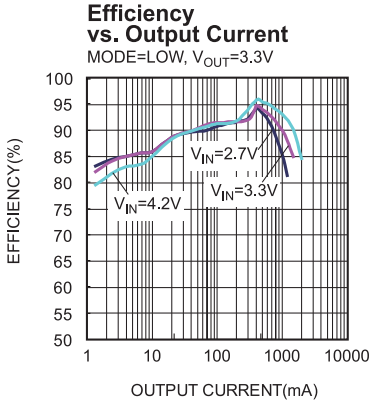
- High efficiency up to 95%.
- Load disconnect during shutdown
- Input voltage range: 2V to 5.5V
- Adjustable output voltage from 1.5V to 5V
- 3.3V/1.3A load capability from 2.7V-to-5.5V V_{IN}
- 1.1MHz switching frequency
- Pulse skipping mode at light load
- Typical 70μA Quiescent current
- Internal loop compensation for fast response
- Internal soft start
- OTP, hiccup SCP
- Available in small 3x3mm QFN10 package

APPLICATIONS

- Battery-powered products
- Portable instruments
- Tablet PCs
- POS systems
- GSM/GPRS

TYPICAL APPLICATION



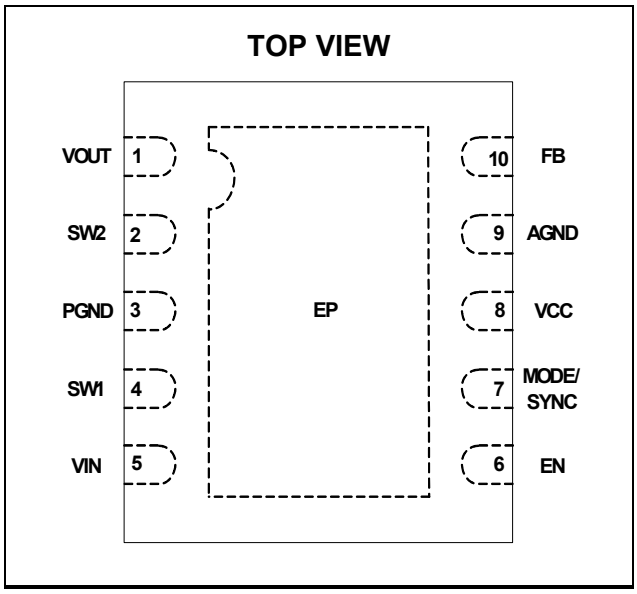


ORDERING INFORMATION

Part Number*	Package	Top Marking
MP28163GQ*	QFN10 (3X3)	AJL

* For Tape & Reel, add suffix –Z (e.g. MP28163GQ–Z);

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

IN to GND .....–0.3V to 6.5V
SW1/2 to GND .....–0.3V(-2V for <10ns) to 6.5V
All Other Pins.....–0.3V to 6.5 V
Junction Temperature.....150°C
Lead Temperature .....260°C
Continuous Power Dissipation (T_A = +25°C) (2)
QFN10 3X3mm..... 2.5W
Storage Temperature..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} .....2V to 5.5V
Output Voltage V_{OUT}.....1.5V to 5V
Operating Junct. Temp. (T_J).... –40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
3X3 QFN10	50	12	°C/W

Notes:

1) Exceeding these ratings may damage the device
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = V_{CC}=V_{EN}=3.3V, T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Under voltage lockout threshold	V_{UVLO}	V_{CC} rising		1.8	1.9	V
		V_{CC} falling		1.7		V
Feedback voltage	V_{FB}		486	496	506	mV
Oscillator frequency	F_{REQ}		900	1100	1300	kHz
Frequency range for synchronization			1000		2000	kHz
Primary current limit	Isw		2.25	2.9		A
Secondary current limit				1.8		A
NMOS switch on resistance	$R_{DS(ON)}$-N			85		mΩ
PMOS switch on resistance	$R_{DS(ON)}$-P			100		mΩ
Quiescent current	I_Q	V_{FB}=0.65V		70	85	μA
Shutdown current	I_S	V_{EN}=0V			1	μA
MODE input low voltage					0.4	V
MODE input high voltage			1.2			V
EN input low voltage					0.4	V
EN input high voltage			1.2			V
EN input current	I_{EN}	V_{EN}=3.3V		3.1		μA
		V_{EN}=0V		0		μA
Thermal shutdown(5)	T_{SHDN}			160		℃
Thermal shutdown hysteresis(5)	T_{HYS}			20		℃

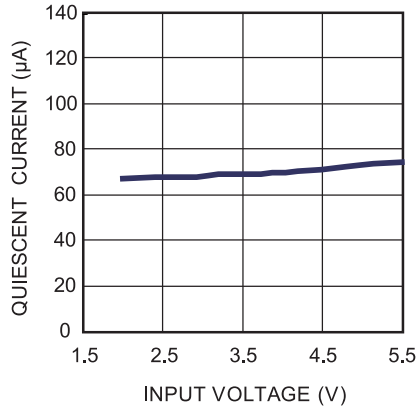
Notes:

5) Guaranteed by engineering sample Characterization, not tested in production.

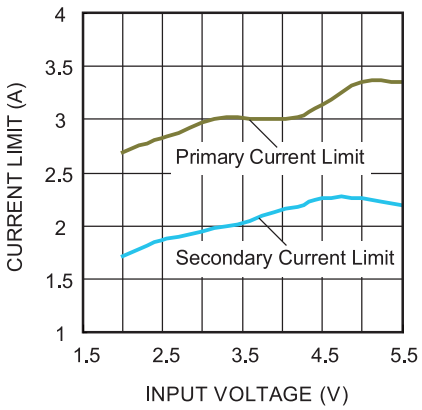
TYPICAL CHARACTERISTICS

V_{IN} = 3.3V, V_{OUT} = 3.3V, L = 3.3µH, C_{OUT}=2x22uF, T_A = +25ºC, unless otherwise noted.

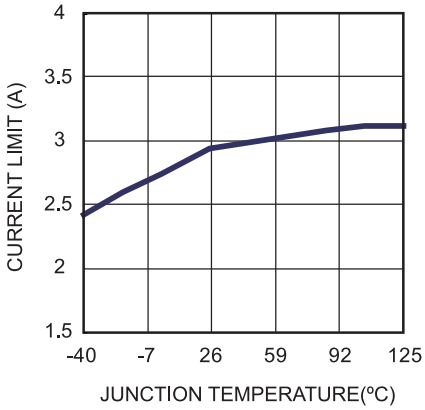
Quiescent Current
V_{FB}=0.65V



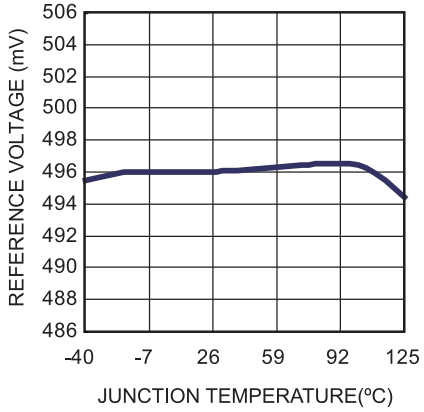
Current Limit vs. Input Voltage



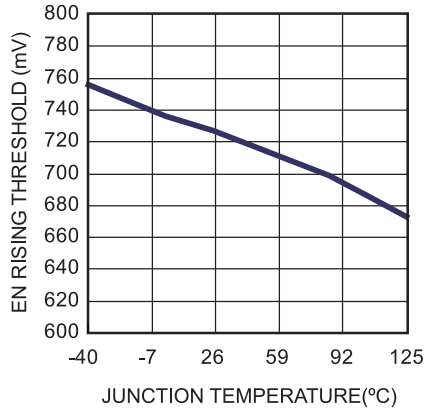
Primary Current Limit vs. Temperature



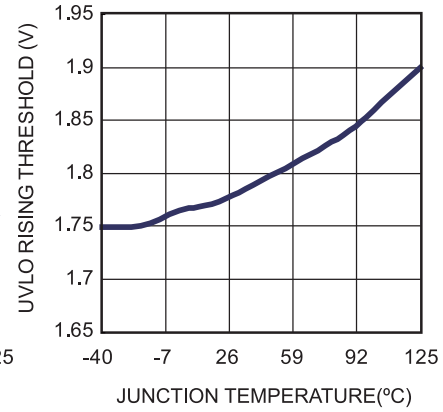
Referenve Voltage vs. Temperature



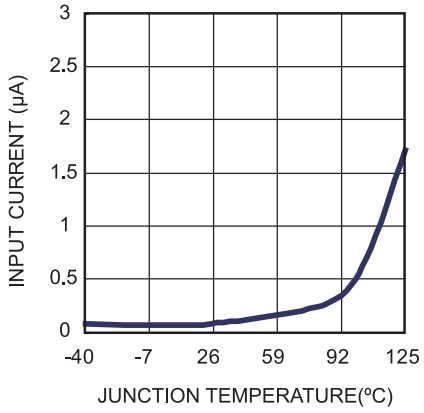
EN Rising Threshold vs. Temperature



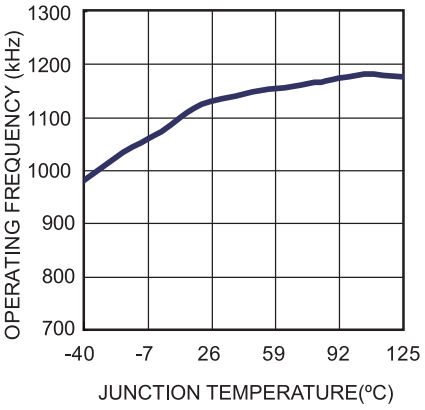
VIN UVLO Rising Threshold vs. Temperature



Disabled Supply Current vs. Temperature
V_{EN}=0V



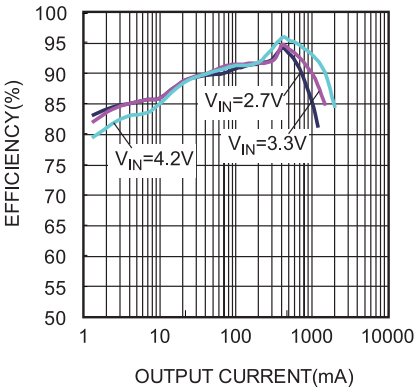
Frequency vs. Temperature
I_{OUT}=0A



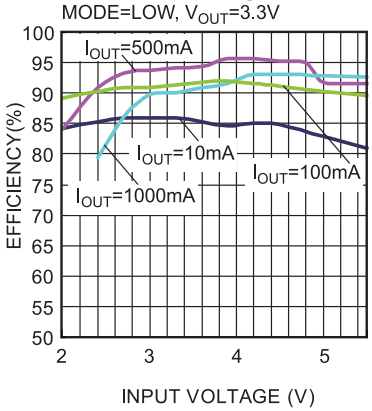
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.3V, V_{OUT} = 3.3V, L = 3.3µH, C_{OUT}=2x22uF, T_A = +25ºC, unless otherwise noted.

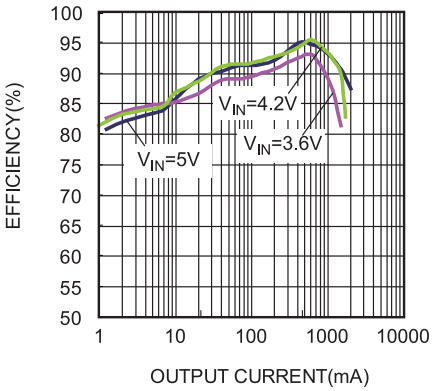
Efficiency vs. Output Current
MODE=LOW, V_{OUT}=3.3V



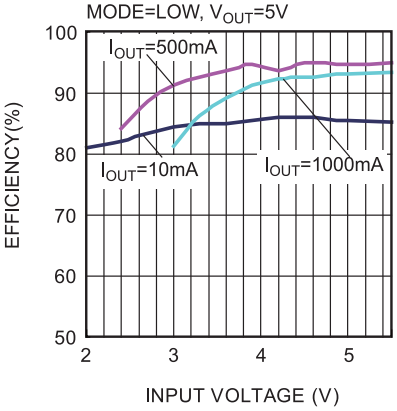
Efficiency vs. Input Voltage
MODE=LOW, V_{OUT}=3.3V



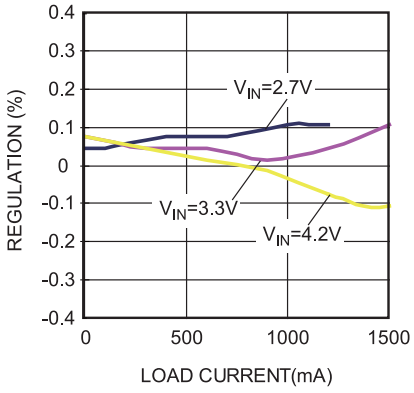
Efficiency vs. Output Current
MODE=LOW, V_{OUT}=5V



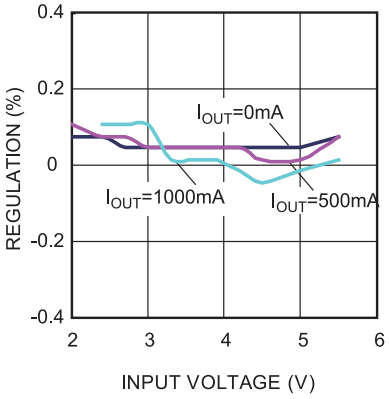
Efficiency vs. Input Voltage
MODE=LOW, V_{OUT}=5V



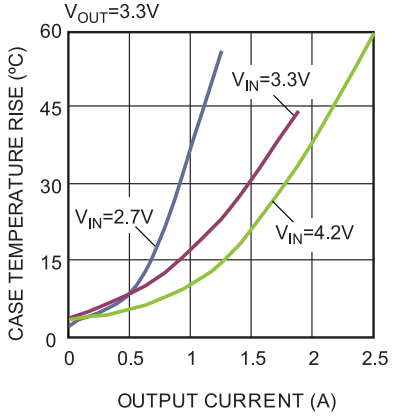
Load Regulation
MODE=HIGH



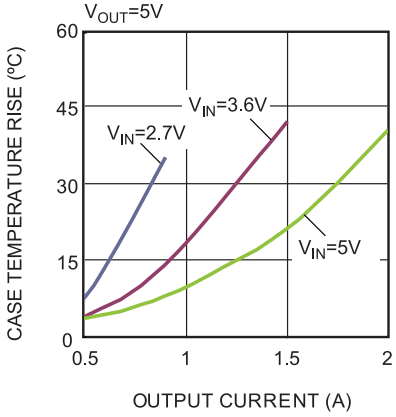
Line Regulation
MODE=HIGH



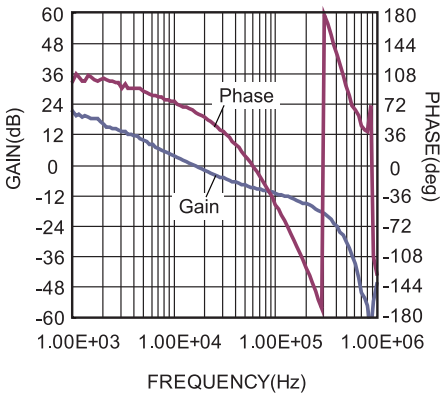
Case Temperature Rise vs. Output Current
V_{OUT}=3.3V



Case Temperature Rise vs. Output Current
V_{OUT}=5V



Loop Gain vs. Frequency
V_{IN}=2.4V, I_{OUT}=0.8A

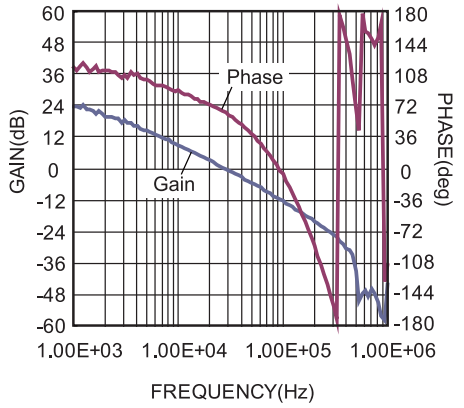


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 3.3V, L = 3.3µH, C_{OUT}=2x22uF, T_A = +25°C, unless otherwise noted.

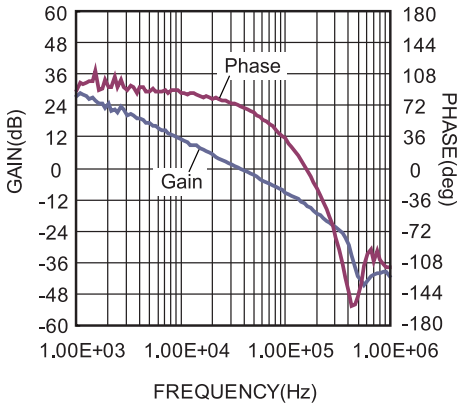
Loop Gain vs. Frequency

V_{IN}=3.3V, I_{OUT}=1A



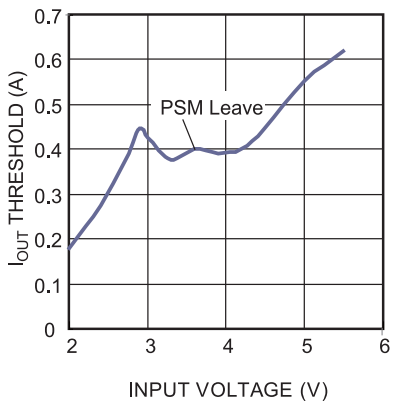
Loop Gain vs. Frequency

V_{IN}=4.2V, I_{OUT}=1.5A

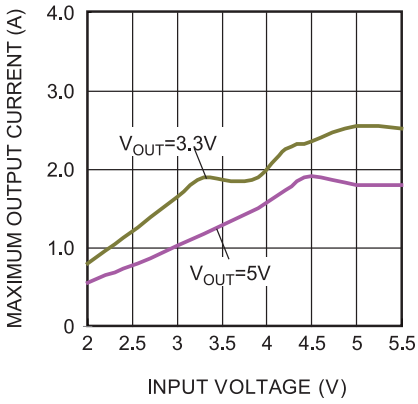


PSM to PWM Transition Threshold

MODE=LOW



Output Current Capability vs. Input (6)



Notes:

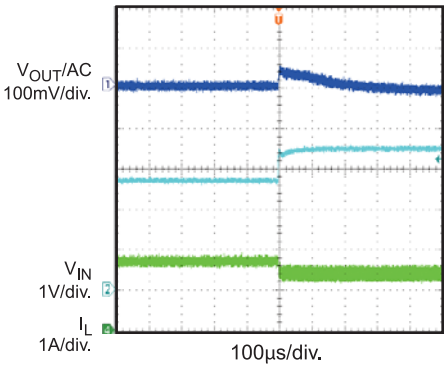
6) Tested with 2.25A inductor peak current at 3.3V input point. Under other VIN conditions, it takes the same current limit variation trend with VIN into consideration as “Current Limit vs. Input Voltage” curve shows". Some margin is recommended for max load design。

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 3.3V, L = 3.3µH, C_{OUT}=2x22uF, T_A = +25°C, unless otherwise noted.

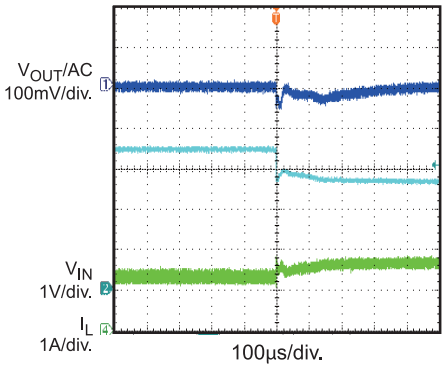
Line Transient Response

V_{IN}=2.4V-->3.3V, I_{OUT}=1A



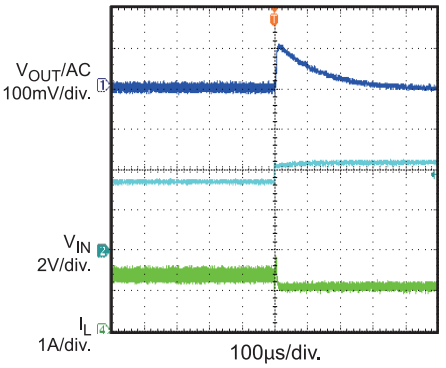
Line Transient Response

V_{IN}=3.3V-->2.4V, I_{OUT}=1A



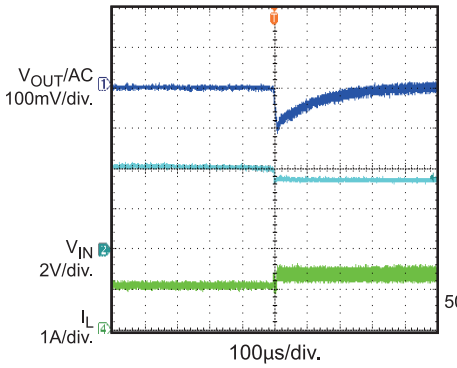
Line Transient Response

V_{IN}=3.3V-->4.2V, I_{OUT}=1A



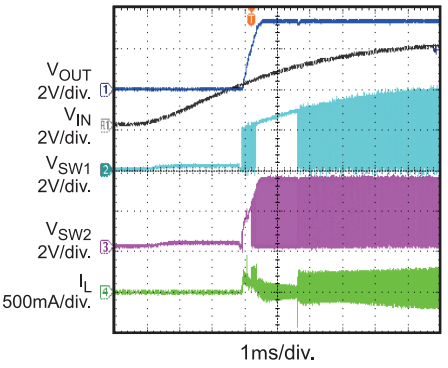
Line Transient Response

V_{IN}=4.2V-->3.3V, I_{OUT}=1A



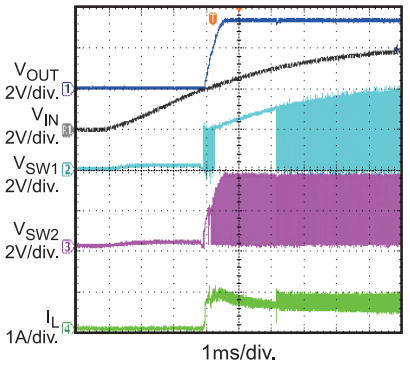
Power Up

V_{IN}=4.2V, I_{OUT}=0A, MODE=HIGH



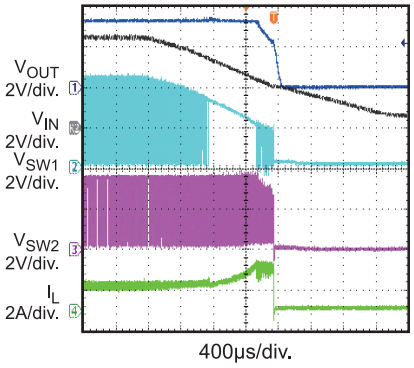
Power Up

V_{IN}=4.2V, I_{OUT}=0.5A, MODE=HIGH



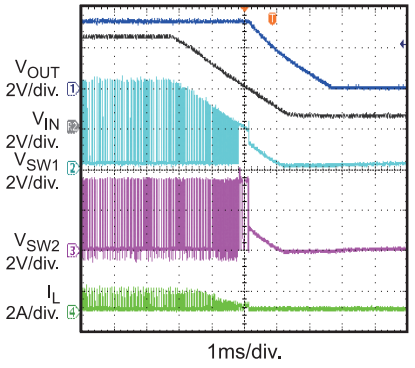
Power Off

V_{IN}=4.2V, I_{OUT}=1A, MODE=HIGH



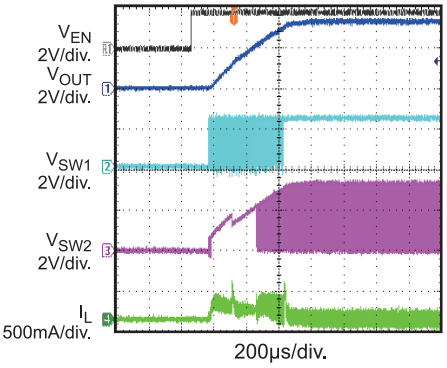
Power Off

V_{IN}=4.2V, I_{OUT}=0.05A, MODE=LOW



EN Start Up

V_{IN}=2.4V, I_{OUT}=0A, MODE=HIGH

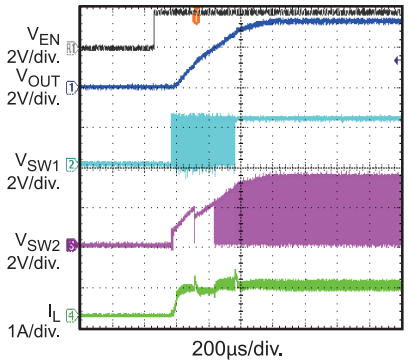


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 3.3V, L = 3.3µH, C_{OUT}=2x22uF, T_A = +25°C, unless otherwise noted.

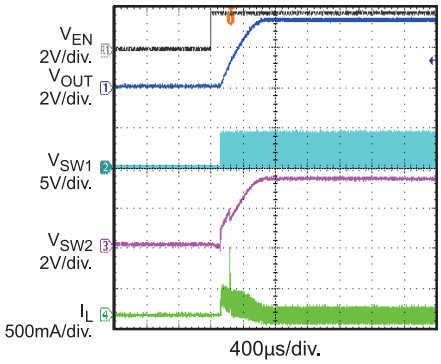
EN Start Up

V_{IN}=2.4V, I_{OUT}=0.5A, MODE=HIGH



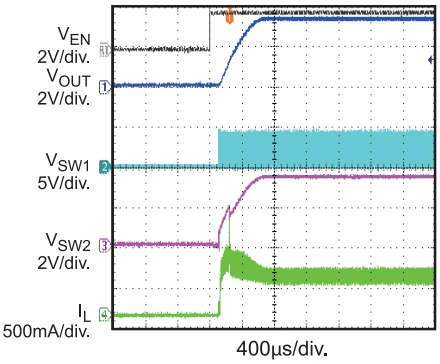
EN Start Up

V_{IN}=4.2V, I_{OUT}=0A, MODE=HIGH



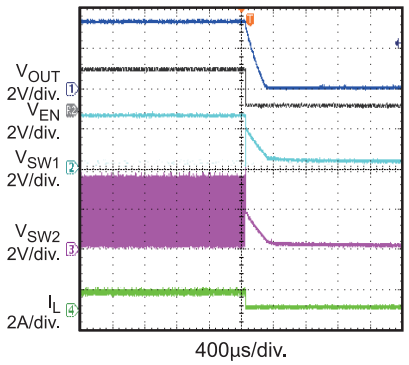
EN Start Up

V_{IN}=4.2V, I_{OUT}=0.5A, MODE=HIGH



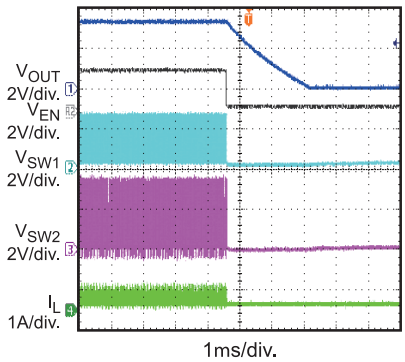
EN Shutdown

V_{IN}=2.4V, I_{OUT}=0.5A, MODE=HIGH



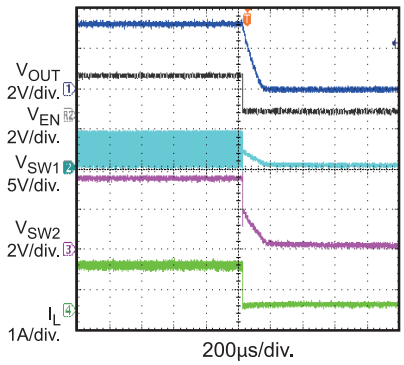
EN Shutdown

V_{IN}=2.4V, I_{OUT}=0.05A, MODE=LOW



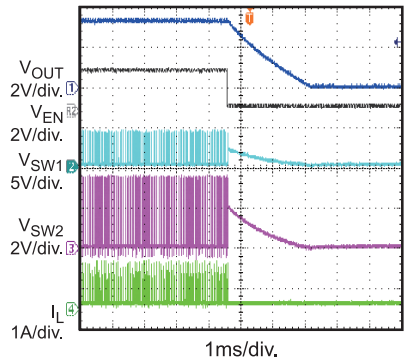
EN Shutdown

V_{IN}=4.2V, I_{OUT}=1A, MODE=HIGH



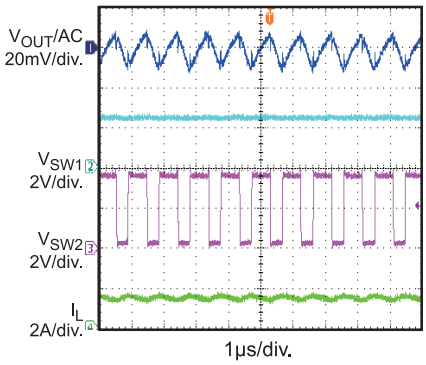
EN Shutdown

V_{IN}=4.2V, I_{OUT}=0.05A, MODE=LOW



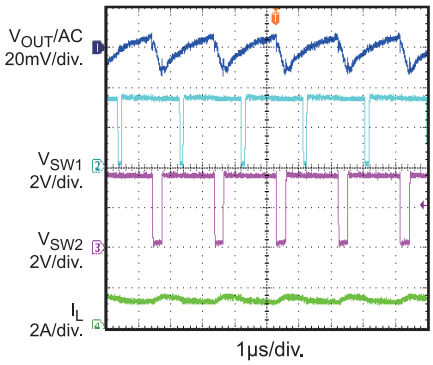
Steady State

V_{IN}=2.4V, I_{OUT}=0.8A, MODE=HIGH



Steady State

V_{IN}=3.3V, I_{OUT}=1A, MODE=HIGH

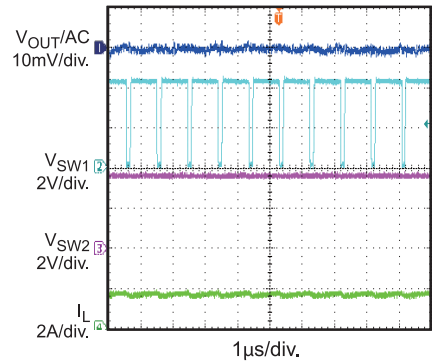


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 3.3V, L = 3.3µH, C_{OUT}=2x22uF, T_A = +25ºC, unless otherwise noted.

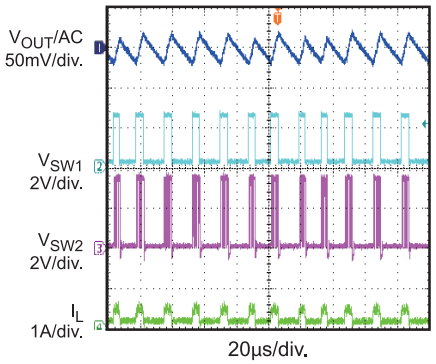
Steady State

V_{IN}=4.2V, I_{OUT}=1.5A, MODE=HIGH



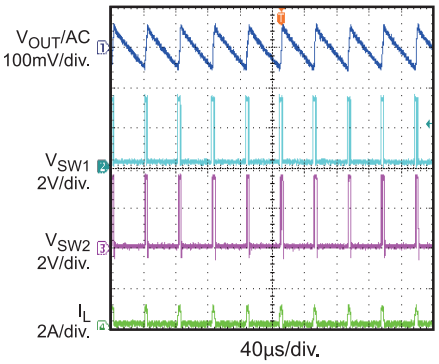
Steady State

V_{IN}=2.4V, I_{OUT}=0.05A, MODE=LOW



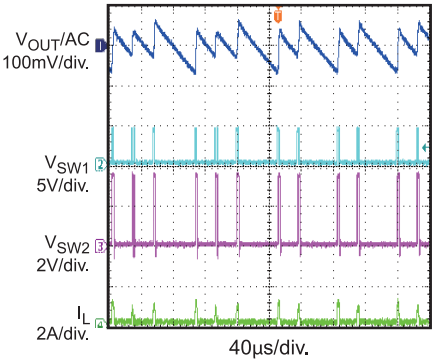
Steady State

V_{IN}=3.3V, I_{OUT}=0.05A, MODE=LOW



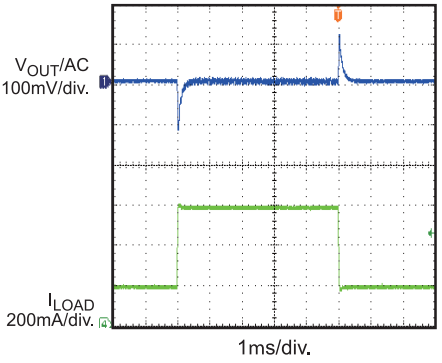
Steady State

V_{IN}=4.2V, I_{OUT}=0.05A, MODE=LOW



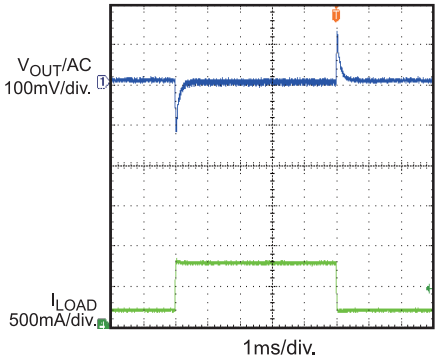
Load Transient Response

V_{IN}=2.4V, I_{OUT}=0.2-->0.6A@250mA/µs, MODE=HIGH



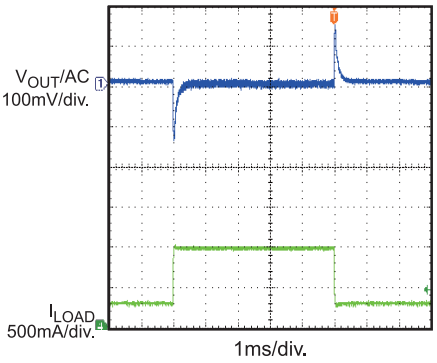
Load Transient Response

V_{IN}=3.3V, I_{OUT}=0.2-->0.8A@250mA/µs, MODE=HIGH



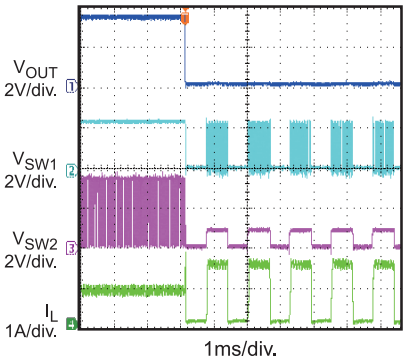
Load Transient Response

V_{IN}=4.2V, I_{OUT}=0.3-->1A@250mA/µs, MODE=HIGH



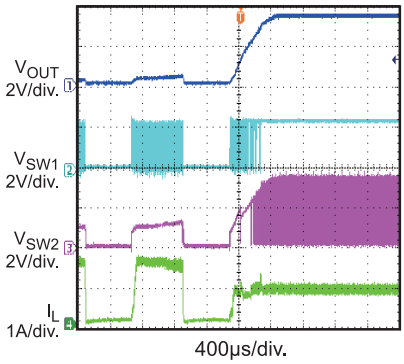
SCP Entry

Vin=2.4V, Io=0.5A, MODE=HIGH



SCP Recovery

V_{IN}=2.4V, I_{OUT}=0.5A, MODE=HIGH

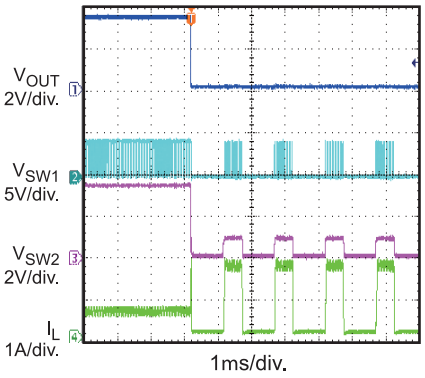


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 3.3V, L = 3.3µH, C_{OUT}=2x22uF, T_A = +25ºC, unless otherwise noted.

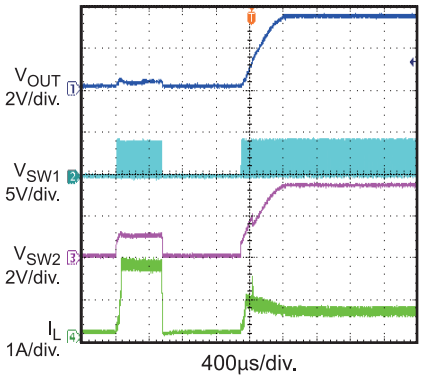
SCP Entry

V_{IN}=4.2V, I_{OUT}=0.5A, MODE=HIGH



SCP Recovery

V_{IN}=4.2V, I_{OUT}=0.5A, MODE=HIGH



PIN FUNCTIONS

Pin #	Name	Description
1	VOUT	Buck-Boost converter output.
2	SW2	Switch pin-Internal switches are connected to this pin. Connect inductor between SW1 and SW2.
3	PGND	Power ground.
4	SW1	Switch pin-Internal switches are connected to this pin. Connect inductor between SW1 and SW2.
5	VIN	Supply voltage for power stage.
6	EN	ON/OFF control, it's not recommended to leave this pin float.
7	MODE/ SYNC	Operation mode selection. If MODE pin is low, the MP28163 automatically switches between PSM and fixed frequency PWM according to the load level. If MODE pin is pulled high, the MP28163 works always in PWM mode. External clock can be applied to MODE pin for changing switching frequency. This pin is sensitive to noise, so it should be strongly pulled up above 1.2V or pulled down below 0.4V. Must NOT leave it float.
8	VCC	Supply voltage for control stage.
9	AGND	Signal ground, should be connected to PGND externally.
10	FB	Feedback to set output voltage. Keeps this pin and associated trace far from noise source like SW.
-	EP	Thermal pad, which is recommended to connected to PGND.

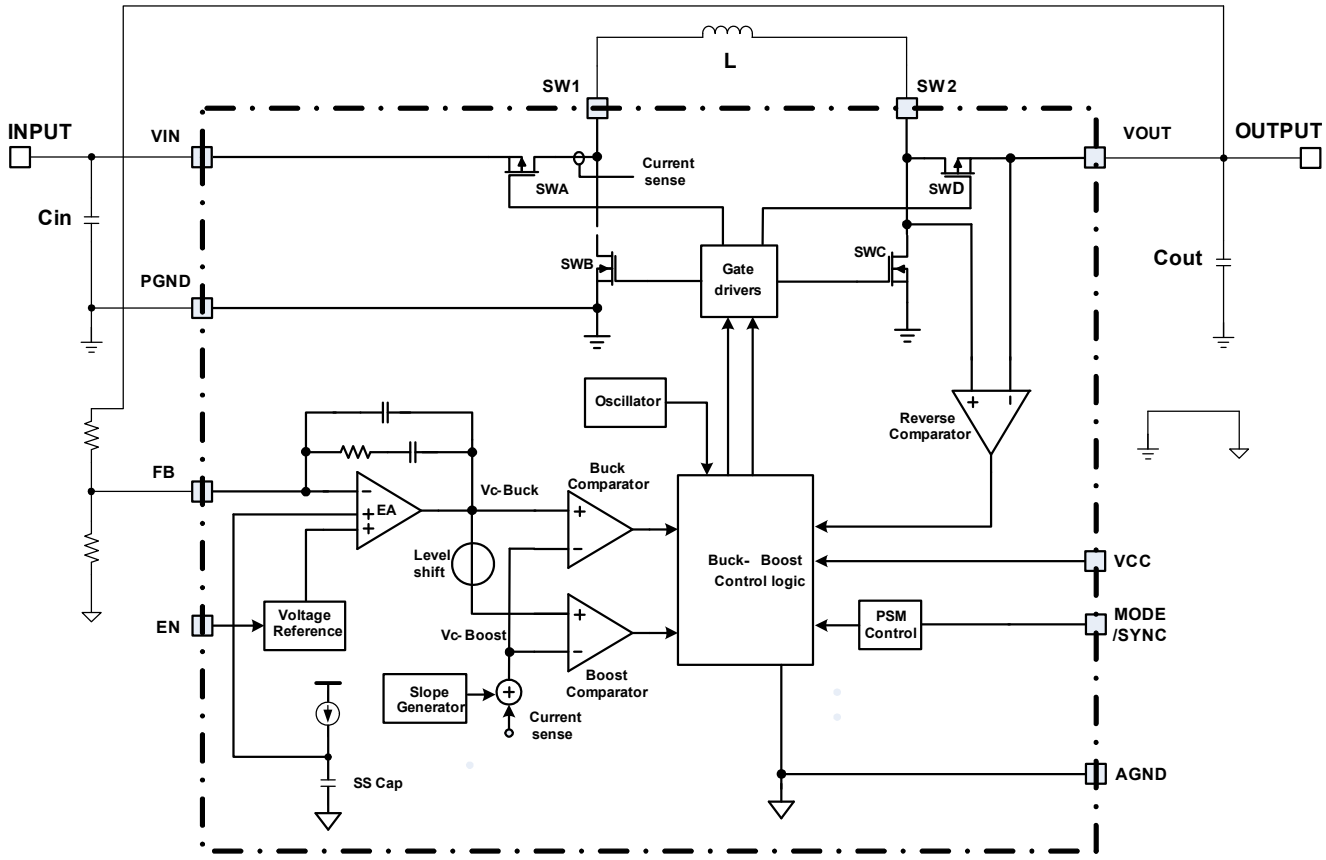


Figure 1— Function Block Diagram

OPERATION

The MP28163 is a high efficiency, dual mode buck-boost converter that provides output voltage above, equal to or below the input voltage. When the MODE pin is held high, the MP28163 operates in constant-frequency PWM mode with peak current mode control. As shown in Figure 1, the output voltage is sensed via the FB pin through an external resistor-divider from the output to ground. The voltage difference between FB pin and the internal reference is amplified by error amplifier to generate control signal $V_{C\text{-}Buck}$. By comparing $V_{C\text{-}Buck}$ with internal compensation ramp (the sensed SWA's current with slope compensation) through Buck comparator, a PWM control signal for PWM buck mode is outputted. Another control signal $V_{C\text{-}Boost}$ is derived from $V_{C\text{-}Buck}$ through level shift. Similarly, $V_{C\text{-}Boost}$ compares with the same ramp signal through Boost comparator and generates the PWM control signal for PWM boost mode. The switch topology for the buck-boost converter is shown in Figure 2.

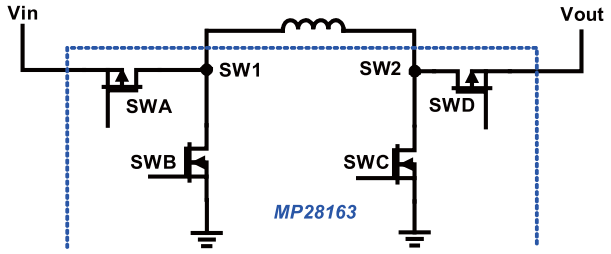


Figure 2—Buck-Boost Switch Topology

Buck Region ($V_{IN} > V_{OUT}$)

When the input voltage is significantly greater than output voltage, which means the converter can deliver energy to load within the maximum duty cycle of SWA, so the converter operates in buck mode. The control signal $V_{C\text{-}Boost}$ is always lower than compensation ramp because Buck can deliver enough energy to load, thus switch D turns on constantly and switch C remains off. Meanwhile, $V_{C\text{-}Buck}$ compares with compensation ramp normally and generates PWM signal, therefore, switches A and B are pulse-width-modulated to produce the required duty cycle to support the output voltage.

Buck-Boost Region ($V_{IN} \approx V_{OUT}$)

When Vin is close to Vout, due to duty cycle limit of SWA the converter isn't able to provide wanted energy to load. In this case SWA will be turned on over all the period, that is, there is no BD operation(SWB and SWD being turned on simultaneously). Now a new period begins. Since there is no BD in last period, an offset voltage is added to the ramp signal to make the ramp signal easily hit $V_{C\text{-}Buck}$. At the same time due to loop regulation $V_{C\text{-}Boost}$ (as well as $V_{C\text{-}Buck}$) rises to some level, so that the ramp signal can intersect it to produce the PWM driving signal for Boost operation. After SWC is turned off the ramp signal continues rising (the actual inductor current may rise or fall depending on the difference between Vin and Vout), when the ramp intersects $V_{C\text{-}Buck}$, PWM signal for Buck operation then is generated. Now the buck's duty cycle is within its limit, so there is BD operation in current period, which means next period the offset voltage will be removed. This is the so-called buck-boost region. With heavy load due to voltage drop on switches the actual input range for this region may be a little wide.

Boost Region ($V_{IN} < V_{OUT}$)

When the input voltage is significantly lower than output voltage, the converter operates in boost mode. The control signal $V_{C\text{-}Buck}$ is always higher than compensation ramp even with the offset voltage always added, thus switch A turns on continuously and switch B remains off. Meanwhile, $V_{C\text{-}Boost}$ compares compensation ramp normally and generates PWM signal, therefore, switches C and D are pulse-width-modulated to produce the required duty cycle to support the output regulation voltage.

PSM

When Mode Pin is pulled down below the low level threshold, the MP28163 will automatically enter PSM if load is light. When working in PSM, a train of SW pulses are initiated by a Boost operation, and ended with BD operation. During this process, SWD will be turned off if inductor current is below about 100mA. In actual

waveforms the current may be much lower than this value when SWD is turned off because of internal delay.

SCP/OCP vs. two current limits

There are two current limits in MP28163. The primary one is for steady PWM operation and it's typically 2.9A at 3.3V input.; The secondary one is for limiting inrush current at startup, it's typically 1.6A to 1.9A, depending on Vin, too. When load is over heavy, the primary limit would protect MP28163 from being over thermal. Therefore Vout would drop due to OCP. If Vout drops below 0.6 times normal output, a hiccup period is initiated to protect MP28163. this is the SCP. In hiccup period, SWA and SWC are turned off while SWB and SWD are turned on. After the hiccup period ends, a soft re-startup begins. Because Vout is below 1V (due to over load or output short), the secondary current takes charge of this process. After Vo rises above 1V, primary current limit get in charge of. Now if load is still over heavy (or output short still exists) such that after SS ends Vout is still below $0.6*V_{OUT\_NORMAL}$ and current hits one of the limits, another hiccup period begins. However if the load recovers to normal value during re-startup so that current doesn't hit its limit, or, Vout already rises above $0.6*V_{OUT\_NORMAL}$, the re-startup succeeds, and MP28163 enter normal operation.

As to the input/EN startup, the cases are same as the SCP recovery process.

Enable

The MP28163 has a dedicated enable control pin (EN). The device operates when it is set high. If it is set low the device stops switching, all the internal blocks are turned off. Tie EN to Vin through a resistor for automatic start up. Due to EN bias or leakage current, the value of this resistor should be set to provide EN pin with a current above 10uA. Any signal to drive this pin should be limited to 100uA if the maximum voltage of this signal is above 6.5V.

Internal Soft-start

When EN pin is pulled high, and at the same time the voltage on Vcc pin is above its UVLO rising threshold MP28163 will start up with Soft-start function to eliminate output overshoot. Soft-start also functions during SCP recovery.

Under-Voltage Lockout

The under voltage lockout (UVLO) is implement to protect the device from improper operating at insufficient supply voltage. When the supply voltage at VCC is below the UVLO threshold the device is in shutdown mode. The UVLO rising threshold is about 1.8V with 200mV hysteresis.

Over-Temperature Protection

An internal temperature sensor continuously monitors the IC junction temperature. If the IC temperature exceeds 160ºC typically the device stops operating. As soon as the temperature falls below 140 ºC typically normal operation is restored.

APPLICATION INFORMATION

Setting the Output Voltage

To use MP28163 correctly, A resistor divider must be connected between Vout and GND, and the middle point of the divider connected to FB pin as shown in Typically Application on page 1.

$$R1 = (\frac{V_{OUT}}{V_{FB}} - 1) \times R2 \quad (1)$$

High R2 resistance (eg. 100kΩ) can reduce the power consumption, while lower than 1MΩ resistance is recommended for R1 for good output accuracy.

Inductor Selection

The inductor is the key passive component for switching converters. With a buck-boost device, the inductor selection affects the boundary conditions in which the converter works, as buck at the maximum input voltage and as a boost at the minimum input voltage.

Two critical inductance values are then obtained according to the following formulas.

$$L_{MIN-BUCK} = \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times F_{REQ} \times \Delta I_L} \quad (2)$$

$$L_{MIN-BOOST} = \frac{V_{IN(MIN)} \times (V_{OUT} - V_{IN(MIN)})}{V_{OUT} \times F_{REQ} \times \Delta I_L} \quad (3)$$

Where:

F_{REQ}: minimum switching frequency

ΔI_L: the peak-to-peak inductor ripple inductor current. As a rule of thumb, the peak-to-peak ripple can be set at 10%-20% of the output current.

The minimum inductor value for the application is the higher one between Equation 2 and Equation 3. In addition to the inductance value the maximum current the inductor can handle must be calculated in order to avoid saturation.

$$I_{PEAK-BUCK} = \frac{I_{OUT}}{\eta} + \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{2 \times V_{IN(MAX)} \times F_{REQ} \times L} \quad (4)$$

$$I_{PEAK-BOOST} = \frac{V_{OUT} \times I_{OUT}}{\eta \times V_{IN(MIN)}} + \frac{V_{IN(MIN)} \times (V_{OUT} - V_{IN(MIN)})}{V_{OUT} \times F_{REQ} \times L} \quad (5)$$

Where η is the estimated efficiency of MP28163. The maximum of the two values above must be considered when selecting the inductor.

Input and Output Capacitor Selection

It is recommended to use ceramic capacitors with low ESR as input and output capacitors in order to filter any disturbance present in the input line and to obtain stable operation.

Minimum values of 10uF for both capacitors are needed to achieve good behavior of the device.

The input capacitor must be placed as close as possible to the device.

Other Consideration

MP28163 employs the classic hiccup mode for SCP. This method has an inherited drawback: if the output short is released at a time closed to SS end, then Vo would has overshoot. To attenuate Vo overshoot at SCP recovery, a forward RC series can be connected in parallel with high side resistor of FB divider, as R3 and C5 in Figure 5 shows. The RC acts as a soft startup when Vo short is released at the time of internal SS's end.

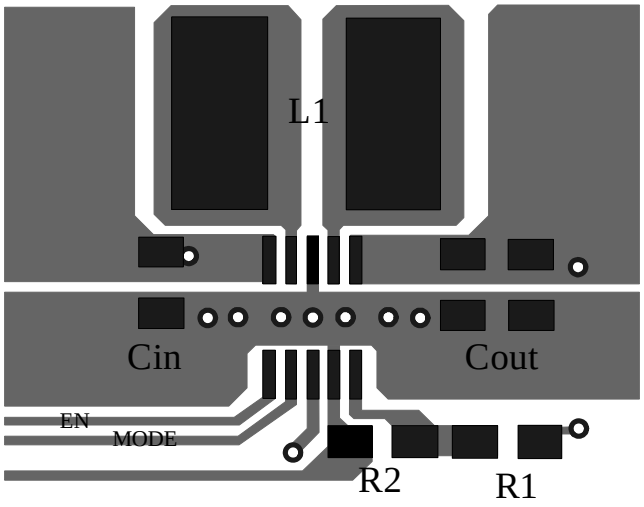
PCB Layout Guide

1. Input and output capacitors should be close to MP28163's Vin, Vout and PGND pins.

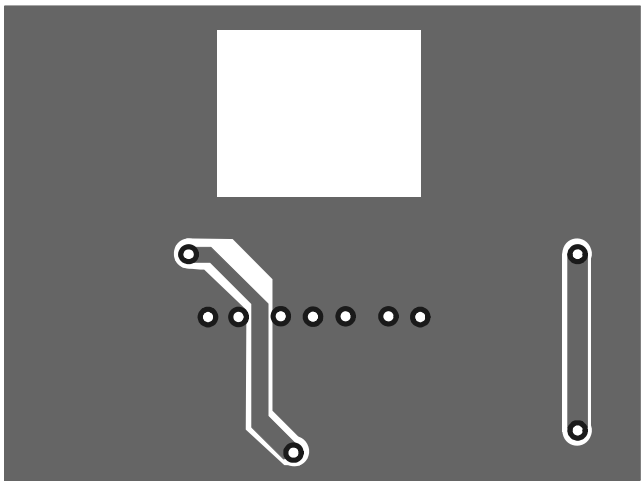
2. The wire connecting input capacitor to Vcc pin should be as short as possible. For better performance in noisy environment, an additional capacitor very close to Vcc pin can be used to bypass noise for Vcc.

3. FB resistor divider should be very close to FB pin, and keep FB trace far away from noise.

Figure 3 shows an example of PCB layout for which the reference schematic is shown on Figure 4.



Top Layer



Bottom Layer

Figure 3—PCB Layout

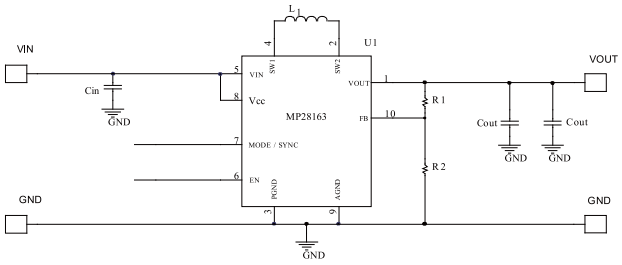


Figure 4—Reference Circuit for PCB Guide

Design Example

Below is a design example following the application guidelines for the specifications:

Table 1: Design Example

V_{IN} (V)	2-5.5
V_{OUT} (V)	3.3V

The detailed application schematic is shown in Figure 5 and its performance can be found in TPC section.

TYPICAL APPLICATION CIRCUITS

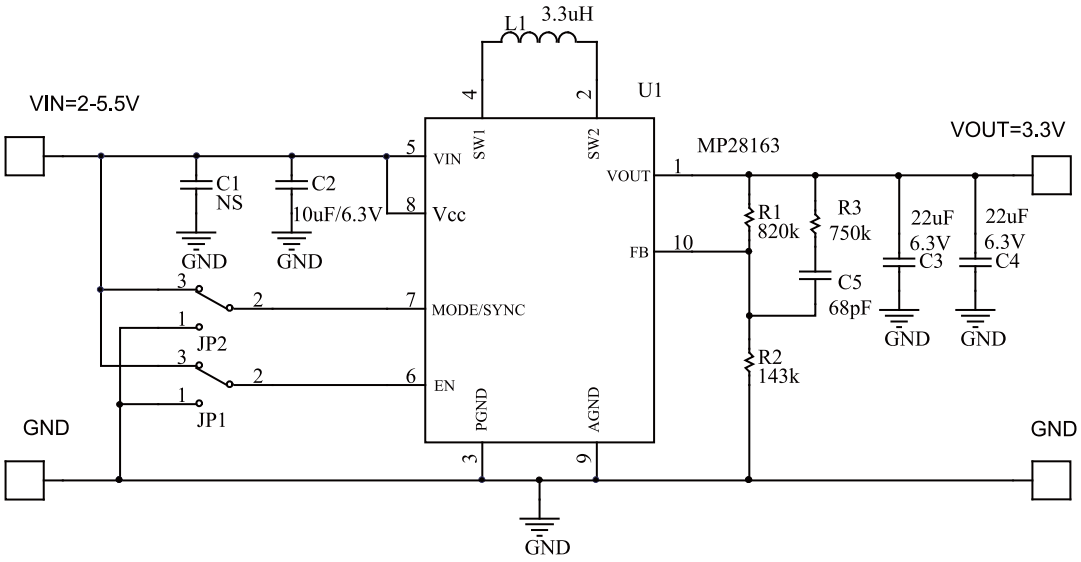


Figure 5—3.3V Output Application Circuit

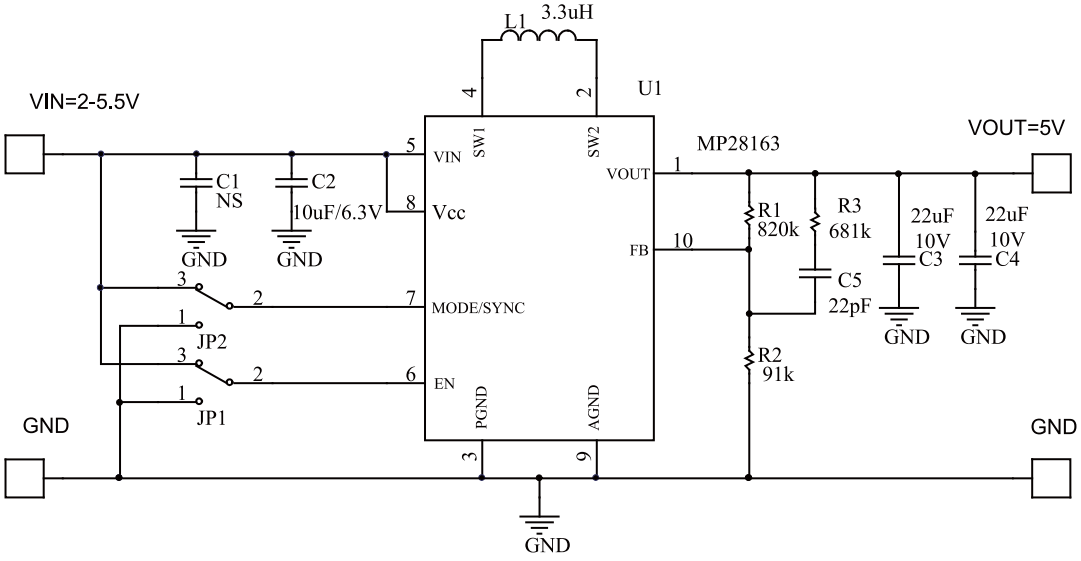
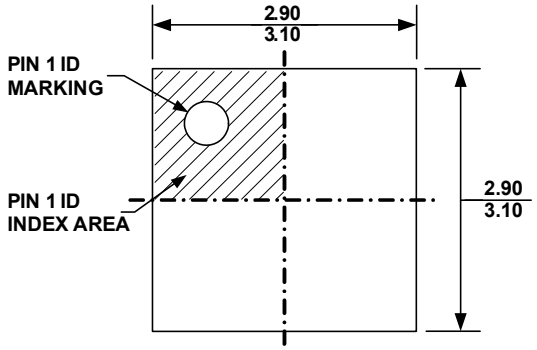


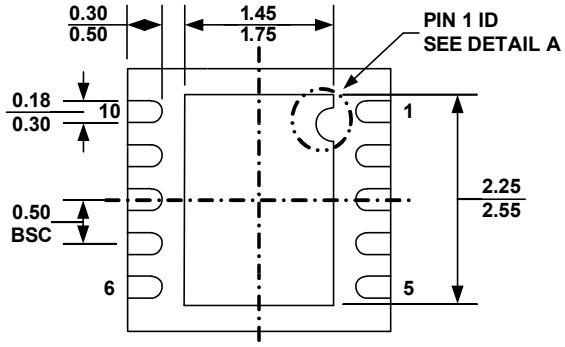
Figure 6—5V Output Application Circuit

PACKAGE INFORMATION

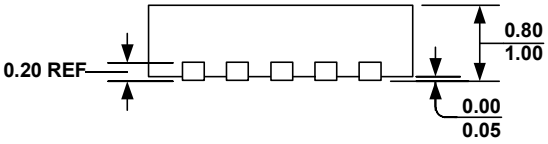
QFN10 (3mmX3mm)



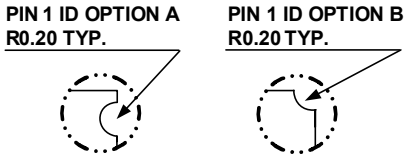
TOP VIEW



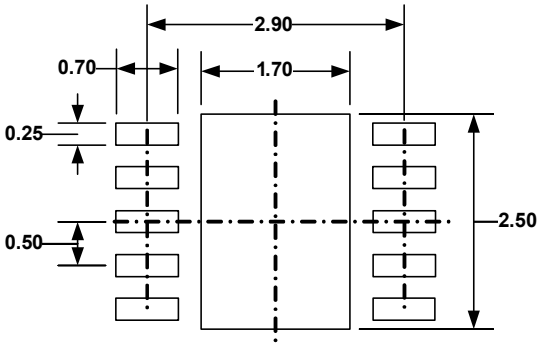
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX
4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VEED-5.
5) DRAWING IS NOT TO SCALE