ZL40804

6 GHz Fixed Modulus ÷ 4

Data Sheet

March 2006

Features

- 3.45 V Single Supply Operation
- Low Power Dissipation: 210 mW typ
- Broadband: DC to 6 GHz
- SSB Phase Noise: –148 dBc/Hz @ 10 KHz
- Pout 3 dBm

Prescaler Modulus

- ZL40804 – Divide by 4

Applications

- DC to 6 GHz PLL applications
- HyperLan
- LMDS
- Instrumentation
- Satellite Communications
- Fibre Optic Communications; OC48, OC192
- Ultra Low Jitter Clock Systems

Ordering Information

ZL40804/DCA	8 pin SOIC	Tubes
ZL40804/DCB	8 pin SOIC	Tape and Reel
ZL40804DCE1	8 Pin SOIC*	Trays, Bake & Drypack
ZL40804DCF1	8 Pin SOIC*	Trays, Bake & Drypack

*Pb Free Matte Tin

-40°C to +85°C

Description

The ZL40804 are Bipolar 3.45 V supply, very low power prescalers for professional applications with a fixed modulus of 4. The ultra low close in (10 KHz offset) SSB phase noise performance is ideal for narrow band communications systems or systems with ultra low jitter budgets such as next generation fibre optic communications. The devices are broadband from DC to 6 GHz.

See Figure 1 and Application Note for RF Prescalers for more details.

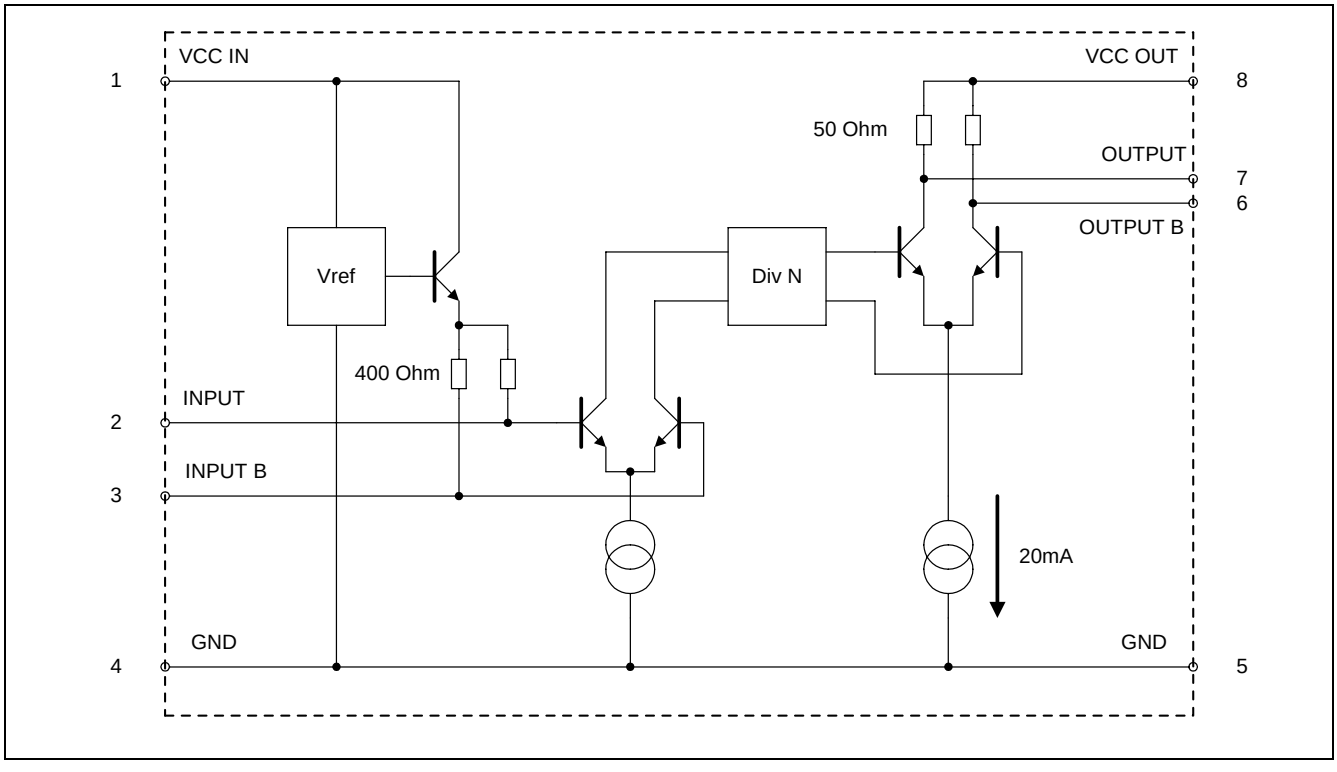


Figure 1 - Functional Block Diagram

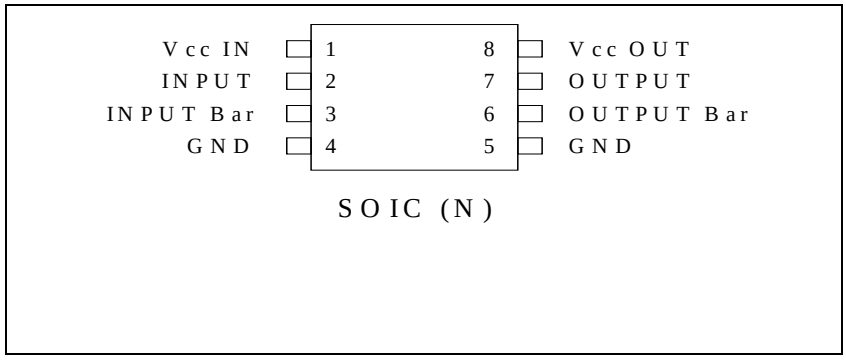


Figure 2 - Pin Connections – Top View

Application Configuration

Figure 3 shows a recommended application configuration. This example shows the device set up for single ended operation.

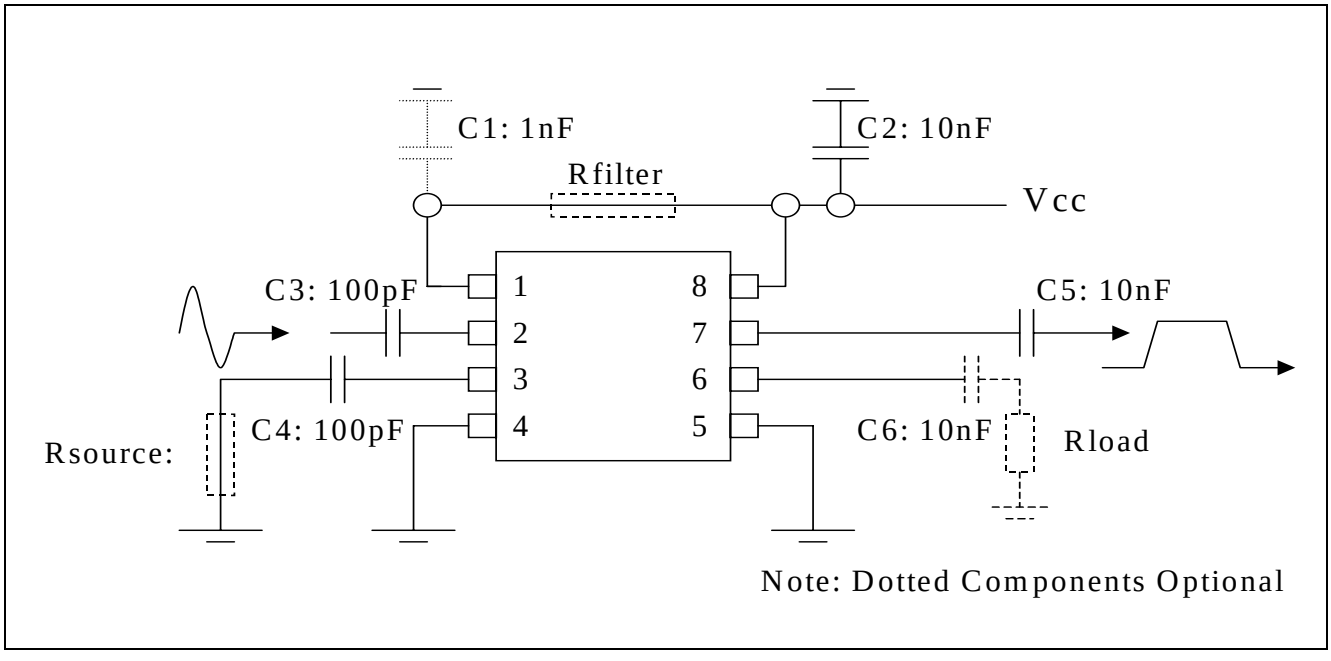


Figure 3 - Recommended Circuit Configuration

This represents the circuit used to complete characterization. The tabulated Electrical performance is guaranteed using this application circuit.

Unpopulated evaluation boards are available, type No. ZLE40008. A fully populated evaluation board is also available, type No. ZLE40804.

Circuit Options

The application circuit includes some optional components that may be required to improve tolerance of system noise present in the application.

Dummy R source may be added to the inverting input to provide a better matched source impedance at the input. This will improve the rejection of common mode noise present within the system.

Dummy R load may be added to the inverting output to provide better matched load at the output. This will reduce the radiated EMI at the output and reduce the Output Noise present on the supply rail.

Rfilter can be inserted between the Vcc_In and the Vcc_out to provide additional filtering to the input Vcc. The input Vcc powers the input bias reference only and can be a sensitive point to system noise. The nominal input current at Vcc_In is 0.35 mA. An alternative would be to use an inductive choke.

C1 is additional Supply Filtering and should be added with Rfilter. The IC includes 10pF of on Chip Supply Filtering.

Input & Output Circuit

Figure 4 shows the equivalent input and output circuit.

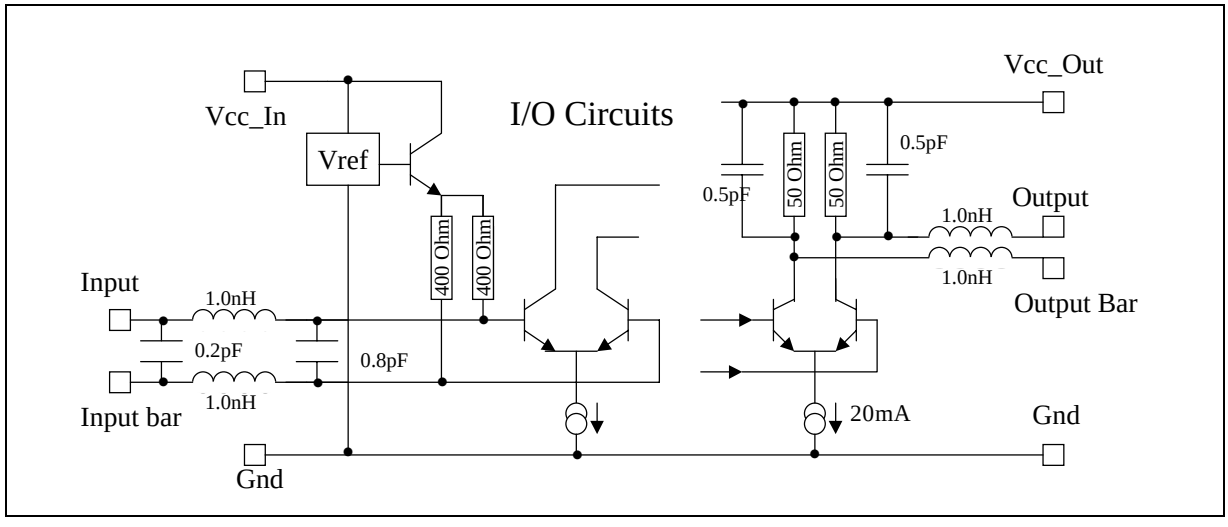


Figure 4 - Input and Output Equivalent Circuit

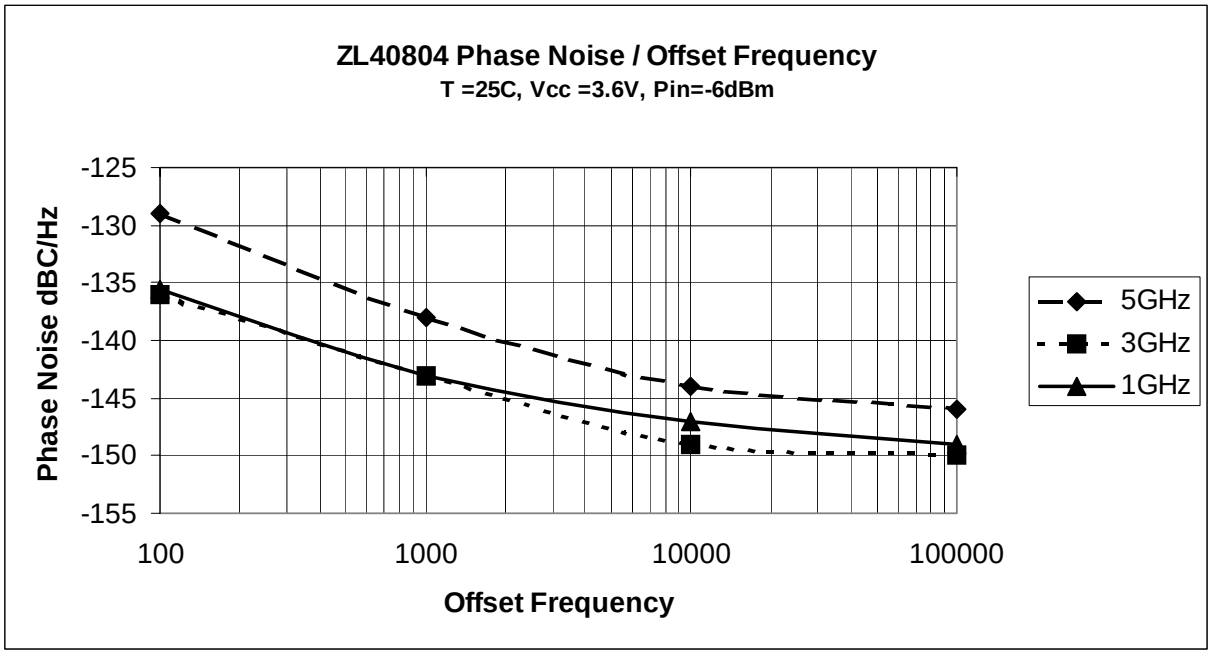


Figure 5 - ZL40804 Typical Phase Noise

Absolute Maximum Ratings

	Parameter	Symbol	Min.	Max.	Units	Comments
1	Supply voltage	Vcc	- 0.5	6	V	
2	RFin			12	dBm	
3	All I/O ports		-0.5	Vcc+0.5	V	
4	Storage temperature	T_{ST}	-55	150	°C	
5	ESD protection			2	kV	Mil-std 883B / 3015 cat1

Operating Range

Characteristic	Min.	Typ.	Max.	Units	Comments
Supply Voltage (Vcc)	3.3		3.6	V	
RFin Frequency Range	0.1		6	GHz	
Operating Junction Temperature	-40		+125	°C	
Junc'n to Amb't resistance Theta Ja		150		°C/W	4 layer FR4 Board
Junc'n to Case resistance Theta Jc		60		°C/W	4 layer FR4 Board

AC/DC Characteristics

Electrical Characteristics†

Characteristic	Pin	Min.	Typ.	Max.	Units	Conditions
Icc_in (Supply current)	1		0.35		mA	
Icc_out (Supply current)	8	36	61	96	mA	
Input frequency	2,3	1		6	GHz	RMS sinewave,
Input sensitivity	2,3		-20	-10	dBm	fin = 1 GHz to 6 GHz, Note 1
Input overload	2,3	4	10		dBm	fin = 1 GHz to 6 GHz, Note 1
Phase Noise	6,7		-150		dBC/Hz	@ 10 KHz Offset Fin = 3 GHz
Output voltage	6,7		1		Vp-p	Differential Into 50 ohm pull up resistors
Output power	6,7	-7	-2	2	dBm	fin = 1 GHz to 6 GHz, Pin = -10 dBm, Note 2
Output t-rise	6,7		110		ps	fin = 1 GHz to 6 GHz, Pin = -10 dBm
Output t-fall	6,7		110		ps	fin = 1 GHz to 6 GHz, Pin = -10 dBm
T – prop delay	2,6		250		ps	50% IN to 50% OUT
Jitter			0.1		ps	
Output Duty Cycle	6,7	45	50	55	%	fin = 1 GHz to 6 GHz, In = -10 dBm
Input. Edge Speed		500			V/us	For < 1 GHz input operation

† These characteristics are guaranteed by design and characterization over the following range of operating conditions unless otherwise stated: Tamb = -40C to +85C, Vcc = 3.3 V to 3.6 V

Note 1: Pin = power measured into 50 ohm Load from 50 ohm Source.

Note 2: Pout Single Ended AC coupled Single 50 ohm Termination.
For details of the test set-up, refer to the Application Note for RF Prescalers.

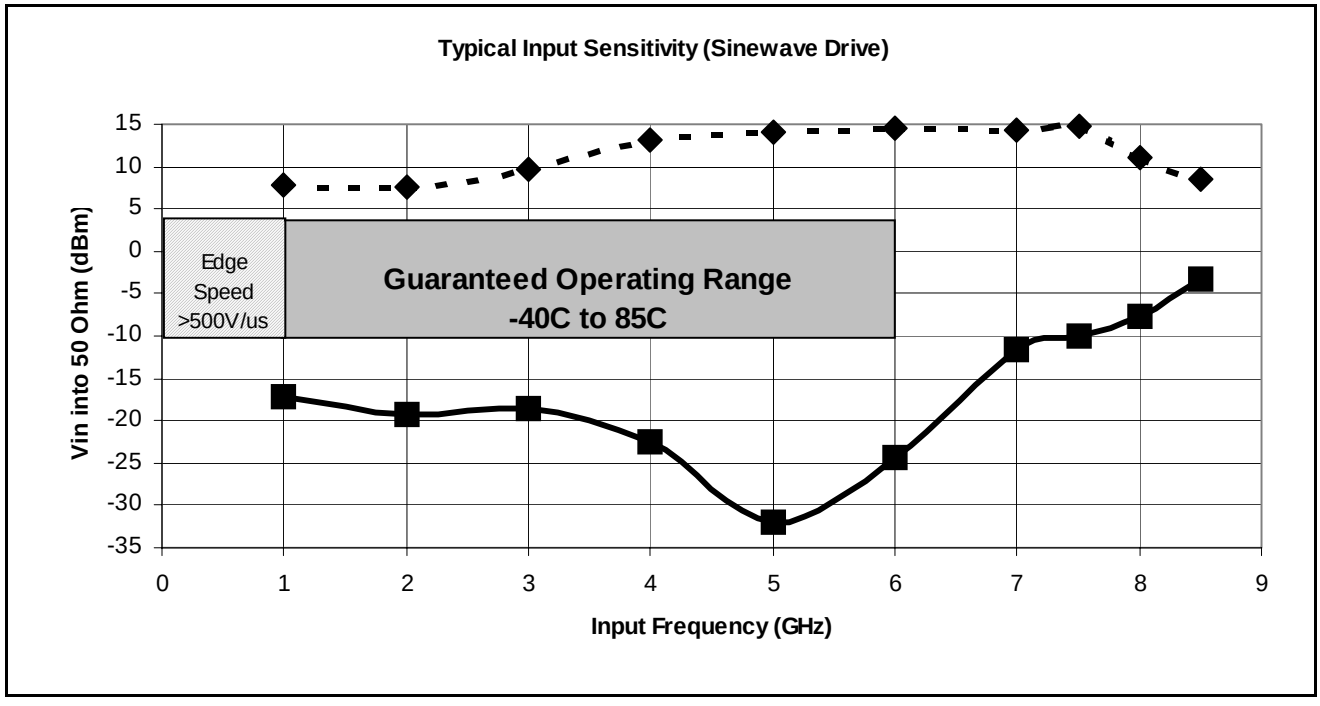


Figure 6 - Typical Input Sensitivity (sine wave drive)

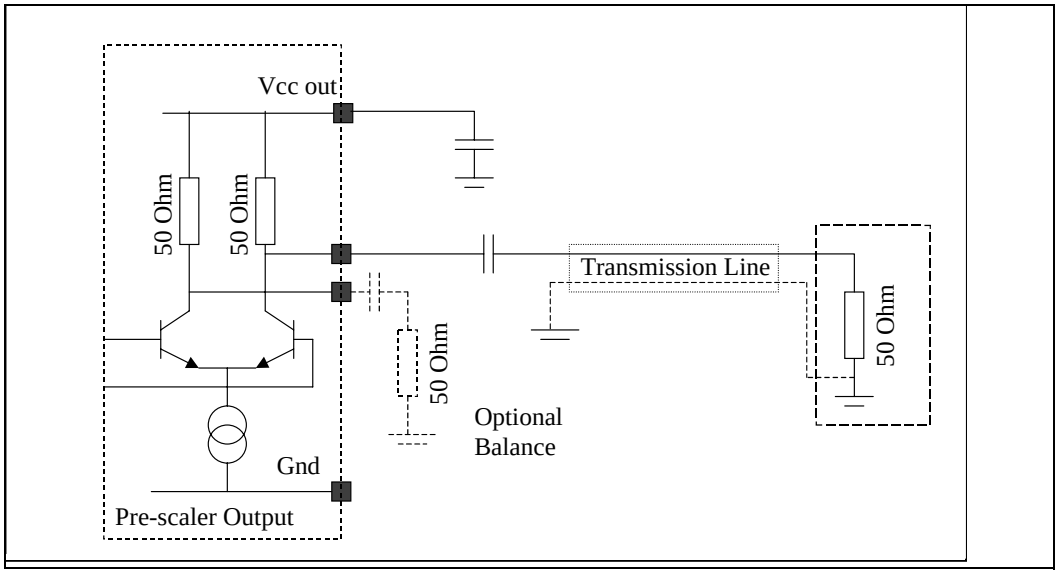


Figure 7 - Single Ended AC Coupled Single Termination

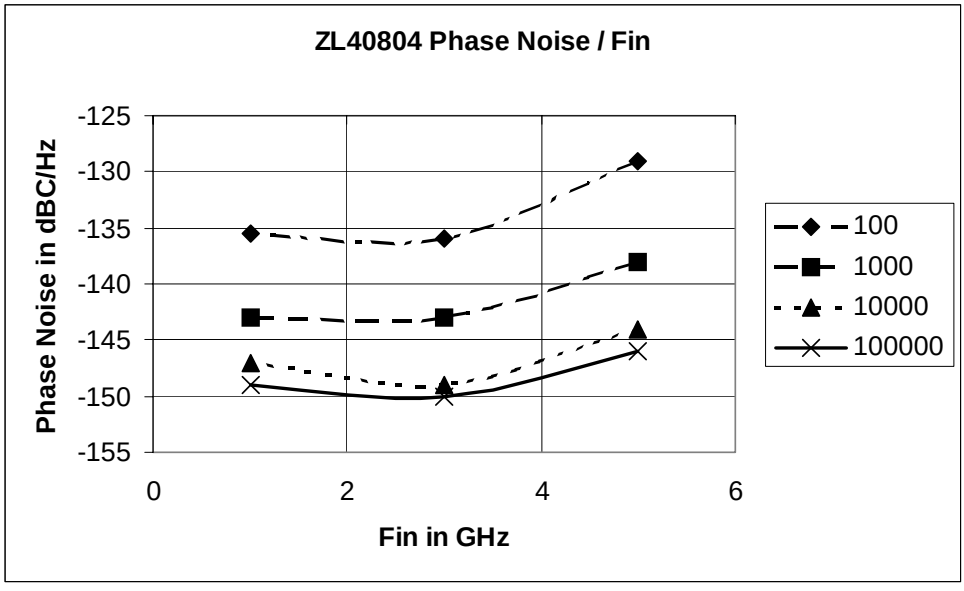


Figure 8 - ZL40804 Phase Noise vs Input Frequency

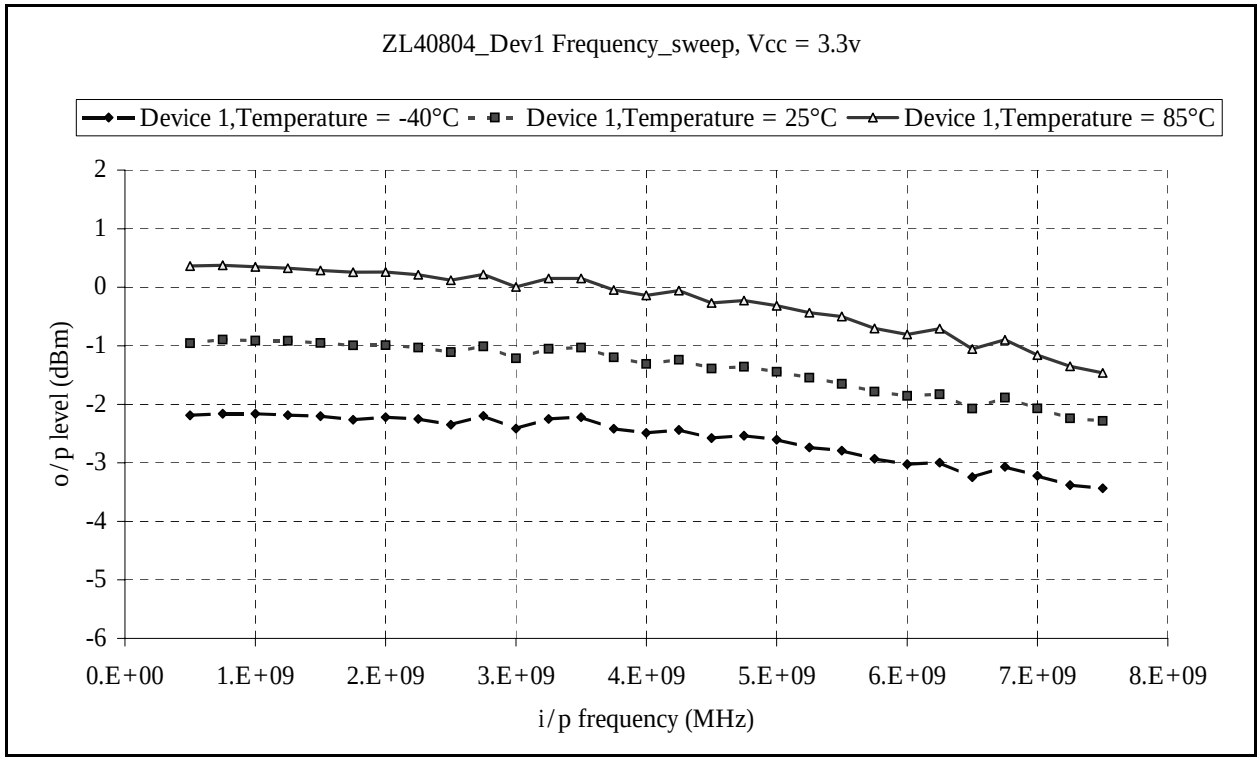


Figure 9 - ZL40804 Pout vs Input Frequency
(Vcc = 3.3 V, T=25C, T=85C)

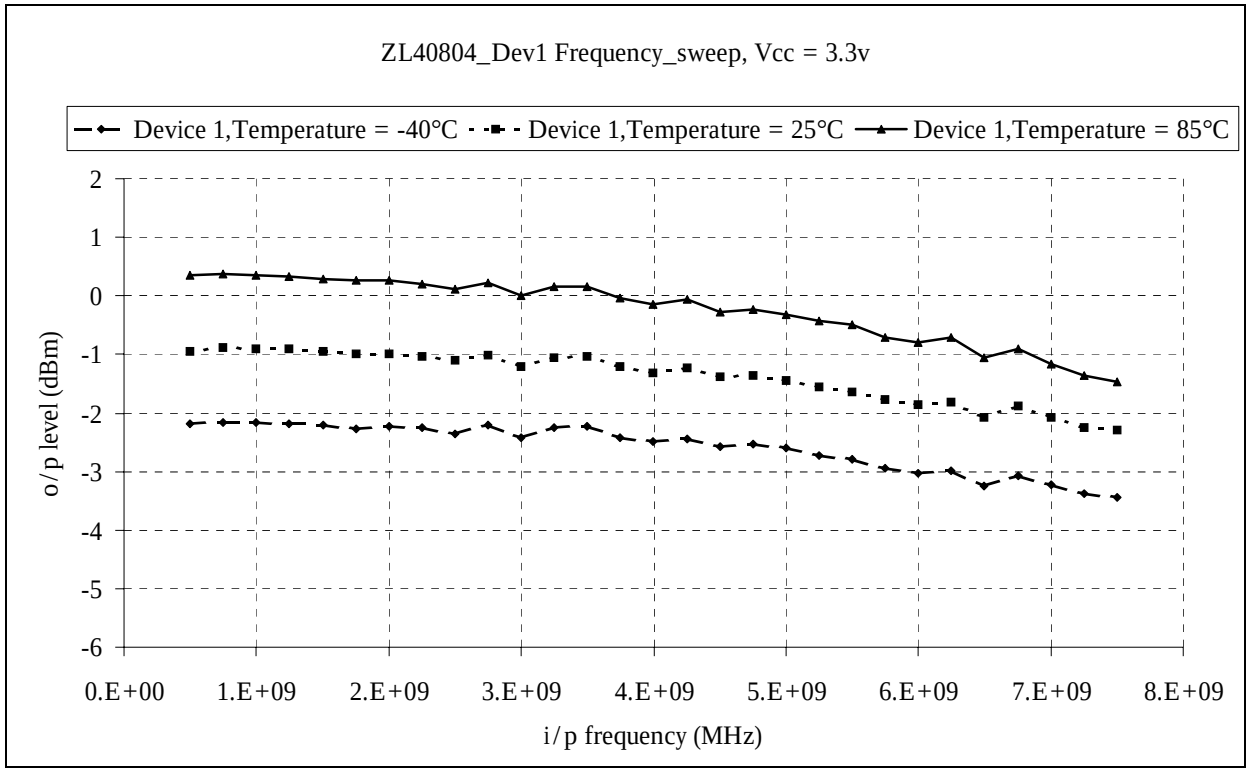


Figure 10 - ZL40804 Pout / Input Frequency (Vcc = 3.6 V, T=25C, T=85C)

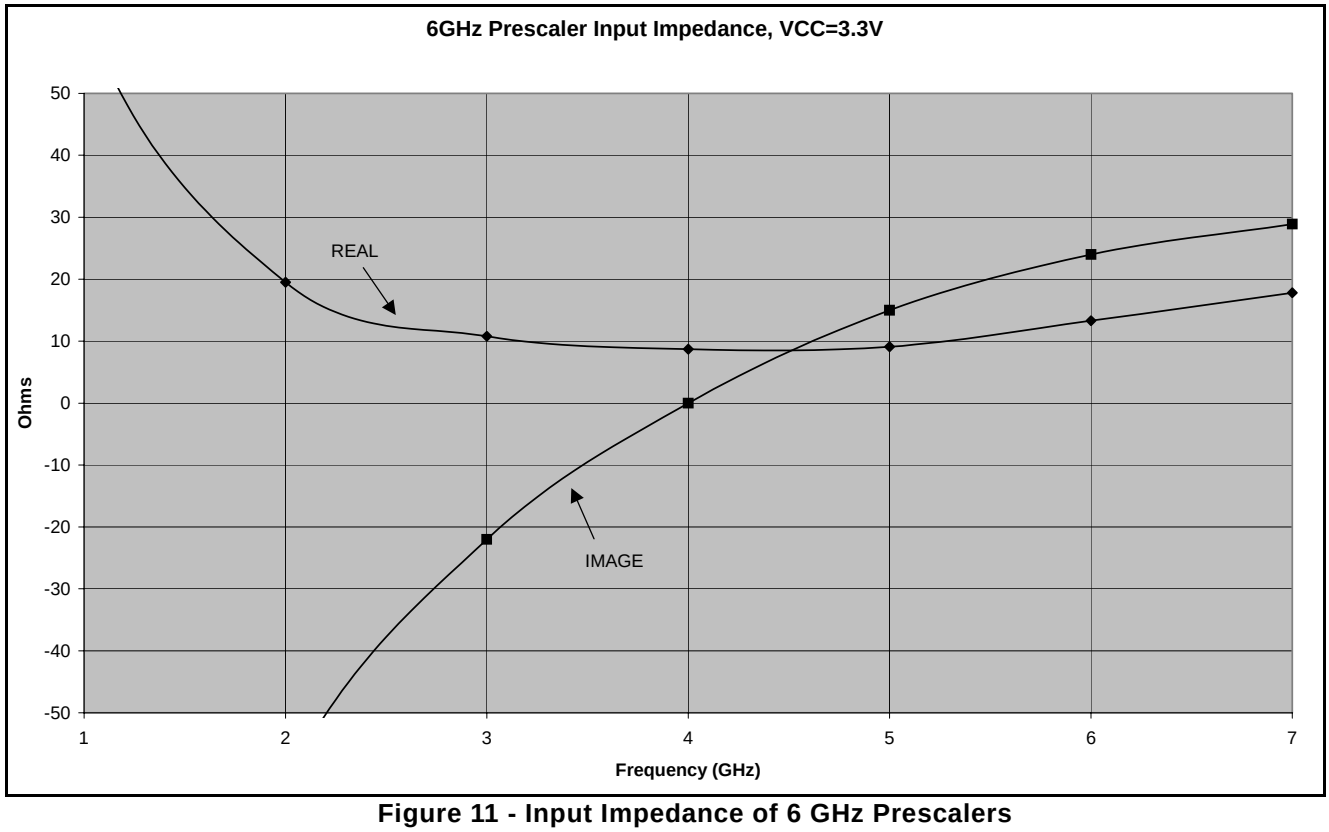


Figure 11 - Input Impedance of 6 GHz Prescalers

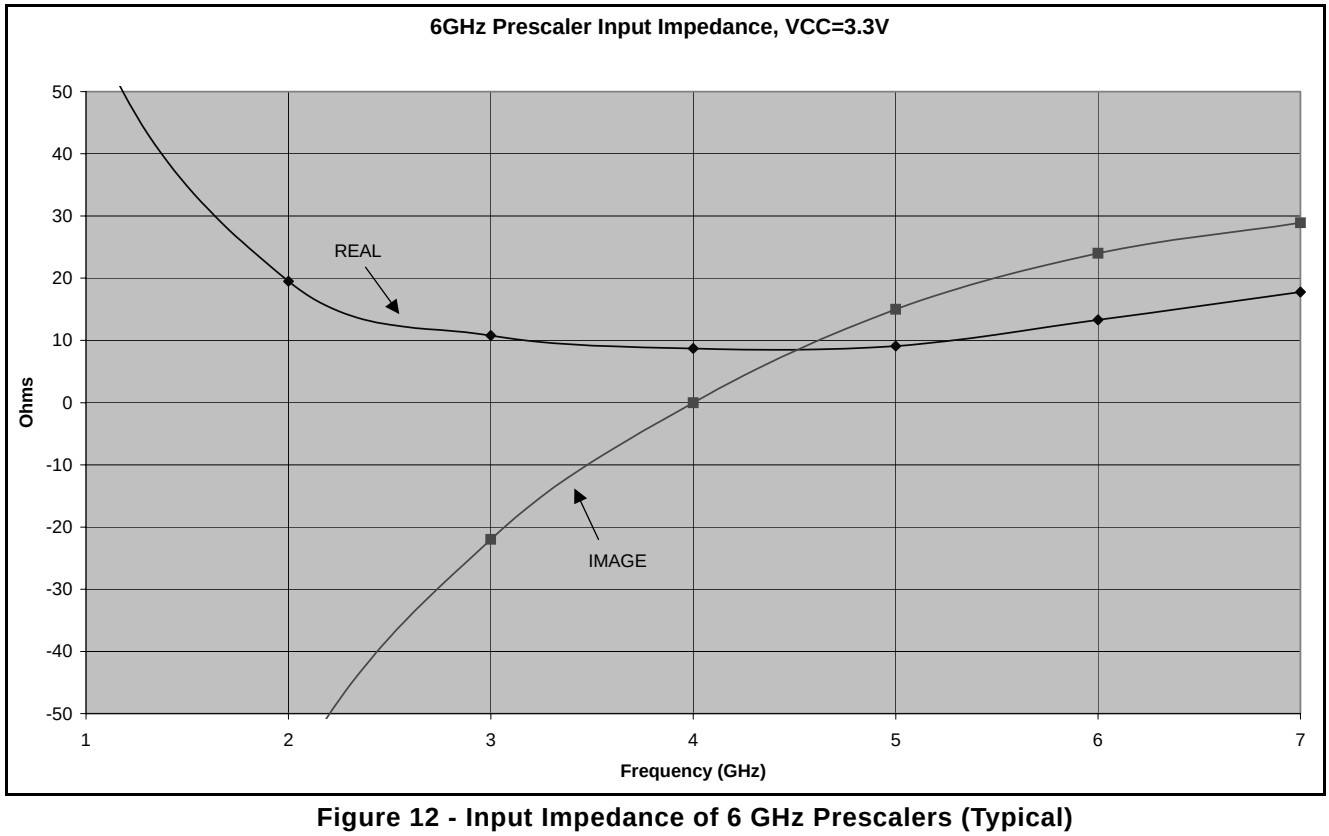


Figure 12 - Input Impedance of 6 GHz Prescalers (Typical)

Single Ended or Differential Load

Figures 11 and 12 illustrate the output waveform when measured differential and single ended with a 5 GHz waveform at the input at a level of +2 dBm. The single ended output contains some input frequency break through which contributes to the distortion present. This is a common mode signal which is rejected if the output is taken differentially.

Differential operation also provides an additional 6 dB output power.

Differential Operation reduces the radiated EMI in the system and reduces the susceptibility to common mode system noise.

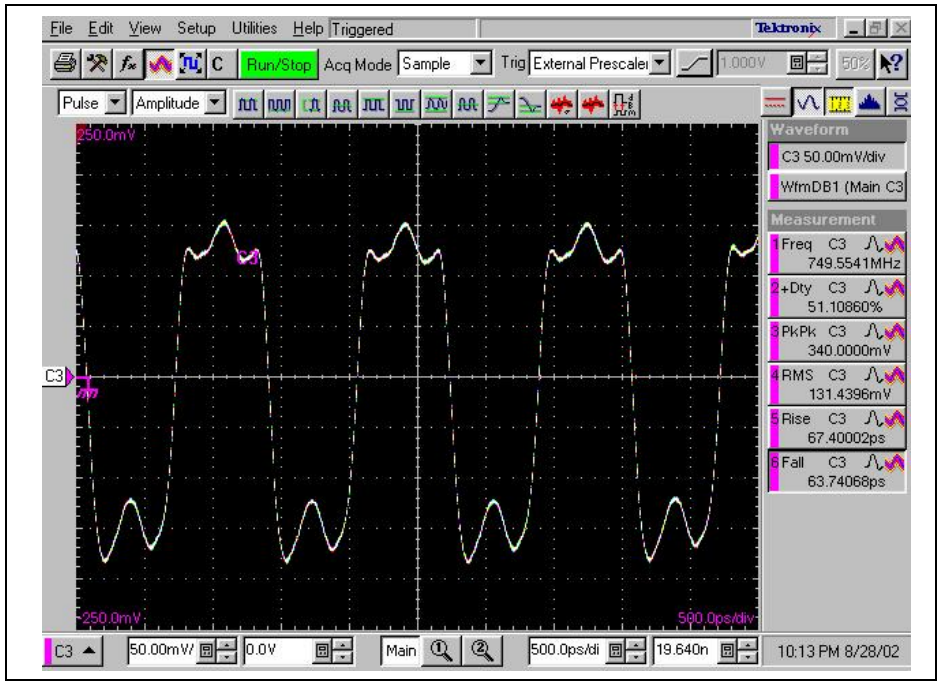


Figure 13 - ZL40804 Single Ended Out @ 3 GHz +2 dBm

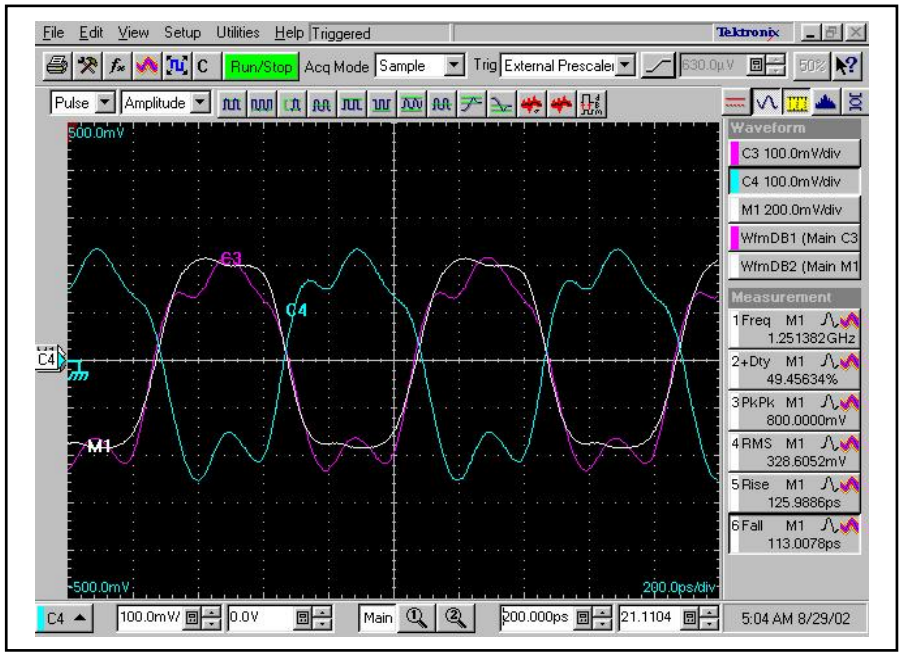
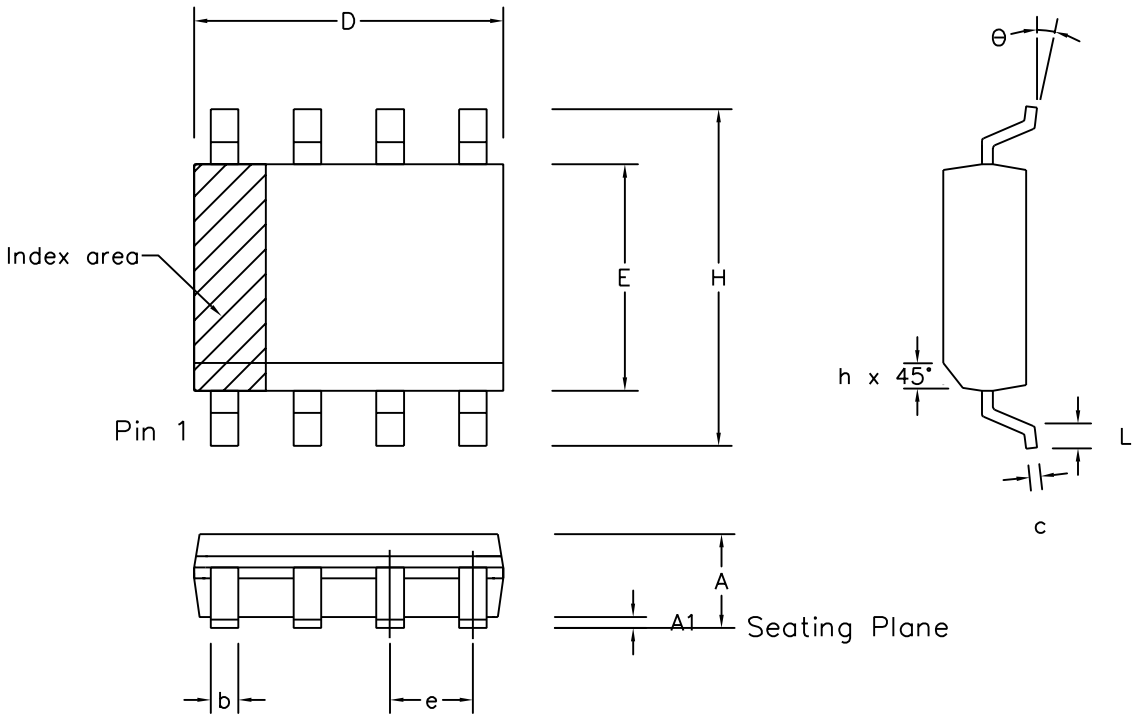


Figure 14 - ZL40804 Differential Out @ 5 GHz +2 dBm



	Min mm	Max mm	Min inch	Max inch
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	4.80	5.00	0.189	0.197
H	5.80	6.20	0.228	0.244
E	3.80	4.00	0.150	0.157
L	0.40	1.27	0.016	0.050
e	1.27 BSC		0.050 BSC	
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.008	0.010
θ	0°	8°	0°	8°
h	0.25	0.50	0.010	0.020
	Pin Features			
N	8		8	
Conforms to JEDEC MS-012AA Iss. C				

Notes:

1. The chamfer on the body is optional. If not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimensions are in inches.
3. Dimension D do not include mould flash, protusion or gate burrs. These shall not exceed 0.006" per side.
4. Dimension E1 do not include inter-lead flash or protusion. These shall not exceed 0.010" per side.
5. Dimension b does not include dambar protusion / intrusion. Allowable dambar protusion shall be 0.004" total in excess of b dimension.

ISSUE	1	2	3	4	5
ACN	6745	201936	202595	203705	212424
DATE	5Apr95	27Feb97	12Jun97	9Dec97	22Mar02
APPRD.					

ZARLINK SEMICONDUCTOR

Previous package codes

MP / S

Package Code DC

Package Outline for 8 lead SOIC (0.150" Body width)

GPD00010

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