MP3432

Fully Integrated, Synchronous, 30W Boost Converter with Pass-through Mode and Programmable Switching Current Limit

DESCRIPTION

The MP3432 is a 600kHz, fixed frequency, wide input range, highly integrated, boost converter. The MP3432 starts from an input voltage as low as 2.7V and supports up to 30W of load power from a 1-cell battery with integrated low $R_{DS(ON)}$ power MOSFETs.

The MP3432 adopts constant-off-time (COT) control topology, which provides fast transient response. MODE supports the selection of pulse-skip mode (PSM), forced continuous conduction mode (FCCM), and ultrasonic mode (USM) in a light-load condition. The programmable switching peak current limit provides accurate overload protection. And the high-side MOSFET eliminates the need for an external Schottky diode.

Full protection features include programmable input under-voltage lockout (UVLO) and over-temperature protection (OTP).

The MP3432 is available in a QFN-13 (3mmx4mm) package.

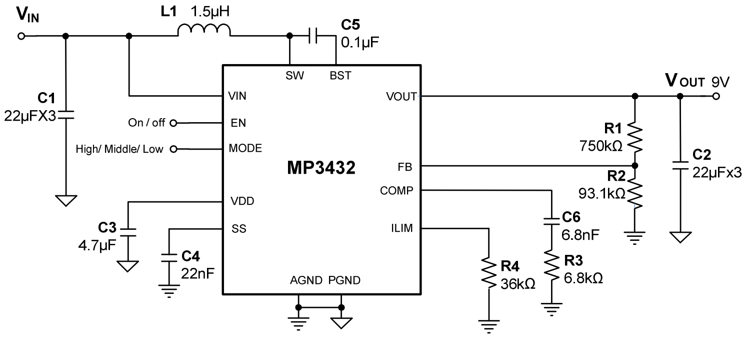
FEATURES

- 2.7V to 13V Start-Up Voltage
- 0.8V to 13V Operation Voltage
- Up to 16V Output Voltage
- Supports 30W Average Power Load and 40W Peak Power Load from 3.3V
- Programmable Switching Peak Current Limit
- Integrated 6.5mΩ and 10mΩ Power MOSFET
- >95% Efficiency for 3.6V V_{IN} to 9V/3A
- Selectable PSM, >23kHz USM, and FCCM in Light-Load Condition
- Auto Pass-Through Function in PSM Mode when V_{IN}>$V_{OUT-SET}$
- 600kHz Fixed Switching Frequency
- Adaptive COT for Fast Transient Response
- External Soft Start and Compensation Pins
- Programmable UVLO and Hysteresis
- 150°C Over-Temperature Protection (OTP)
- Available in a QFN-13 (3mmx4mm) Package

APPLICATIONS

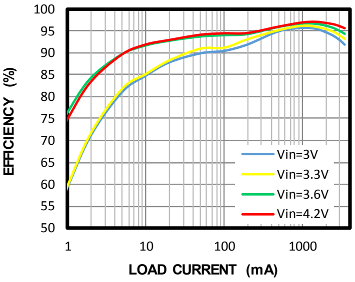
- Notebooks
- Bluetooth Speakers
- Portable POS Systems
- Quick Charger Power Banks

TYPICAL APPLICATION



Efficiency vs. Load Current

PSM



ORDERING INFORMATION

Part Number*	Package	Top Marking
MP3432GL	QFN-13(3mmx4mm)	*See Below*

*For Tape & Reel, add suffix –Z (e.g. MP3432GL–Z);

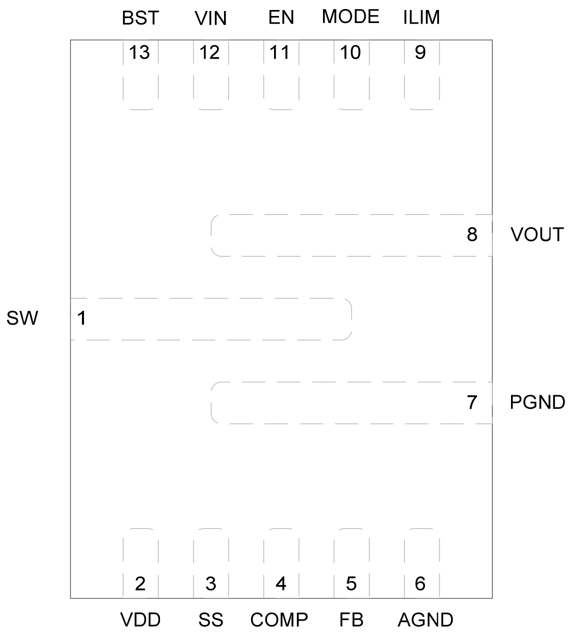
TOP MARKING

MPYW
3432
LLL

MP: MPS prefix
Y: Year code
W: Week code
3432: First four digits of the part number
LLL: Lot number

PACKAGE REFERENCE

TOP VIEW



QFN-13 (3mmx4mm)

ABSOLUTE MAXIMUM RATINGS (1)

SW	-0.3V (-3.5V for <10ns) to +18V (22V for <10ns)
VIN, EN, MODE, VOUT	-0.3V to +18V
BST	-0.3V to V_{SW} + 4.5V
All other pins	-0.3V to +4.5V
Continuous power dissipation (T_A = +25°C) (2)	4W (5)
Junction temperature	150°C
Lead temperature	260°C
Storage temperature	-65°C to +150°C

Recommended Operating Conditions (3)

Start-up input voltage (V_{ST})	2.7V to 13V
Operation input voltage (V_{IN})	0.8V to 13V
Startup input voltage with VDD bias (V_{ST2})	0.9V to 13V
Maximum external VDD bias voltage	3.6V (4)
Boost output voltage (V_{OUT})	V_{IN} to 16V
Operating junction temp. (T_J)	-40°C to +125°C

Thermal Resistance	θ_{JA}	θ_{JC}	
QFN-13 (3mmx4mm)			
EV3432-L-00A (5)	31	4	°C/W
JESD51-7 (6)	48	11	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) When the external VDD bias voltage is lower than the normal VDD regulated voltage, the external power need prevent the current from flowing out of VDD.
5) Measured on EV3432-L-00A, 4-layer 63mmx63mm PCB.
6) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = V_{EN} = 3.3V, T_J = -40°C to 125°C (7), typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Start-up input voltage	V_{ST}	No VDD bias	2.7		13	V
		VDD = 3V	0.9		13	V
Operating input voltage	V_{IN}		0.8		13	V
Operating VDD voltage (8)	V_{DD}	V_{IN} = 2.7V, 0 - 10mA	2.3	2.55		V
		V_{IN} = 12V, 0 - 15mA		3.4		V
VDD UVLO rising (8)	$VDD_{UVLO\text{-}R}$	VDD rising	2.2	2.4	2.6	V
VDD UVLO falling	$VDD_{UVLO\text{-}F}$	VDD falling	2	2.2	2.4	V
Shutdown current	I_{SD}	V_{EN} = 0V, measured on V_{IN}			2	µA
Quiescent current	I_Q	V_{FB} = 1.1V, V_{IN} = 3V, V_{OUT} = 9V, no switching, measured on V_{IN}			25	µA
		V_{FB} = 1.1V, V_{IN} = 3V, V_{OUT} = 9V, no switching, measured on V_{OUT}		510	600	µA
Pass-through mode quiescent current		V_{IN}=6.6V, FB=1.05V. PSM mode		600		µA
Enable (EN) Control						
EN turn-on threshold voltage	$V_{EN\text{-}ON}$	V_{EN} rising (switching)	1.15	1.23	1.31	V
EN high threshold voltage	$V_{EN\text{-}H}$	V_{EN} rising (micro power)			1.0	V
EN low threshold voltage	$V_{EN\text{-}L}$	V_{EN} falling (micro power)	0.4			V
EN turn-on hysteresis current	$I_{EN\text{-}HYS}$	1.0V < EN < $V_{EN\text{-}ON}$	3.5	5	6.5	µA
EN input current	I_{EN}	V_{EN} = 0V, 1.5V		0		µA
EN turn-on delay		EN on to switching		180		µs
Frequency						
Switching frequency	F_{SW}	V_{IN} = 3.3V, V_{OUT} = 9V	500	600	700	kHz
LS-FET minimum on time (9)	$T_{MIN\text{-}ON}$			80		ns
LS-FET maximum on time	$T_{MAX\text{-}ON}$			7.5		µs
Loop Control						
FB reference voltage	V_{REF}	T_J = 25°C	0.99	1	1.01	V
		T_J = -40°C to 125°C	0.985	1	1.015	V
FB input current	I_{FB}	V_{FB} = 1.1V			50	nA
Error amp voltage gain (10)	$A_{V\text{-}EA}$			300		V/V
Error amp tranconductance	G_{EA}			450		µA/V
Error amp max. output current		V_{FB} = 0.8V, V_{COMP} = 1V		63		µA
		V_{FB} = 1.2V, V_{COMP} = 1V		-60		µA
COMP to current gain	G_{CS}			22		A/V
COMP PSM threshold (9)	V_{PSM}	V_{MODE} = 0V		0.5		V
COMP high clamp		V_{FB} = 0.8V		2.8		V
Soft-start charge current	I_{SS}		6	7.5	9	µA
MODE Selection						
PSM MODE tri-state region	$V_{MODE\text{-}TRI}$		0.2		0.7	V
USM MODE tri-state region (11)			0.9		1.2	
FCCM MODE tri-state region			1.6		VDD	
Ultrasonic mode frequency	F_{USM}		23	33		kHz

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = V_{EN} = 3.3V, T_J = -40°C to 125°C (7), typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
HS-FET ZCD		PSM, V_{FB} = 1V, L = 1.5μH, V_{OUT} = 9V	-200	0	300	mA
HS-FET ZCD (9) (12)		V_{FB} = 1.1V, USM and FCCM			-2	A
Power Switch						
Low-side switch on resistance	R_{ON-L}			6.5		mΩ
High-side synchronous switch on resistance	R_{ON-H}			10		mΩ
Low-side switch leakage current		V_{SW} = 16V, T_J = 25°C			0.15	μA
High-side switch leakage current		V_{OUT} = 16V, V_{SW} = 0V, T_J = 25°C			0.15	μA
BST Power						
BST voltage				3.3		V
Current Limit						
Switching current limit	$I_{PK-LIMT}$	R_{ILIM} =36kΩ	9.3	10	10.7	A
Protection						
Output OVP threshold				16.5		V
Output OVP hysteresis				0.2		V
Thermal Protection						
Thermal shutdown (9)	T_{SD}			150		°C
Thermal shutdown hysteresis (9)	T_{SD-HYS}			25		°C

NOTES:

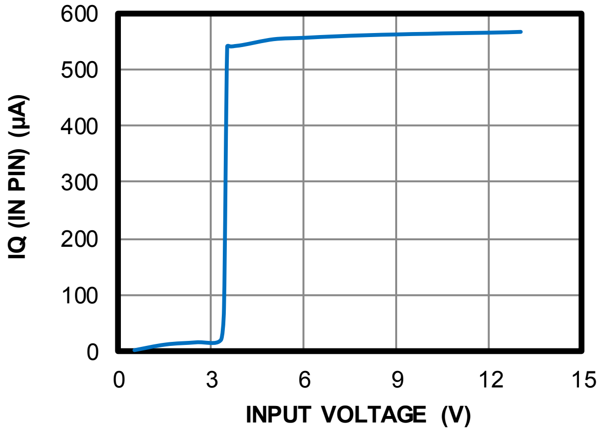
7) Guaranteed by over-temperature correlation, not tested in production.
8) VDD regulation voltage from 2.7V. V_{IN} is higher than the VDD UVLO rising threshold in each unit, which can guarantee that the IC starts up with 2.7V V_{IN}.
9) Guaranteed by sample characterization, not tested in production.
10) Guaranteed by design, not tested in production.
11) Add an external voltage within this range or float MODE for USM.
12) The HS-FET ZCD is lower than -2A in USM and FCCM.

TYPICAL CHARACTERISTICS

V_{IN} = V_{EN} = 3.3V, V_{OUT} = 9V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

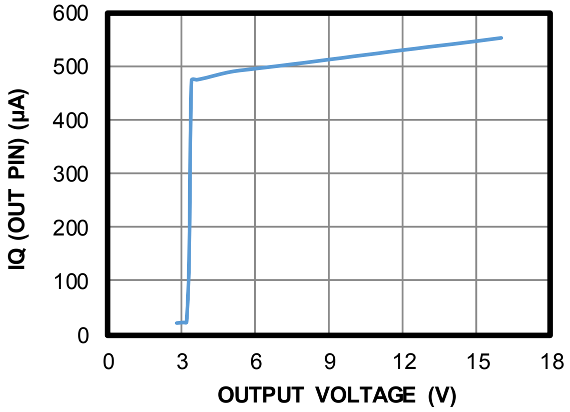
IQ (V_{IN} Pin) vs. Input Voltage

Boost Mode, V_{OUT}=15V[13]



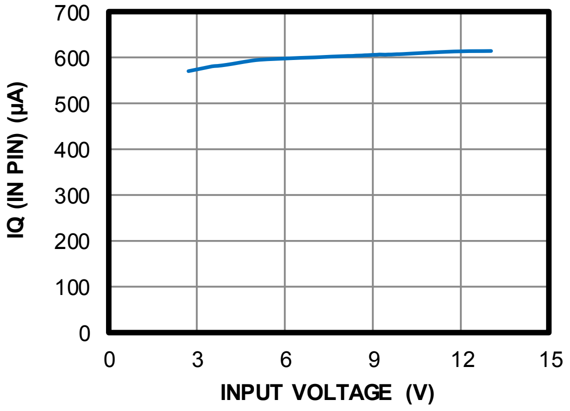
IQ (V_{OUT} Pin) vs. Output Voltage

Boost Mode[13]

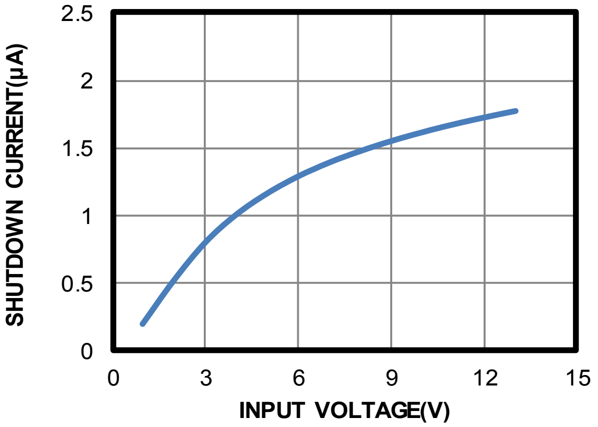


IQ vs. Input Voltage

Auto Pass-Through Mode

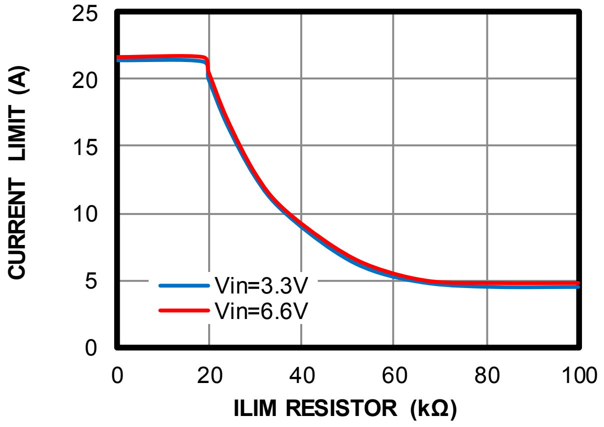


Shutdown Current vs. Input Voltage



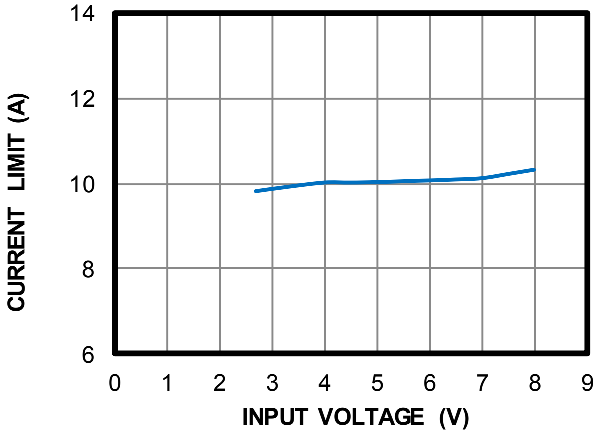
Switching Current Limit vs. ILIM Resistor

V_{OUT}=15V



Switching Current Limit vs. Input Voltage

R_{ILIM}=36k, V_{OUT}=15V



NOTE:

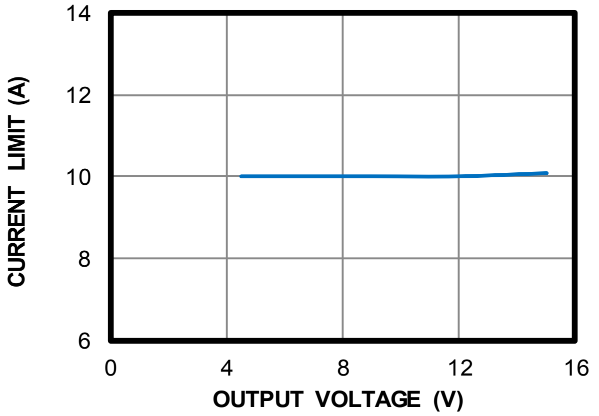
13) When VIN is higher than 3.4V, VIN supplies power to VDD, so the I_Q on VIN rises to higher when VIN > 3.4V. When VIN is 3V, the higher voltage source of either VIN or VOUT supplies VDD, so the I_Q on VOUT rises higher when VOUT > 3V and VIN = 3V.

TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = V_{EN} = 3.3V, V_{OUT} = 9V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

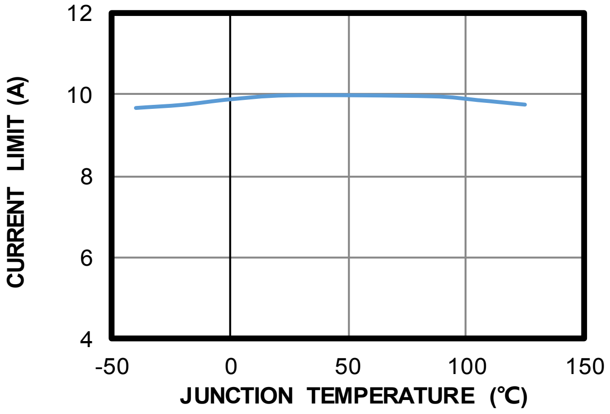
Switching Current Limit vs. Output Voltage

R_{ILIM}=36k

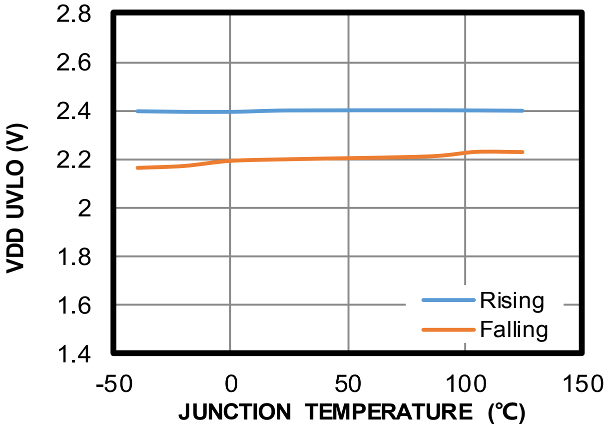


Switching Current Limit vs. Junction Temperature

R_{ILIM}=36k

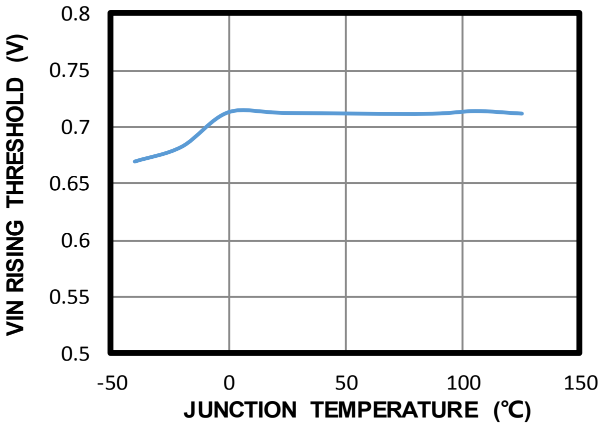


VDD UVLO vs. Junction Temperature



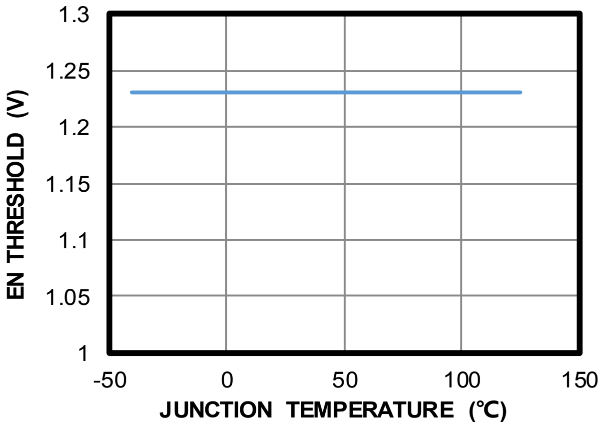
V_{IN} Rising Threshold vs. Junction Temperature

V_{DD_BIAS}=3.3V

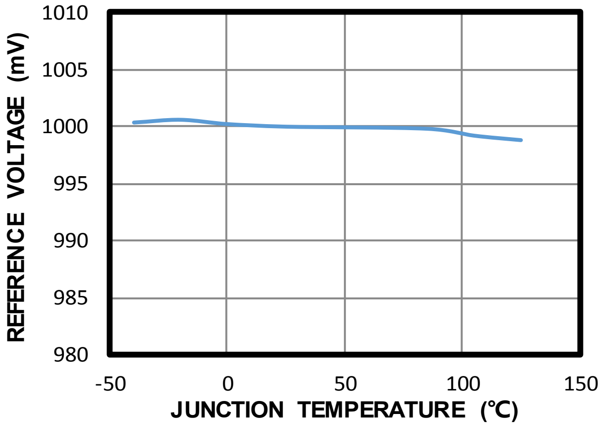


EN Threshold vs. Junction Temperature

IC Start-Up Switching



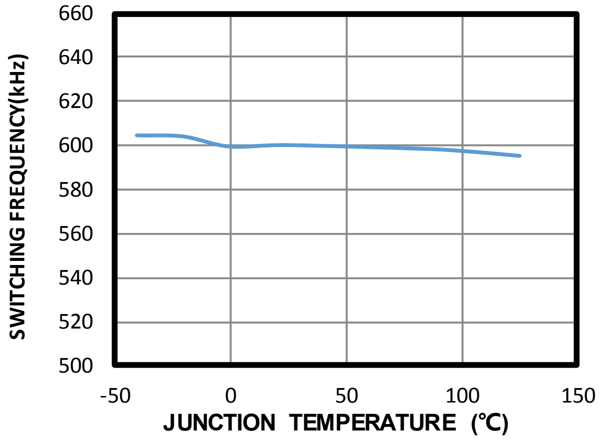
Reference Voltage vs. Junction Temperature



TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = V_{EN} = 3.3V, V_{OUT} = 9V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

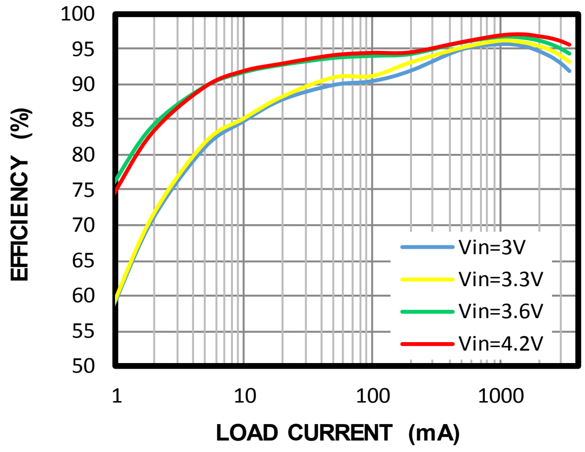
Switching Frequency vs. Junction Temperature



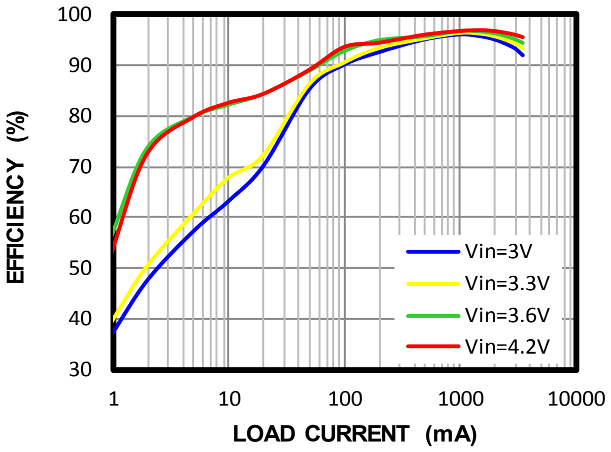
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.3V, V_{OUT} = 9V, L = 1.5µH, R_{ILIM}=27kΩ, I_{OUT} = 3.5A, USM, T_A = 25°C, unless otherwise noted.

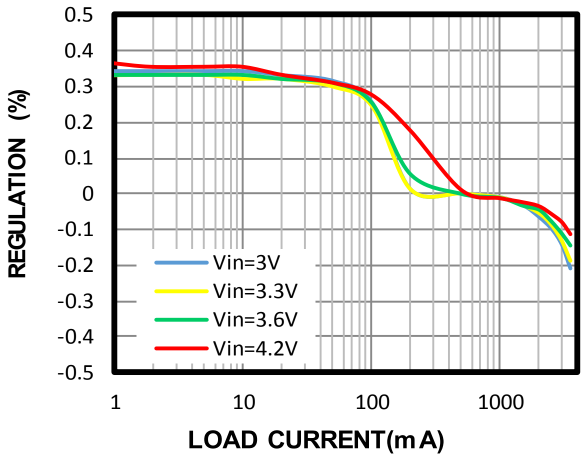
Efficiency vs. Load Current
PSM



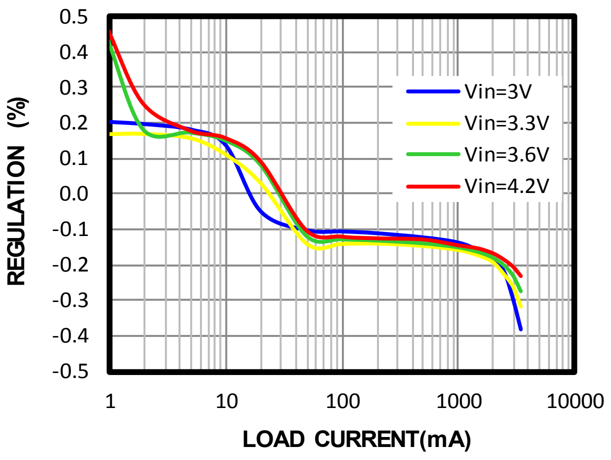
Efficiency vs. Load Current
USM



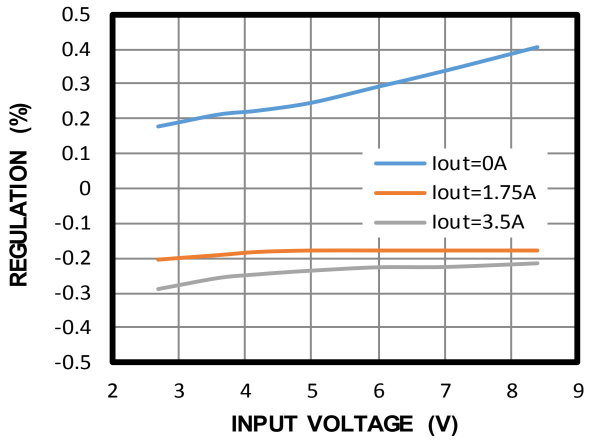
Load Regulation
PSM



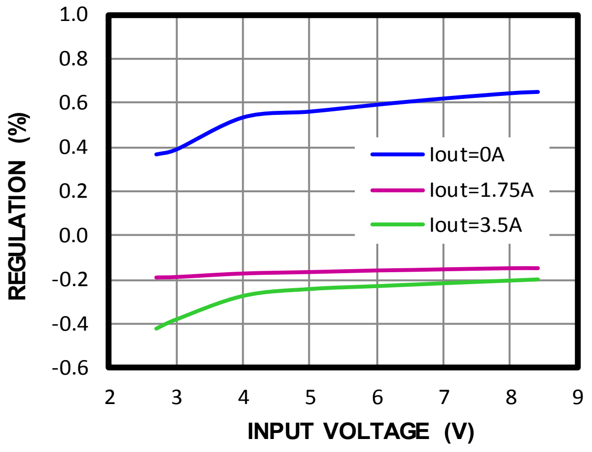
Load Regulation
USM



Line Regulation
PSM



Line Regulation
USM

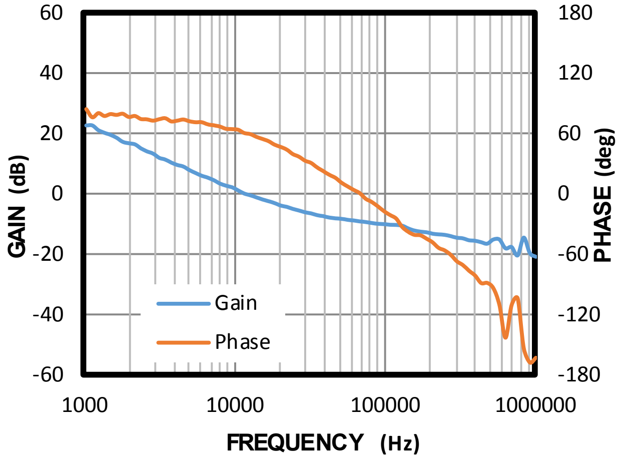


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

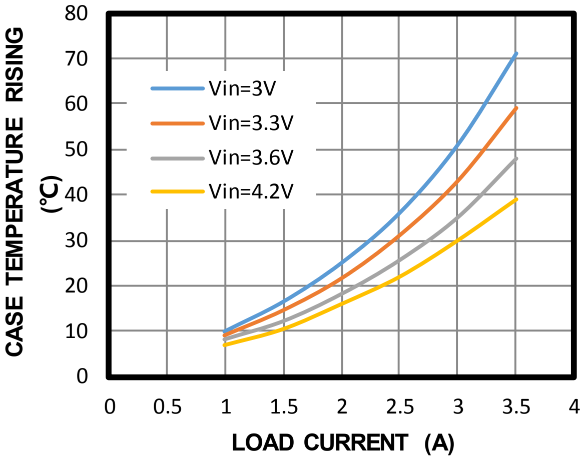
V_{IN} = 3.3V, V_{OUT} = 9V, L = 1.5µH, R_{ILIM}=27kΩ, I_{OUT} = 3.5A, USM, T_A = 25°C, unless otherwise noted.

Body Plot

I_{OUT}=3.5A



Case Temperature Rising

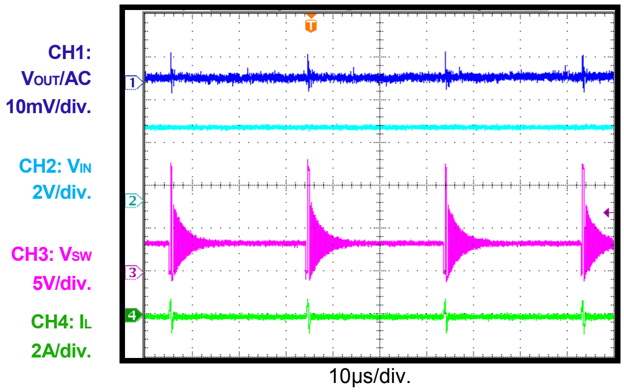


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 9V, L = 1.5µH, R_{ILIM}=27kΩ, I_{OUT} = 3.5A, USM, T_A = 25°C, unless otherwise noted.

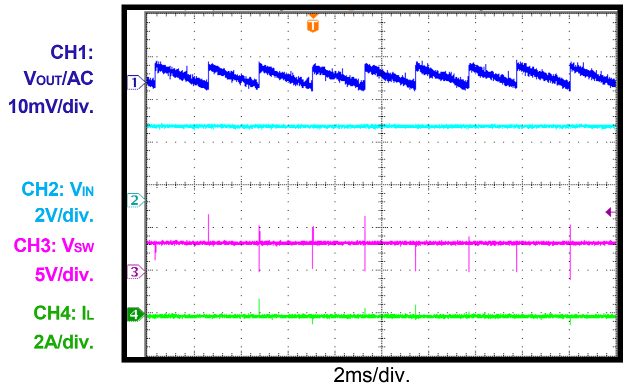
Steady State

I_{OUT}=0A, USM



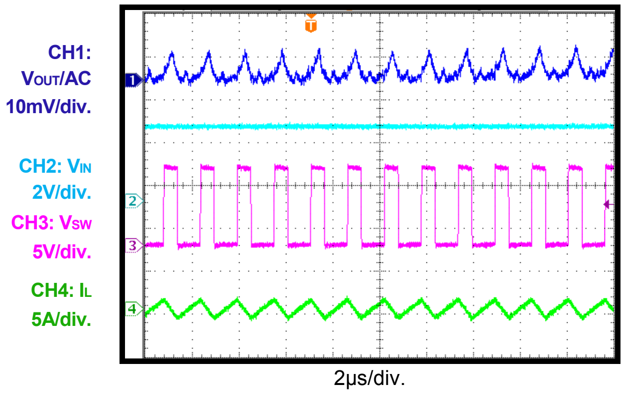
Steady State

I_{OUT}=0A, PSM



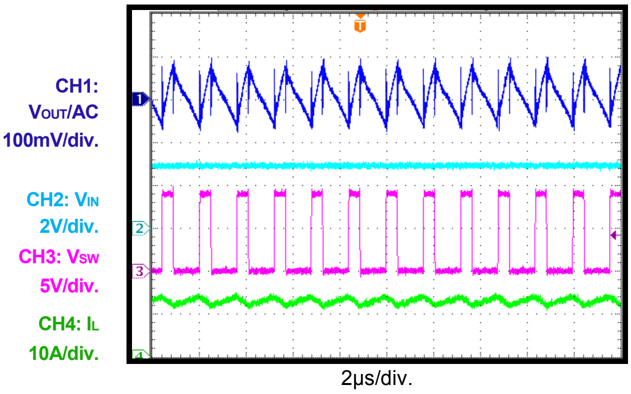
Steady State

I_{OUT}=0A, FCCM



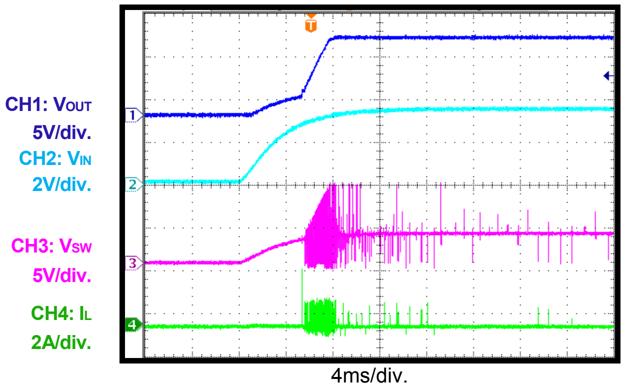
Steady State

I_{OUT}=3.5A



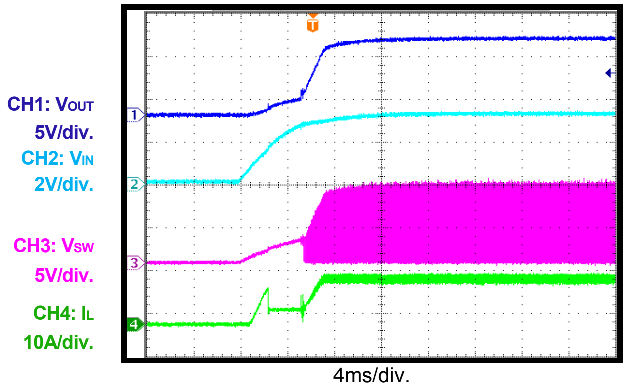
VIN Start-Up

I_{OUT}=0A



VIN Start-Up

I_{OUT}=3.5A

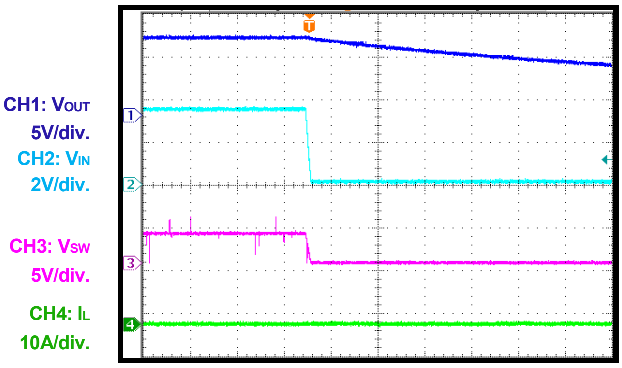


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 9V, L = 1.5µH, R_{ILIM}=27kΩ, I_{OUT} = 3.5A, USM, T_A = 25°C, unless otherwise noted.

V_{IN} Shutdown

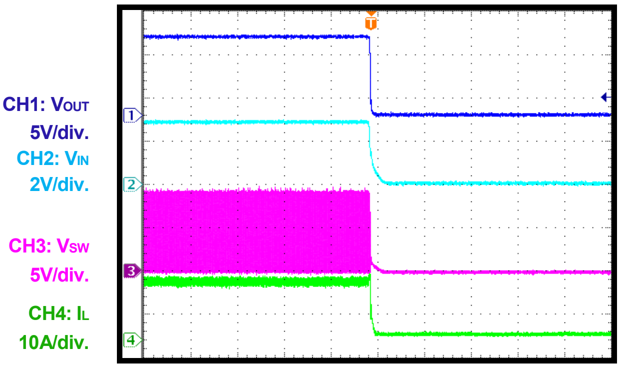
I_{OUT}=0A



1s/div.

V_{IN} Shutdown

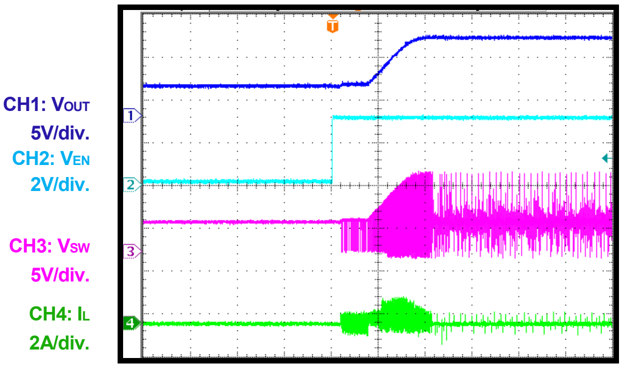
I_{OUT}=3.5A



10ms/div.

EN Start-Up

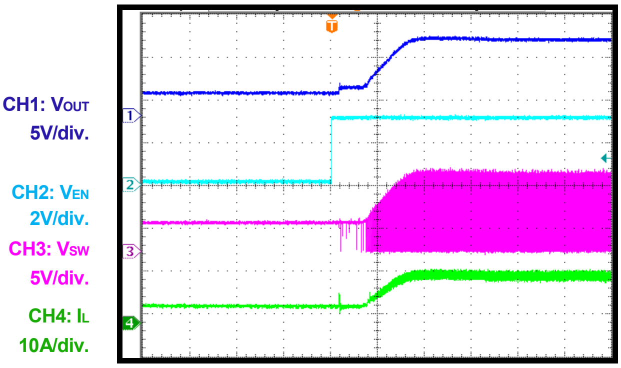
I_{OUT}=0A



2ms/div.

EN Start-Up

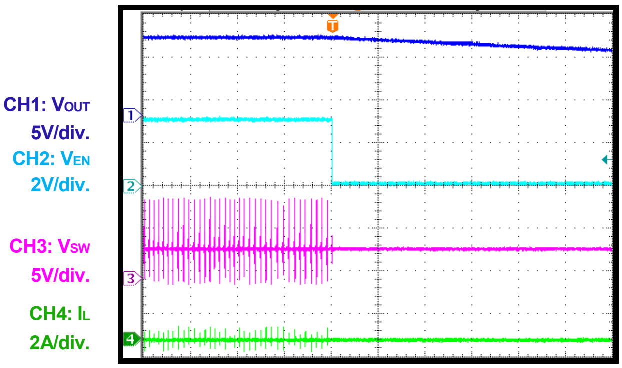
I_{OUT}=3.5A



2ms/div.

EN Shutdown

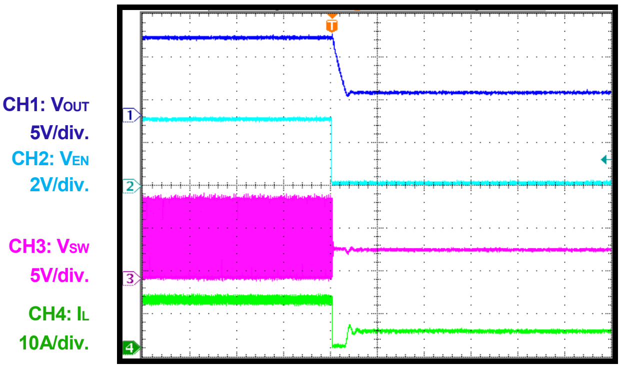
I_{OUT}=0A



400ms/div.

EN Shutdown

I_{OUT}=3.5A



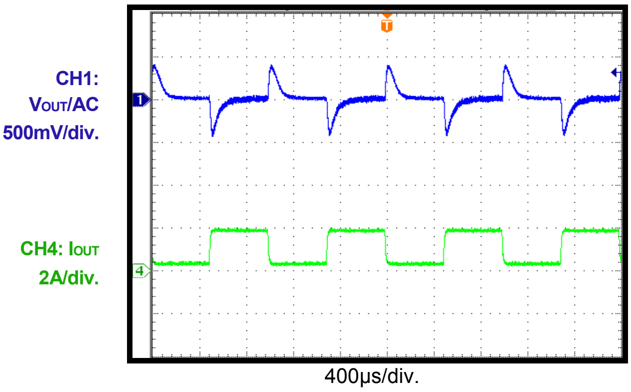
400µs/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 9V, L = 1.5µH, R_{ILIM}=27kΩ, I_{OUT} = 3.5A, USM, T_A = 25°C, unless otherwise noted.

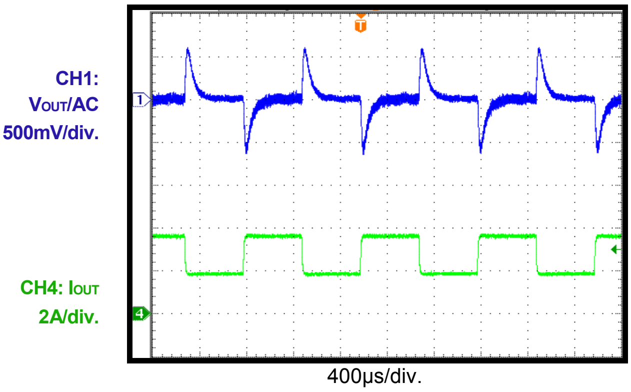
Load Transient

I_{OUT}=0-1.75A, I_{RAMP}=25mA/µs, USM



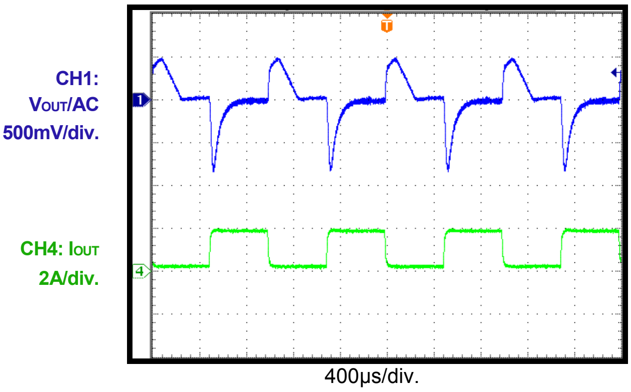
Load Transient

I_{OUT}=3.5-1.75A, I_{RAMP}=25mA/µs



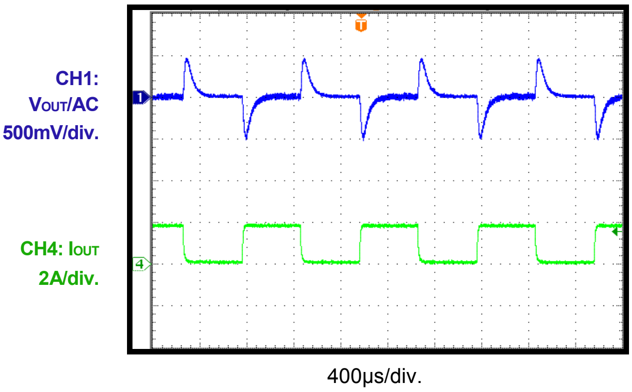
Load Transient

I_{OUT}=0-1.75A, I_{RAMP}=25mA/µs, PSM



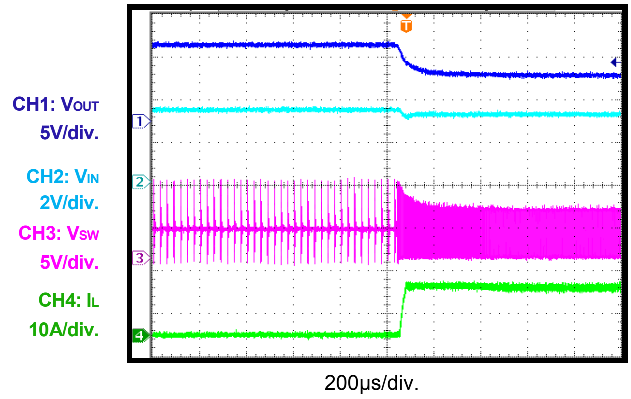
Load Transient

I_{OUT}=0-1.75A, I_{RAMP}=25mA/µs, FCCM



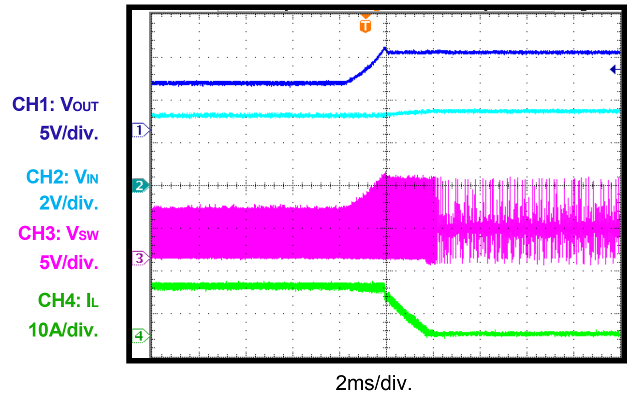
Over-Current Entry

Increase Output Current Slow, 0A->6A



Over-Current Recovery

Decrease Output Current Slow, 6A->0A



PIN FUNCTIONS

Pin #	Name	Description
1	SW	**Converter switch.** SW is connected to the drain of the internal low-side power MOSFET and the source of the internal high-side synchronous power MOSFET. Connect the power inductor to SW.
2	VDD	**Internal bias supply.** Decouple VDD with a 4.7µF ceramic capacitor placed as close to VDD as possible. When V_{IN} is higher than 3.4V, VDD is powered by V_{IN}. Otherwise, VDD is powered by the higher voltage of either V_{IN} or V_{OUT}. If the external bias voltage connected to VDD is higher than 3.4V, the regulator from V_{IN} and V_{OUT} is disabled. The VDD regulator starts working when V_{IN} is higher than about 0.9V, if EN is high. Supply V_{IN} with a power source higher than 2.7V during V_{IN} start-up to provide enough VDD power voltage.
3	SS	**Soft-start programming.** Place a capacitor from SS to AGND to set the V_{OUT} rising slew rate.
4	COMP	**Internal error amplifier output.** Connect a capacitor and resistor in series from COMP to AGND for loop compensation.
5	FB	**Feedback input.** Connect a resistor divider from V_{OUT} to FB.
6	AGND	**Analog ground.**
7	PGND	**Power ground.**
8	VOUT	**Output.** V_{OUT} is connected to the drain of the high-side MOSFET. V_{OUT} powers VDD when V_{OUT} is higher than V_{IN}, and V_{IN} is lower than 3.4V.
9	ILIM	**Switching peak current limit setting.** Place a resistor from ILIM to AGND to set the switching peak current limit.
10	MODE	**MODE selection.** If MODE is floating, the MP3432 works in ultrasonic mode (USM). If MODE is high, the MP3432 works in forced continuous conduction mode (FCCM). If MODE is low, the MP3432 works in pulse-skip mode (PSM). MODE must always be higher than 0.2V in the application, even if in PSM. Place a 130kΩ + 20kΩ resistor divider from VDD to MODE to set the MP3432 in PSM.
11	EN	**Chip enable control.** When not in use, connect EN to V_{IN} for automatic start-up. EN can program the V_{IN} UVLO. Do not leave EN floating.
12	VIN	**Input supply.** V_{IN} must be bypassed locally. Supply V_{IN} with a power source higher than 2.7V during V_{IN} start-up to provide enough VDD power voltage.
13	BST	**Bootstrap.** A capacitor between BST and SW powers the synchronous HS-FET.

BLOCK DIAGRAM

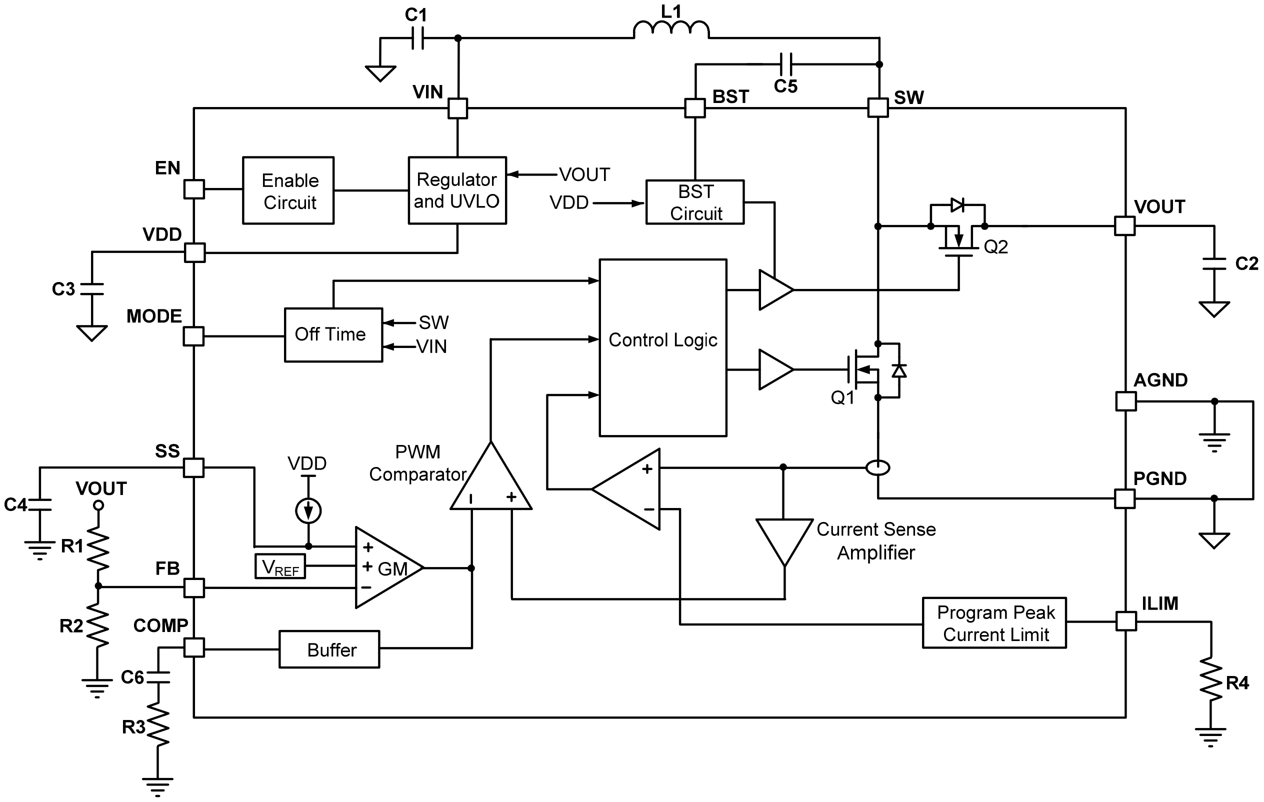


Figure 1: Functional Block Diagram

OPERATION

The MP3432 is a 600 kHz, fixed frequency, high-efficiency, wide input range, boost converter. Its fully integrated low $R_{DS(ON)}$ MOSFETs provide small size and high efficiency for high-power step-up applications. Constant-off-time (COT) control provides fast transient response, while MODE selection provides flexible light-load performance design.

Boost Operation

The MP3432 uses COT control to regulate the output voltage. At the beginning of each cycle, the low-side N-channel MOSFET (LS-FET) Q1 is turned on, forcing the inductor current to rise. The current through the LS-FET is sensed. If the current signal rises above the COMP voltage (V_{COMP}), which is an amplifier output comparing the feedback voltage (V_{FB}) against the internal reference voltage, the pulse-width modulation (PWM) comparator flips and turns the LS-FET off. Then the inductor current flows to the output capacitor through the high-side switch MOSFET (HS-FET), causing the inductor current to decrease. After a fixed off time, the LS-FET turns on again and the cycle repeats. In each cycle, the LS-FET off-time is determined by the V_{IN}/V_{OUT} ratio, and the on time is controlled by V_{COMP}, so the inductor peak current is controlled by COMP, which itself is controlled by the output voltage. Therefore, the inductor current regulates the output voltage.

Operation Mode

The MP3432 works with a 600kHz quasi-constant frequency with PWM control in heavy-load condition. When the load current decreases, the MP3432 can work in forced continuous conduction mode (FCCM), pulse-skip mode (PSM), or ultrasonic mode (USM) based on the MODE setting.

Forced Continuous Conduction Mode (FCCM)

The MP3432 works in a fixed-frequency PWM mode for any load condition if MODE is high (>1.6V). In this condition, the off time is determined by the internal circuit to achieve the 600kHz frequency based on the V_{IN}/V_{OUT} ratio. When the load decreases, the average input current drops, and the inductor current from V_{OUT} to V_{IN} may become negative during the off-time (LS-FET is off, and HS-FET is on). This forces the inductor current to work in continuous conduction mode (FCCM) with a fixed frequency, producing a lower V_{OUT} ripple than in PSM.

Pulse-Skip Mode (PSM)

The MP3432 works in PSM in light-load condition if the MODE voltage is low ($0.2V < V_{MODE} < 0.7V$). In this condition, once the inductor current drops to 0A, the HS-FET turns off to stop current flowing from V_{OUT} to V_{IN}, forcing the inductor current to work in discontinuous conduction mode (DCM). At the same time, the internal off time becomes longer once the MP3432 enters DCM. The off time is inversely proportional to the HS-FET on period in each cycle. In deep DCM conditions, the MP3432 slows down the switching frequency and saves power loss.

If V_{COMP} drops to the 0.5V PSM threshold, the MP3432 stops switching to decrease the switching power loss further. Switching resumes once V_{COMP} rises above 0.5V. The switching pulse skips based on V_{COMP} in very light-load conditions. PSM has much higher efficiency than FCCM in light load, but the V_{OUT} ripple may be higher, and the frequency may go down and produce audible noise.

In DCM, frequency is low, and the LS-FET will not turn on in the prolonged off time. If the load increases and COMP runs higher, the off time shortens and the MP3432 returns to the 600kHz fixed-frequency regularly, so the loop can respond to the high load current.

Auto Pass-Through Function in PSM Mode

In PSM mode, if V_{IN} is increased close to $V_{OUT-SET}$, V_{OUT} will be charged higher than $V_{OUT-SET}$ due to the LS-FET minimum on time. In this mode, V_{COMP} drops to the PSM threshold, and the MP3432 works with group switching pulses. If V_{IN} continues rising and V_{COMP} remains low for a long time in this condition, the MP3432 runs into auto pass-through mode, in which the HS-FET is always on and the LS-FET is always off. Pass-through mode avoids the HS-FET body-diode conduction current when V_{IN} is higher than $V_{OUT-SET}$. In pass-through mode, if V_{OUT} drops and

V_{COMP} rises higher than the PSM threshold, the MP3432 exits auto pass-through mode and recovers to normal switching mode.

If V_{IN} is close to $V_{OUT-SET}$, the MP3432 may switch between boost mode and auto pass-through mode; this will cause a high V_{OUT} ripple, so it is recommended to avoid use in this condition. If pass-through mode is needed, set the feedback resistor to make $V_{OUT-SET}$ much lower than V_{IN}.

Ultrasonic Mode (USM)

To prevent audible noise with a switching frequency lower than 20kHz in PSM, the MP3432 implements USM by floating MODE or setting MODE in the USM range ($0.9V < V_{MODE} < 1.2V$). In USM, the inductor current works in DCM, and the frequency stretches as if in PSM when the load decreases to a moderate level. However, the switching does not stop when COMP drops to the 0.5V PSM threshold. The LS-FET on time is controlled by COMP, even if V_{COMP} is lower than the PSM threshold, unless it triggers the minimum on time.

The MP3432 continues decreasing the switching frequency if the load is still decreasing. Once the MP3432 detects that the LS-FET is off for 30μs, it forces the LS-FET on. This limits the frequency, avoiding audible frequency in a light-load or no-load condition.

USM may convert more energy to the output than the required load due to the minimum 23kHz frequency, which causes V_{OUT} to rise above the normal voltage setting. When V_{OUT} rises and V_{COMP} drops, the inductor peak current may drop as well. If V_{COMP} drops below one internal clamped level, the HS-FET zero-current detection (ZCD) threshold is regulated to one negative level gradually, so the energy in the inductor can flow back to V_{IN} in each cycle. This keeps the output at the setting voltage with a >23kHz frequency. The MP3432 also works with a 600kHz frequency if V_{COMP} rises again.

USM has the same efficiency as in PSM if the frequency is higher than the typical 33kHz. USM has more power loss than PSM if the frequency is clamped at the typical 33kHz, but USM does not introduce audible noise caused by the group pulse in PSM.

Minimum On Time and Minimum Off Time

The MP3432 blanks the LS-FET on-state with 80ns in each cycle to enhance noise immunity. This 80ns minimum on time restricts applications with a high V_{IN}/V_{OUT} ratio. The MP3432 also blanks the LS-FET off state with a minimum off time in each cycle. During the minimum off time, the LS-FET cannot turn on, and the minimum off time is short enough to convert the 0.8V input to a 16V output.

LS-FET and HS-FET Maximum On Time

If the inductor current cannot trigger V_{COMP} with an on time of 7.5μs, the MP3432 shuts down the LS-FET. After the LS-FET is shut down, the inductor current goes through the HS-FET and charges V_{OUT} in the off time period. This helps refresh V_{OUT} with a minimum frequency of about 133 kHz in heavy-load transient conditions.

In a USM condition, the HS-FET on time is limited below 8μs. This helps limit the maximum LS-FET off time when V_{OUT} is close to V_{IN}. In USM, if V_{IN} is too close to V_{OUT}, the HS-FET may be turned off by the 8μs HS-FET maximum on time, because the inductor current cannot ramp down within this 8μs limit. After the HS-FET turns off, the LS-FET turns on immediately with one pulse control by V_{COMP}, and then the HS-FET turns on again. This makes the LS-FET work in a quasi-constant minimum duty cycle. If V_{IN} is high enough, V_{OUT} is higher than the setting voltage with this duty cycle ratio. In PSM, the IC works with normal PSM logic. The IC stops working when V_{OUT} is higher than the setting voltage and resumes switching when V_{OUT} drops below the setting voltage.

VDD Power

The MP3432 internal circuit is powered by VDD. A ceramic capacitor no less than 4.7μF is required on VDD. When V_{IN} is lower than 3.4V, VDD is powered from the higher value of either V_{IN} or V_{OUT}. This allows the MP3432 to maintain a low $R_{DS(ON)}$ and high efficiency, even with a low input voltage. When V_{IN} is higher than 3.4V, VDD is always powered by V_{IN}. This decreases the V_{OUT} to VDD regulator loss because V_{OUT} is always higher than V_{IN}.

If VDD is powered by an external supply and the voltage is higher than 3.4V, the regulators from V_{IN} and V_{OUT} are disabled. In this condition, the MP3432 starts once the external VDD power supply is higher than VDD UVLO, even if V_{IN} is as low as 0.9V. When VDD is powered by the external power supply, the MP3432 continues working, even if both V_{IN} and V_{OUT} are dropping but are higher than 0.8V. The external VDD power source should be limited within 3.6V.

There is a reverse-blocking circuit to limit the current flowing between V_{IN} and V_{OUT}. If the external VDD power is higher than the VDD regulation voltage, the current is supplied from the external power, and there is no path for the current from VDD to V_{IN} or from VDD to V_{OUT}.

VDD is charged when V_{IN} is higher than about 0.9V, and EN is higher than the micro-power threshold. If EN is low, VDD is disconnected from V_{IN} and V_{OUT}. Supply V_{IN} with a power source higher than 2.7V during V_{IN} start-up to provide enough VDD power voltage.

Start-Up

When the MP3432 input is powered, it starts charging VDD from V_{IN}. Once VDD rises above its UVLO threshold and EN is high, the MP3432 starts switching with closed loop control. If VDD is powered by an additional supply, the MP3432 starts switching once VDD rises to above its under-voltage lockout (UVLO) threshold.

After the IC is enabled, the MP3432 starts up with a soft-start (SS) control. The SS signal is controlled by charging SS from 0V and compared with the internal reference voltage. The lower value is fed to the error amplifier to control the output voltage. After the SS signal rises above the reference voltage, soft start is completed, and the internal reference takes charge of the feedback loop regulation.

If there is some bias voltage on V_{OUT} during PSM, the MP3432 stops switching until the SS signal rises above V_{FB}, which is proportional to the V_{OUT} bias voltage. If the IC is in USM or FCCM, the MP3432 works with a frequency of about 33kHz or 600kHz. Both USM and FCCM have a negative inductor current, so the energy may transfer from V_{OUT} to V_{IN} if the V_{OUT} bias is high.

Synchronous Rectifier and BST Function

The MP3432 integrates both a LS-FET Q1 and HS-FET Q2 to reduce external components. During switching, the rectifier switch Q2 is powered from BST (typically 3.4V higher than the SW voltage). This 3.4V bootstrap voltage is charged from VDD when the LS-FET turns on.

Switching Peak Current Limit

The MP3432 provides a programmable switching peak current limit function. The switching peak current limit is set by a resister on the ILIM pin, which can be calculated with equation (1):

$$I_{LIM} = \frac{320}{R_{ILIM} - 4} \qquad (1)$$

Where R_{ILIM} is the resister on ILIM and is in KΩ.

When R_{ILIM} is small enough, or ILIM is shorted to GND, the switching current has a maximum value. When R_{ILIM} is big enough, or ILIM is floated, the switching current has a minimum value (see the Typical Characteristics curve).

In each cycle, the internal current sensing circuit monitors the LS-FET current signal. Once the sensed current reaches the setting current limit, the LS-FET turns off. The LS-FET current signal is blanked for about 80ns internally to enhance noise immunity.

Enable (EN) and Programmable UVLO

EN enables and disables the MP3432. When applying a voltage higher than the EN high threshold (1V max threshold), the MP3432 starts up some of the internal circuits (micro-power mode). If the EN voltage exceeds the turn-on threshold (1.23V), the MP3432 enables all functions and starts boost operation. Boost switching is disabled when the EN voltage falls below its turn-on threshold (1.23V). To completely shut down the MP3432, a <0.4V low-level voltage is required on EN. After shutdown, the MP3432 sinks a current from the input power (less than 2µA, typically). EN is compatible with voltages up to 13V. For automatic start-up, connect EN to V_{IN} directly.

The MP3432 features a programmable UVLO hysteresis. When powering up in micro-power mode, EN sinks a 5μA current from an upper resistor (R_{TOP}) (see Figure 2).

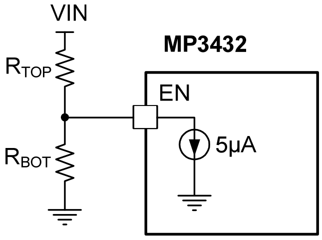


Figure 2: VIN UVLO Program

V_{IN} must increase to overcome the current sink. The V_{IN} start-up threshold is determined by Equation (2):

$$V_{IN-ON} = V_{EN-ON} \times (1 + \frac{R_{TOP}}{R_{BOT}}) + 5\mu A \times R_{TOP} \quad (2)$$

Where V_{EN-ON} is the EN voltage turn-on threshold (1.23V, typically).

Once the EN voltage reaches V_{EN-ON}, the 5μA sink current turns off to create a reverse hysteresis for the V_{IN} falling threshold, which can be calculated with Equation (3):

$$V_{IN-UVLO-HYS} = 5\mu A \times R_{TOP} \quad (3)$$

Over-Voltage Protection (OVP)

If over-voltage is detected from V_{OUT} with a 16.5V threshold (typically), the MP3432 stops switching immediately until the voltage drops to 16.3V. This prevents over-voltage on the output and internal power MOSFETs.

Thermal Protection

Thermal shutdown prevents the IC from operating at exceedingly high temperatures. When the die temperature exceeds 150°C, the IC shuts downs and resumes normal operation when the die temperature drops to 25°C.

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider is used to set the output voltage. Typically, choose R1 to be between 300 - 800kΩ. Then calculate R2 with Equation (4):

$$R2 = \frac{V_{REF}}{V_{OUT} - V_{REF}} \times R1 \qquad (4)$$

Where V_{REF} is 1V, R1 is the top feedback resistor, and R2 is the bottom feedback resistor.

Selecting the Input Capacitor

The input capacitor (C1) is used to maintain the DC input voltage. Low ESR ceramic capacitors are recommended. The input voltage ripple can be estimated with Equation (5):

$$\Delta V_{IN} = \frac{V_{IN}}{8f_s^2 \cdot L \cdot C1} \cdot \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \qquad (5)$$

Where f_S is the switching frequency, and L is the inductor value.

Selecting the Output Capacitor

The output current of the boost converter is discontinuous and therefore requires an output capacitor (C2) to supply AC current to the load. For the best performance, low ESR ceramic capacitors are recommended. The output voltage ripple can be estimated with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \cdot R_L \cdot C2} \cdot \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \qquad (6)$$

Where R_L is the value of the load resistor.

Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients.

Selecting the Inductor

An inductor is required to transfer the energy between the input source and the output capacitors. An inductor with a larger value results in less ripple current and a lower peak inductor current, reducing stress on the power MOSFET. However, the larger value inductor has a larger physical size, a higher series resistance, and a lower saturation current.

For most designs, the inductance value can be calculated with Equation (7):

$$L = \frac{V_{IN}(V_{OUT} - V_{IN})}{f_s \cdot V_{OUT} \cdot \Delta I_L} \qquad (7)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current to be approximately 20 ~ 50% of the average inductor current. Typically, a 1.5µH inductor is recommended. Ensure that the inductor does not saturate under the worst-case condition. The inductor should have a low series resistance (DCR) to reduce the resistive power loss.

Soft-Start (SS) Capacitor Selection

With the required output voltage rising time (T_{RISE}), the value of C_{SS} can be calculated using Equation (8):

$$C_{SS} = \frac{T_{RISE} \times I_{SS}}{V_{REF}} \qquad (8)$$

Where I_{SS} is the SS charging current (7.5µA). Typically, set C_{SS} to be 22nF for about 3ms of the rising time.

Switching Peak Current Limit Setting

The ILIM resistor (R5) is used to set the input current limit. Calculate R5 with Equation (9):

$$R_{ILIM} = \frac{320}{I_{LIM}} + 4 \qquad (9)$$

For example, if the required peak current limit is 10A, then R5 is 36kΩ.

VDD Capacitor Selection

The MP3432 integrates the VDD power at about 3.4V, which powers the internal MOSFET gate driver and internal control circuit, typically. One ceramic bypass capacitor 4.7µF or higher is necessary for the internal regulator. Do not connect the external load to the VDD power.

BST Capacitor

The MP3432 uses one bootstrap circuit to power the output N-channel MOSFET. One external bootstrap capacitor is necessary for the charge pump power. A 0.1µF ceramic capacitor between BST and SW is recommended.

Programmable UVLO

The MP3432 features a programmable UVLO hysteresis. When powering up, EN sinks a 5µA current from an upper resistor (R_{TOP}) (see Figure 2). V_{IN} must increase to overcome the current sink.

Determine the V_{IN} start-up threshold with Equation (10):

$$V_{IN-ON} = V_{EN-ON} \times (1 + \frac{R_{TOP}}{R_{BOT}}) + 5\mu A \times R_{TOP} \quad (10)$$

Where V_{EN-ON} is the EN voltage turn-on threshold (typically 1.23V).

Once the EN voltage reaches V_{EN-ON}, the 5µA sink current turns off to create a reverse hysteresis for the V_{IN} falling threshold, which can be calculated with Equation (11):

$$V_{IN-UVLO-HYS} = 5\mu A \times R_{TOP} \quad (11)$$

For automatic start-up, connect EN with a 30kΩ R_{TOP} resistor to operate with 150mV hysteresis.

MODE Selection

The MP3432 can work in forced continuous conduction mode (FCCM), pulse-skip mode (PSM), or ultrasonic mode (USM) based on the MODE setting. Pull MODE to VDD directly for FCCM; float MODE for USM; pull the MODE voltage to 0.2 - 0.7V to make the MP3432 work in PSM. With no appropriate voltage for the PSM threshold, a resistor divider from VDD to GND can be used (see Figure 3).

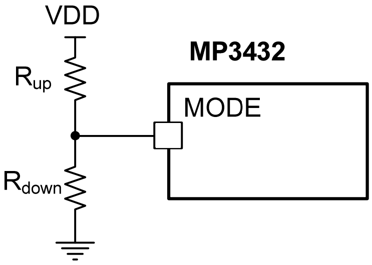


Figure 3: MODE Setting

The typical VDD voltage range is 2V to 3.3V. Set R_{up} to 130kΩ and R_{down} to 20kΩ to achieve a 267 - 450mV voltage on MODE. When MODE is pulled below 1V, a current less than 2µA flows out of MODE. A 20kΩ R_{BOT} causes a 40mV MODE voltage increase. The ideal MODE voltage is 307 - 490mV.

Compensation

The output of the transconductance error amplifier (COMP) is used to compensate for the regulation control system. The system uses two poles and one zero to stabilize the control loop.

The pole F_{P1} is set by the output capacitor (C_{OUT}) and the load resistance. Pole F_{P2} starts from the origin. The zero F_{Z1} is set by the compensation capacitor (C_{COMP}) and the compensation resistor (R_{COMP}). These are determined by Equation (12) and Equation (13):

$$F_{P1} = \frac{1}{2 \times \pi \times R_{LOAD} \times C_{OUT}} (Hz) \quad (12)$$

$$F_{Z1} = \frac{1}{2 \times \pi \times R_{COMP} \times C_{COMP}} (Hz) \quad (13)$$

Where R_{LOAD} is the load resistance.

There is a right-half-plane zero (F_{RHPZ}) that exists in FCCM, where the inductor current does not drop to zero in each cycle. The frequency of the right-half-plane zero can be determined with Equation (14):

$$F_{RHPZ} = \frac{R_{LOAD}}{2 \times \pi \times L} \times (\frac{V_{IN}}{V_{OUT}})^2 (Hz) \quad (14)$$

The right-half-plane zero increases the gain and reduces the phase simultaneously, which results in a smaller phase margin and gain margin. The worst-case happens at the condition of the minimum input voltage and maximum output power.

PCB Layout Guidelines

Efficient PCB layout is critical for high-frequency switching power supplies. A poor layout can result in reduced performance, excessive EMI, resistive loss, and system instability. Use a 4-layer PCB for high-power applications. For best results, refer to Figure 4 and follow the guidelines below.

1. Place the output capacitor (C2A ~ C2C) as close to V_{OUT} and PGND as possible.

2. Place a 0.1μF capacitor close to the IC (C2D) to reduce the PCB parasitical inductance.
3. Keep the connection of V_{OUT} and PGND to the output capacitor short and wide with copper.
4. Place the copper, the IC, and C_{OUT} on the same layer.
5. Place the FB divider R1 and R2 as close to FB as possible.
6. Keep the FB trace far away from noise sources, such as the SW node.
7. Place the current limit setting resister (R4) close to ILIM.
8. Connect the ILIM resistor (R4) ground to AGND.
9. Connect the compensation components and SS capacitor to AGND with a short loop.
10. Connect the VDD capacitor to PGND with a short loop.
11. Keep the input loop (C1, L1, SW, and PGND) as small as possible.
12. Places enough GND vias close to the MP3432 for good thermal dissipation.
13. Use separated AGND and PGND layouts connected between the AGND and PGND pins under the package.

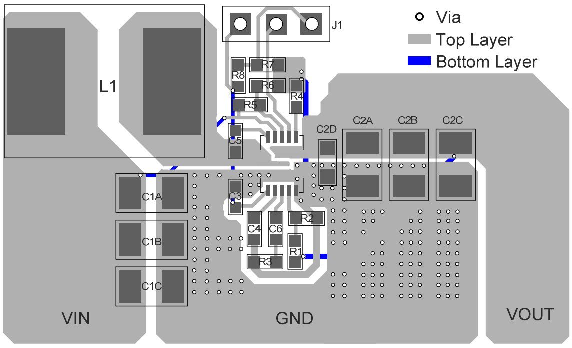


Figure 4: Layout Recommendation

Design Example

Table 1 is a design example following the application guidelines for the specifications below.

Table 1: Design Example

V_{IN}	3 - 8.4V
SW I_{Peak}	14A
V_{OUT}	9V
I_{OUT}	3.5A

The detailed application schematic is shown in Figure 5. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section. For more device applications, please refer to related evaluation board datasheet.

TYPICAL APPLICATION CIRCUITS

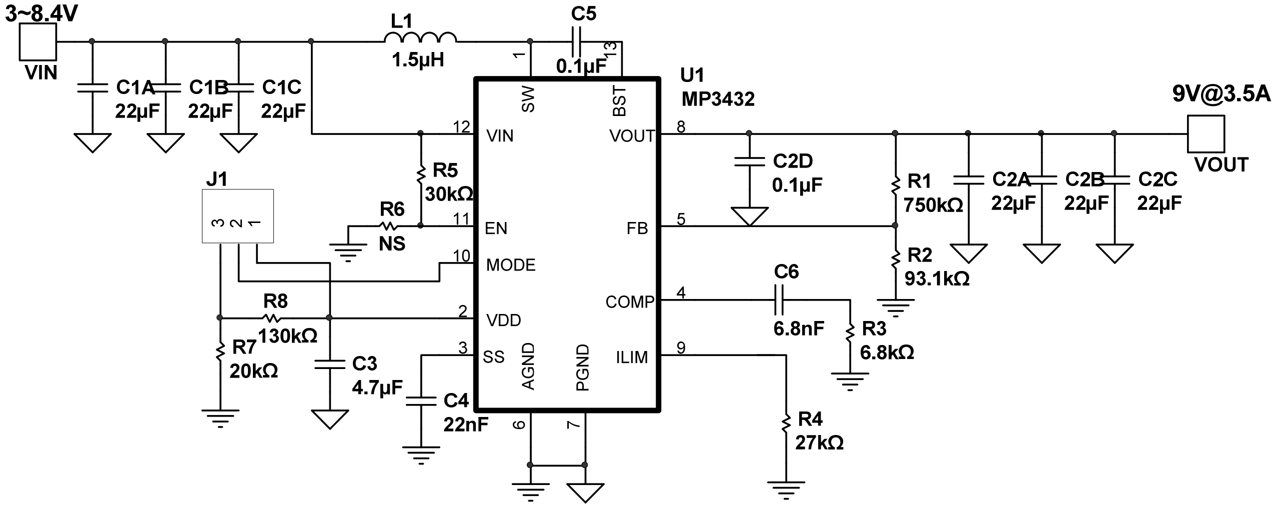
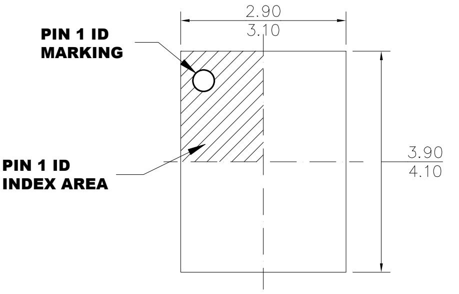


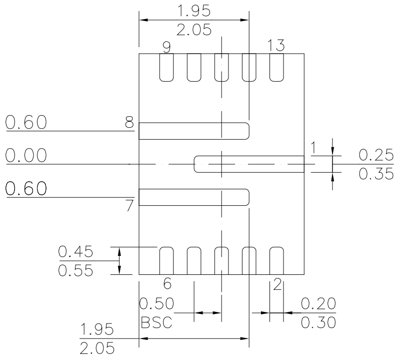
Figure 5: Typical Circuit with 14A Switching Peak Current Limit, V_{IN} = 3 - 8.4V, V_{OUT} = 9V, I_{OUT} = 3.5A

PACKAGE INFORMATION

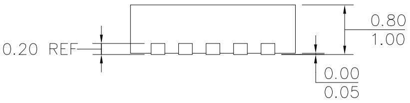
QFN-13 (3mmx4mm)



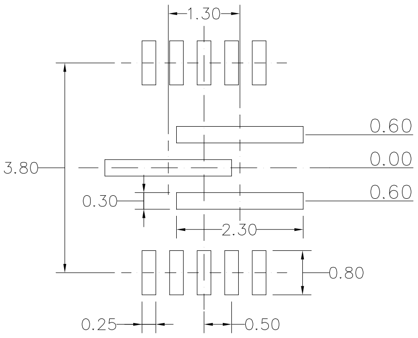
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) LAND PATTERNS OF PIN1,7 AND 8 HAVE THE SAME LENGTH AND WIDTH.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.