MPQ4360

40V, 6A, Low I_Q, Synchronous Step-Down Converter, AEC-Q100 Qualified

DESCRIPTION

The MPQ4360 is a configurable-frequency, synchronous, step-down switching converter with integrated, internal high-side and low-side power MOSFETs. The device provides up to 6A of highly efficient output current, with current mode control for fast loop response.

The wide 3.3V to 40V input voltage range accommodates a variety of step-down applications in an automotive input environment. The 1.7μA shutdown mode quiescent current allows the part to be used in battery-powered applications.

High power conversion efficiency across the wide load range is achieved by scaling down the switching frequency under light-load conditions to reduce the switching and gate driving losses.

An open-drain power good signal indicates that the output is within 95% to 105% of its nominal voltage.

Frequency foldback helps prevent inductor current runaway during start-up. Thermal shutdown provides reliable, fault-tolerant operation. A high duty cycle and low-dropout mode are provided for automotive cold-crank conditions.

The MPQ4360 is available in a QFN-20 (4mmx4mm) package.

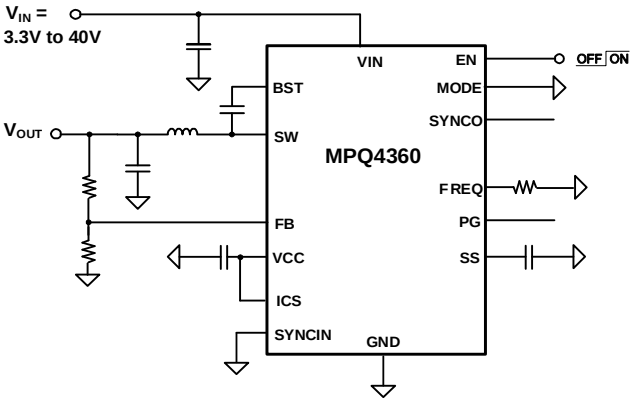
FEATURES

- **Designed for Automotive Applications:**
  - Wide 3.3V to 40V Operating Voltage Range
  - Low Dropout Mode
  - 6A Continuous Output Current.
  - 100ns Minimum On Time
  - Multi-Phase Capability
  - Junction Temperature Operation from -40°C to +150°C
  - Available in AEC-Q100 Grade 1
- **Increased Battery Life:**
  - Low 1.7μA Shutdown Supply Current.
  - 22μA Quiescent Current with Switching
  - AAM Increases Efficiency under Light Loads
- **High Performance for Improved Thermals:**
  - Internal 50mΩ High-Side and 22mΩ Low-Side MOSFET
- **Optimized for EMC/EMI:**
  - 350kHz to 1000kHz Configurable f_{SW}
  - Up to 2.2MHz Configurable f_{SW} for V_{OUT} ≥5V Car Battery Applications
  - Symmetric VIN Pinout
  - Synchronize to External Clock
  - Out-of-Phase Synchronized Clock Output
  - CISPR25 Class 5 Compliant
  - MeshConnect™ Flip-Chip Package
- **Additional Features:**
  - Power Good Output
  - External Soft Start
  - Hiccup Over-Current Protection (OCP)
  - Available in a QFN-20 (4mmx4mm) Package with Wettable Flank

APPLICATIONS

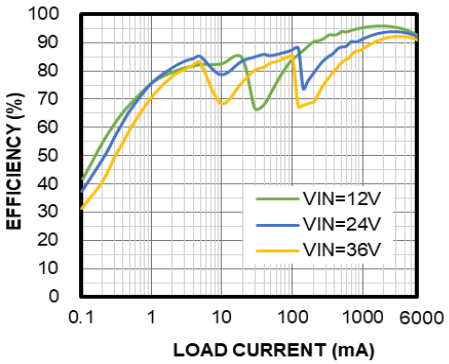
- Automotive Infotainment
- Automotive Clusters
- Automotive Telematics
- Industrial Power Systems

TYPICAL APPLICATION



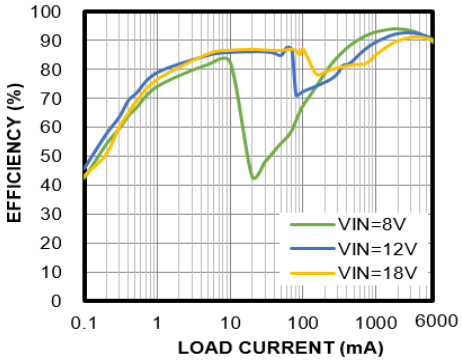
Efficiency vs. Load Current

V_{OUT} = 5V, f_{SW} = 470kHz, L = 4.7µH (DCR = 15mΩ), AAM



Efficiency vs. Load Current

V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 1µH (DCR = 8.5mΩ), AAM



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating**
MPQ4360GRE-AEC1***	QFN-20 (4mmx4mm)	*See Below*	1

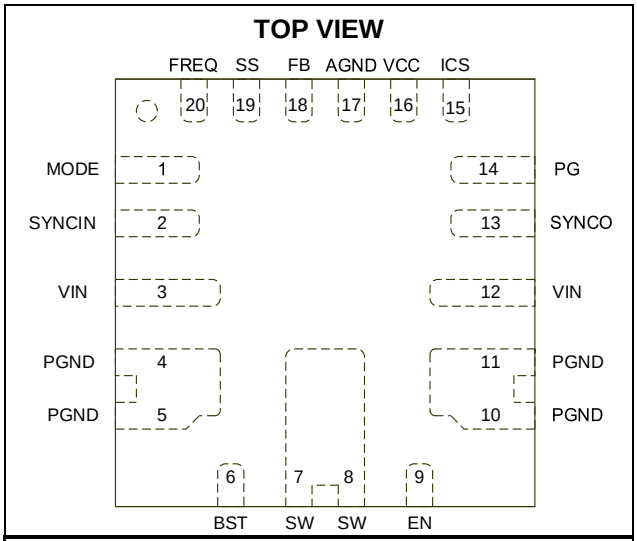
* For Tape & Reel, add suffix -Z (e.g. MPQ4360GRE-AEC1-Z).
**Moisture Sensitivity Level Rating
*** Wettable Flank

TOP MARKING

MPSYWW
MP4360
LLLLLL
E

MPS: MPS prefix
Y: Year code
WW: Week code
MP4360: Part number
LLLLLL: Lot number
E: Wettable flank

PACKAGE REFERENCE



QFN-20 (4mmx4mm)

PIN FUNCTIONS

Pin #	Name	Description
1	MODE	**AAM or FCCM selection pin.** Pull the MODE pin high for forced continuous conduction mode (FCCM). Pull MODE low for advanced asynchronous modulation (AAM) mode under light loads. Do not float the MODE pin.
2	SYNCIN	**SYNC input.** Apply a 350kHz to 2.2MHz clock signal to this pin to synchronize the internal oscillator frequency to the external clock (except for applications where V_{OUT} < 5V). This pin is also used for multi-phase operation. Do not float the SYNCIN pin. SYNCIN has an internal high impedance. Ensure that the external sync clock has adequate pull-up and pull-down capability. It is recommended to place a ⩽51kΩ resistor between SYNCIN and GND in case the external sync clock pull-down capability is not strong enough or the pin enters a high-impedance state.
3, 12	VIN	**Input supply.** VIN supplies power to all the internal control circuitry and the power switch connected to SW. It is recommended to place a decoupling capacitor from VIN to ground, and place it close to VIN to minimize switching spikes.
4, 5, 10, 11	PGND	**Power ground.**
6	BST	**Bootstrap.** BST is the positive power supply for the high-side MOSFET driver connected to SW. Connect a bypass capacitor between BST and SW. See the External BST Diode and Resistor section on page 38 to calculate the size of the capacitor
7, 8	SW	**Switch node.** SW is the output of the internal power switch.
9	EN	**Enable.** Pull the EN pin below the specified threshold (0.85V) to shut down the chip. Pull EN above the specified threshold (1V) to enable the chip.
13	SYNCO	**SYNC output.** Output a clock signal 180° out-of-phase with the internal oscillator signal, or make it opposite to the clock signal applied at the SYNCIN pin. Float SYNCO if it is not used.
14	PG	**Power good indicator.** The output of PG is an open drain. Connect PG to the power source using a pull-up resistor if PG is used. PG goes high if the output voltage is within 95% to 105% of the nominal voltage. PG goes low if the output voltage is above 106.5% or below 93.5% of the nominal voltage.
15	ICS	**Current sharing pin.** In a multi-phase application, connect the ICS pin of the device in parallel to improve the current sharing between different phases. Do not float ICS. Connect ICS to the VCC pin, or connect it to an output that is at least 3V in a single-phase application.
16	VCC	**Biased supply.** The VCC pin supplies 4.9V of power to the internal control circuit and gate drivers. Place a decoupling capacitor close to this pin. See the Setting the VCC Capacitor section on page 38 to calculate the size of the capacitor.
17	AGND	**Analog ground.**
18	FB	**Feedback input.** To set the output voltage, connect FB to the center point of the external resistor divider, from the output to AGND. The feedback threshold is 0.815V. Place the resistor divider as close to FB as possible. Avoid placing vias on the FB traces.
19	SS	**Soft-start input.** Place a capacitor from SS to GND to set the soft-start period. The MPQ4360 sources 6μA from SS to the soft-start capacitor at start-up. As the SS voltage rises, the feedback threshold voltage increases to limit inrush current during start-up.
20	FREQ	**Switching frequency configuration.** Connect a resistor from FREQ to ground to set the switching frequency. See the f_{SW} vs. R_{FREQ} curves on page 15 to set the frequency.

ABSOLUTE MAXIMUM RATINGS (1)

VIN, EN ..... -0.3V to +50V
SW ..... -0.3V to $V_{IN(MAX)}$ + 0.3V
BST ..... V_{SW} + 5.5V
All other pins..... -0.3V to +5.5V
Continuous power dissipation (T_A = 25°C) (2) (6)
QFN-20 (4mmx4mm).....5.4W
Operating junction temperature.....+150°C
Lead temperature .....+260°C
Storage temperature.....-65°C to +150°C

ESD Ratings

Human body model (HBM) ..... Class 2 (3)
Charged device model (CDM).....Class C2b (4)

Recommended Operating Conditions

Supply voltage (V_{IN}) ..... 3.3V to 40V
Output Voltage (V_{OUT}) ..... 0.815V to 0.95 x V_{IN}
Operating junction temp (T_J) ....-40°C to +150°C

Thermal Resistance	***θ_{JA}***	***θ_{JC}***	
QFN-20 (4mmx4mm)			
JESD51-7 (5)	44	9	°C/W
EVQ4360-R-00A(6)	23	2.5	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Per AEC-Q100-002.
4) Per AEC-Q100-011.
5) Measured on JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.
6) Measured on EVQ4360-R-00A, 9cmx9cm, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +125°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
VIN UVLO rising threshold	IN_{UVLO_RISING}		2.8	3.0	3.2	V
VIN UVLO falling threshold	$IN_{UVLO\_FALLING}$		2.5	2.7	2.9	V
VIN UVLO hysteresis	IN_{UVLO_HYS}			280		mV
VCC voltage	V_{CC}	I_{VCC} = 0A	4.6	4.9	5.2	V
VCC regulation		I_{VCC} = 30mA		1	4	%
VCC current limit	I_{LIMIT_VCC}	V_{CC} = 4V	100			mA
VIN quiescent current	I_Q	FB = 0.85V, no load, sleep mode		20	30	µA
VIN quiescent current (switching) (7)	I_{Q_ACTIVE}	MODE = GND (AAM), switching, no load, R_{FB_UP} = 1MΩ, R_{FB_DOWN} = 324kΩ		22		µA
		MODE = high (FCCM), switching, f_{SW} = 2.2MHz, no load		42		mA
		MODE = high (FCCM), switching, f_{SW} = 470kHz, no load		10		mA
VIN shutdown current	I_{SHDN}	EN = 0V		1.7	2.5	µA
FB voltage	V_{FB}	VIN = 3.3V to 40V, T_J = 25°C	0.807	0.815	0.823	V
		VIN = 3.3V to 40V	0.799	0.815	0.831	V
FB current	I_{FB}	V_{FB} = 0.85V	-50	0	+50	nA
Switching frequency	f_{SW}	R_{FREQ} = 62kΩ	420	470	520	kHz
		R_{FREQ} = 12kΩ	1950	2200	2450	kHz
Minimum on time (7)	t_{ON_MIN}			100		ns
Minimum off time (7)	t_{OFF_MIN}			80		ns
SYNCIN voltage rising threshold	V_{SYNC_RISING}		1.8			V
SYNCIN voltage falling threshold	$V_{SYNC\_FALLING}$				0.4	V
SYNCIN clock range	f_{SYNC}	External clock	350		2200	kHz
SYNCO high voltage	V_{SYNCO_HIGH}	I_{SYNCO} = -1mA	3.3	4.5		V
SYNCO low voltage	V_{SYNCO_LOW}	I_{SYNCO} = 1mA			0.4	V
SYNCO phase shift		Tested under SYNCIN		180		Deg
HS current limit	I_{LIMIT}	Duty cycle = 30%, f_{SW} = 470kHz	10	13	16	A
		Duty cycle = 30%, f_{SW} = 2.2MHz	12.5	15.5	18.5	A
LS valley current limit	I_{LIMIT_VALLEY}		8	10	12	A
ZCD current	I_{ZCD}	AAM	-0.15	0.1	+0.35	A
LS reverse current limit	$I_{LIMIT\_REVERSE}$	FCCM	2	4.5	6.5	A

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +125°C, typical values are at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Switch leakage current	I_{SW_LKG}			0.01	1	µA
HS switch on resistance	R_{ON_HS}	V_{BST} - V_{SW} = 5V		50	83	mΩ
LS switch on resistance	R_{ON_LS}	V_{CC} = 5V		22	44	mΩ
Soft-start current	I_{SS}	V_{SS} = 0V	4	6	8	µA
EN rising threshold	V_{EN_RISING}		0.8	1.0	1.2	V
EN falling threshold	$V_{EN\_FALLING}$		0.65	0.85	1.05	V
EN hysteresis voltage	V_{EN_HYS}			180		mV
MODE rising threshold	V_{MODE_RISING}		1.8			V
MODE falling threshold	$V_{MODE\_FALLING}$				0.4	V
PG rising threshold (V_{FB} / V_{REF})	PG_{RISING}	V_{FB} rising	92%	95%	98%	V_{REF}
		V_{FB} falling	102%	105%	108%	
PG falling threshold (V_{FB} / V_{REF})	$PG_{FALLING}$	V_{FB} falling	90.5%	93.5%	96.5%	
		V_{FB} rising	103.5%	106.5%	109.5%	
PG output voltage low	V_{PG_LOW}	I_{SINK} = 1mA		0.1	0.3	V
PG rising delay	$t_{PG\_R\_DELAY}$			35		µs
PG falling delay	$t_{PG\_F\_DELAY}$			35		µs
Thermal shutdown (7)	t_{SD}			170		°C
Thermal shutdown hysteresis (7)	t_{SD_HYS}			20		°C

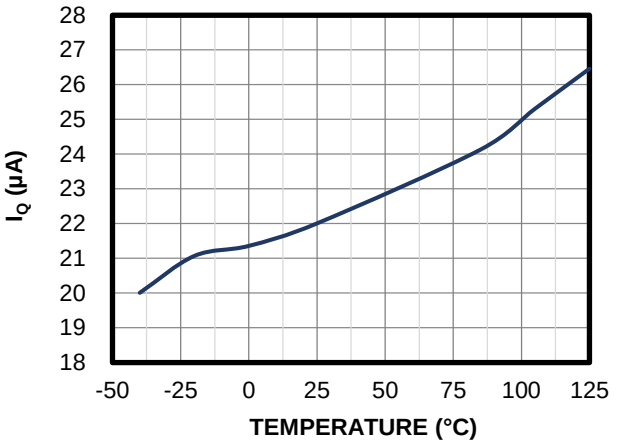
Note:

7) Derived from bench characterization. Not tested in production.

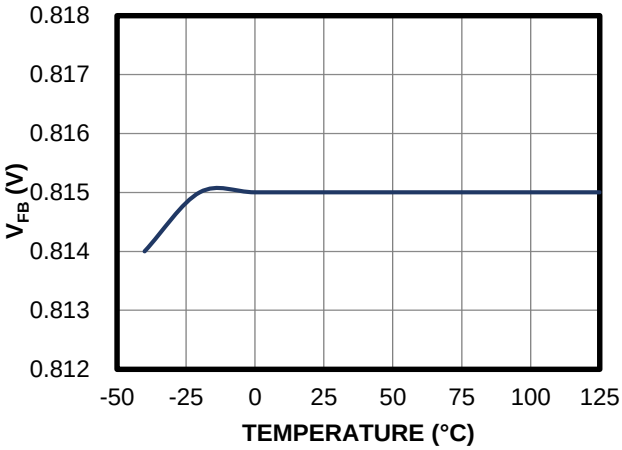
TYPICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

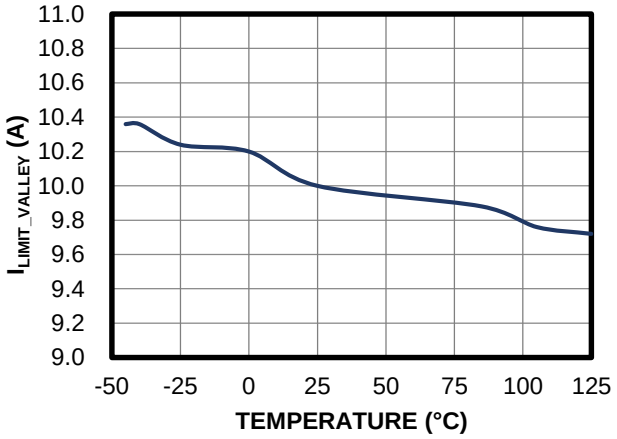
I_Q vs. Temperature



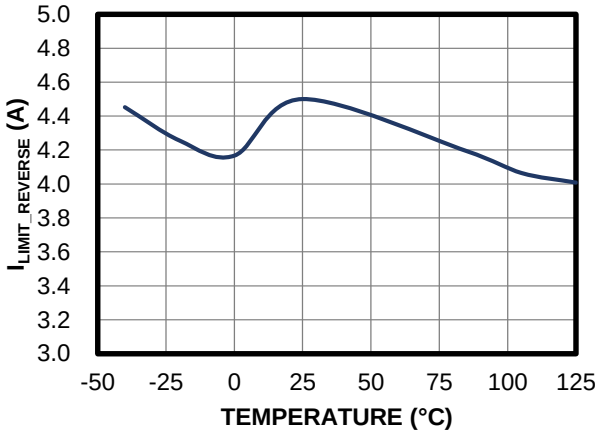
V_{FB} vs. Temperature



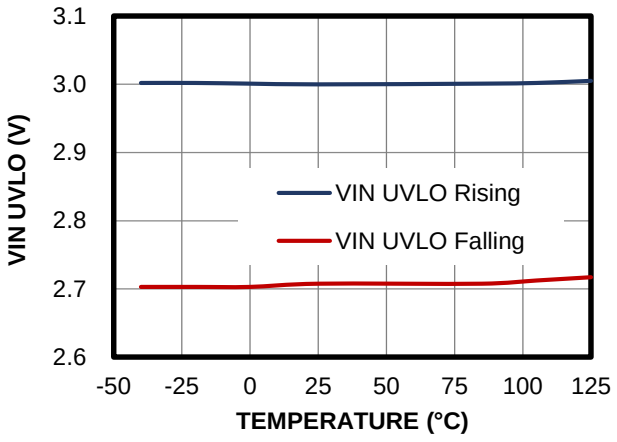
Valley Current Limit vs. Temperature



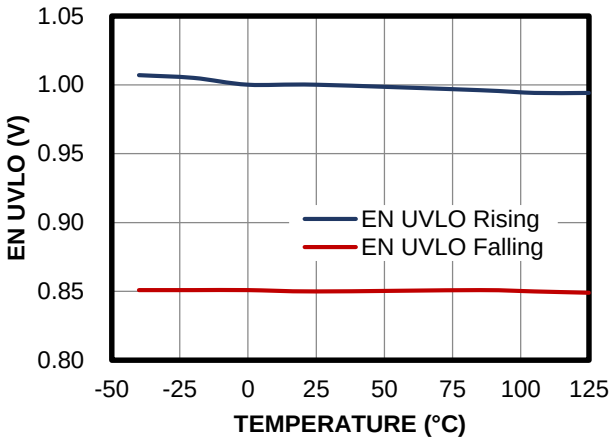
Reverse Current Limit vs. Temperature



V_{IN} UVLO Threshold vs. Temperature



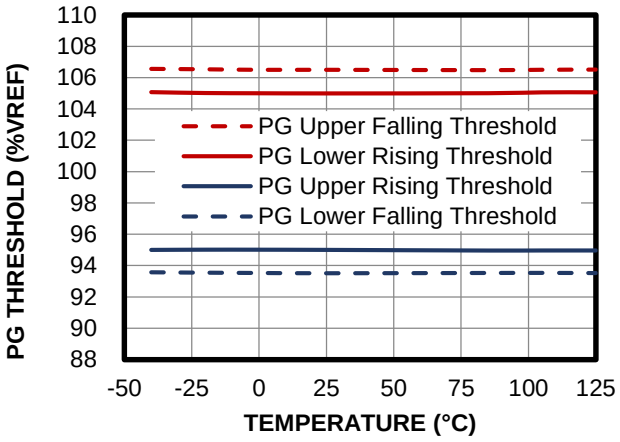
EN UVLO Threshold vs. Temperature



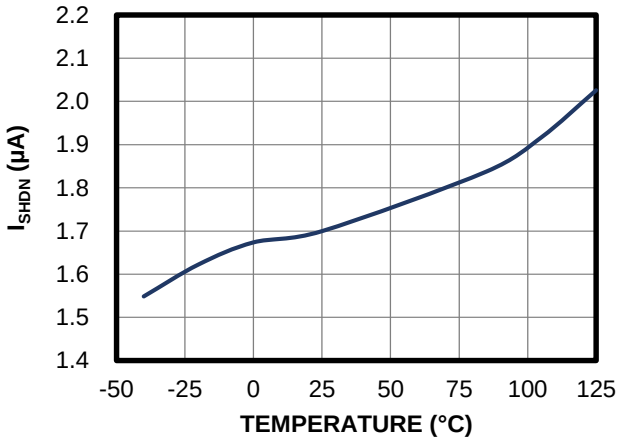
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

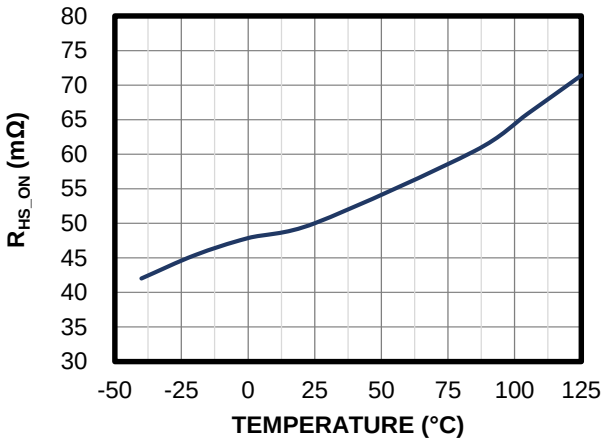
PG Rising/Falling Threshold vs. Temperature



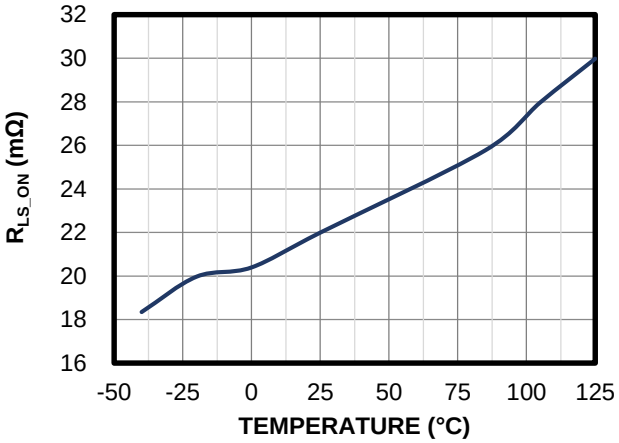
VIN Shutdown Current vs. Temperature



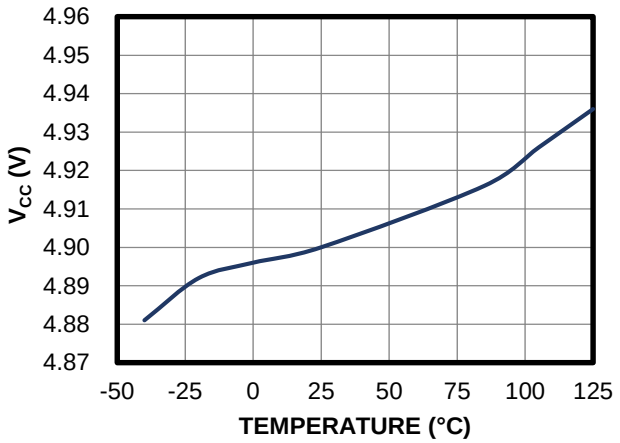
R_{HS_ON} vs. Temperature



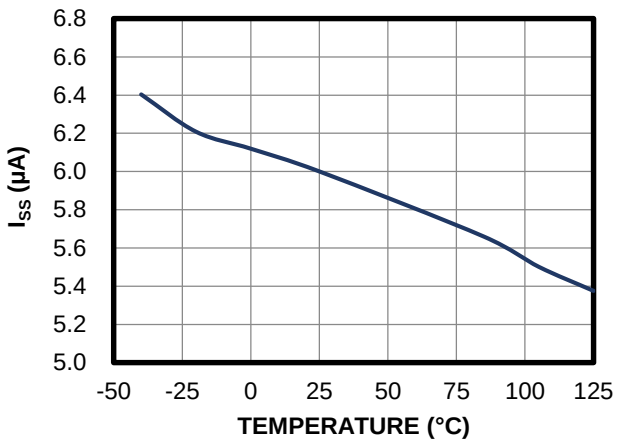
R_{LS_ON} vs. Temperature



V_{CC} vs. Temperature



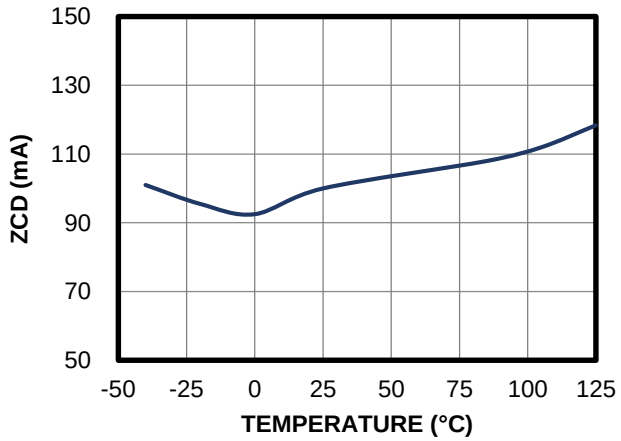
Soft-Start Current vs. Temperature



TYPICAL CHARACTERISTICS *(continued)*

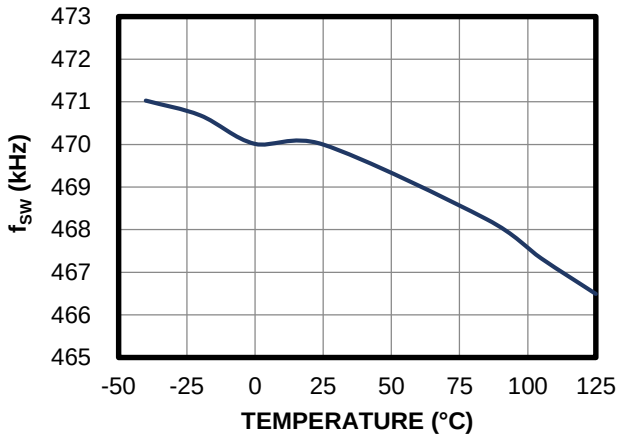
V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

ZCD vs. Temperature



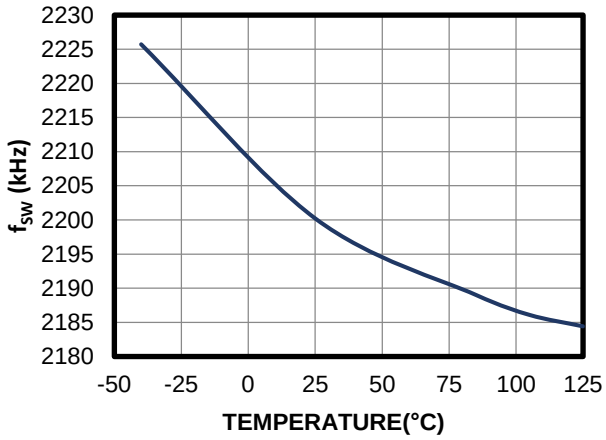
f_{SW} vs. Temperature

R_{FREQ} = 62kΩ



f_{SW} vs. Temperature

R_{FREQ} = 12kΩ

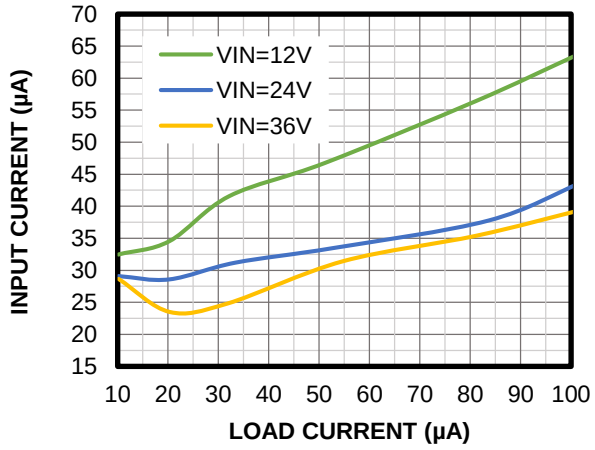


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH [8], f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

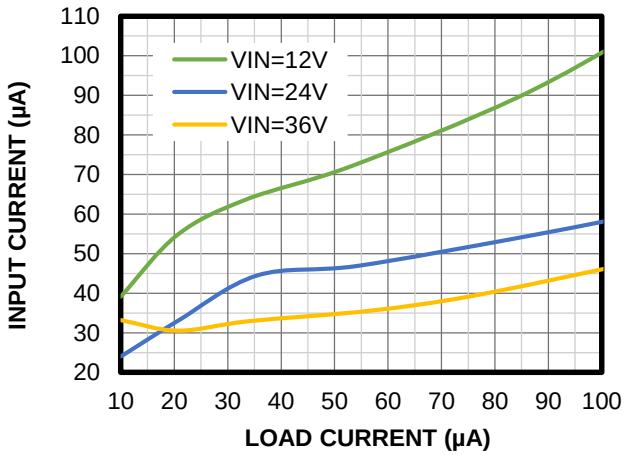
Input Current vs. Load Current

AAM,V_{OUT} = 3.3V



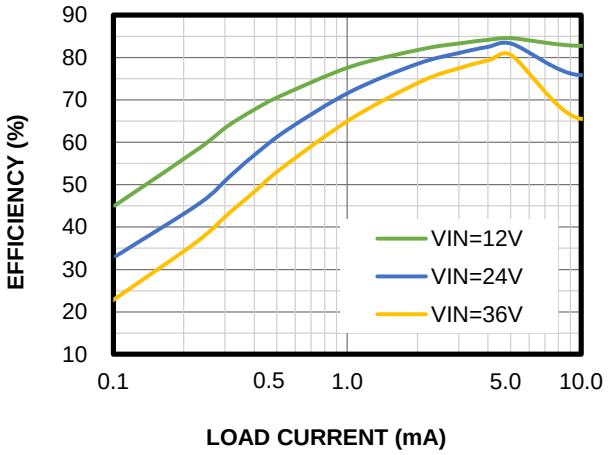
Input Current vs. Load Current

AAM, V_{OUT} = 5V



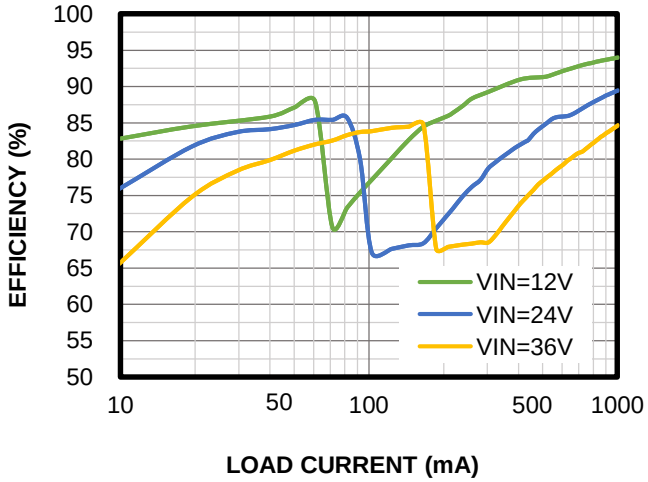
Efficiency vs. Load Current

AAM, V_{OUT} = 3.3V



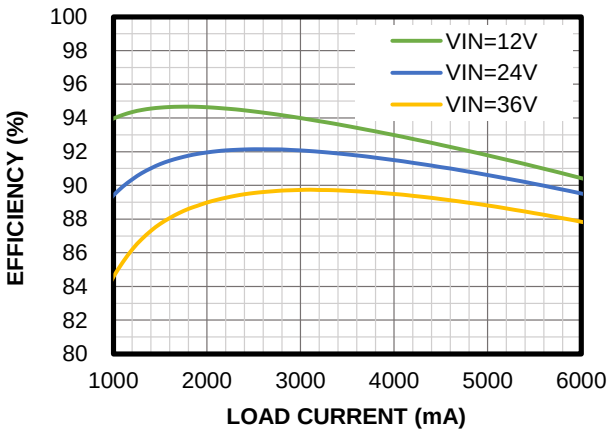
Efficiency vs. Load Current

AAM, V_{OUT} = 3.3V



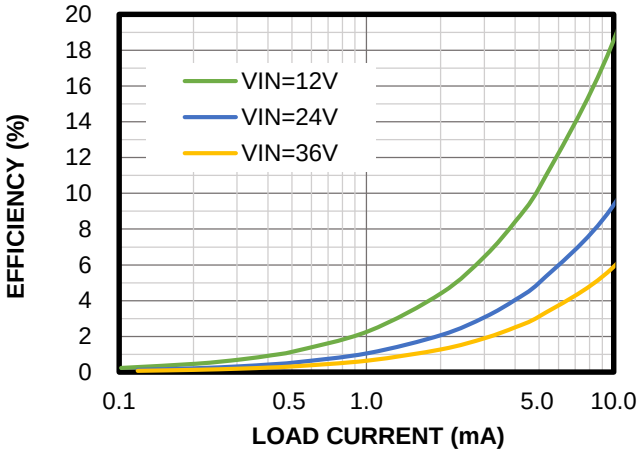
Efficiency vs. Load Current

AAM, V_{OUT} = 3.3V



Efficiency vs. Load Current

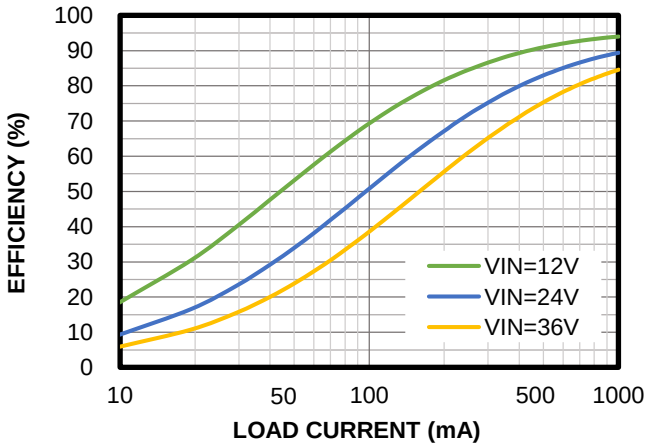
FCCM, V_{OUT} = 3.3V



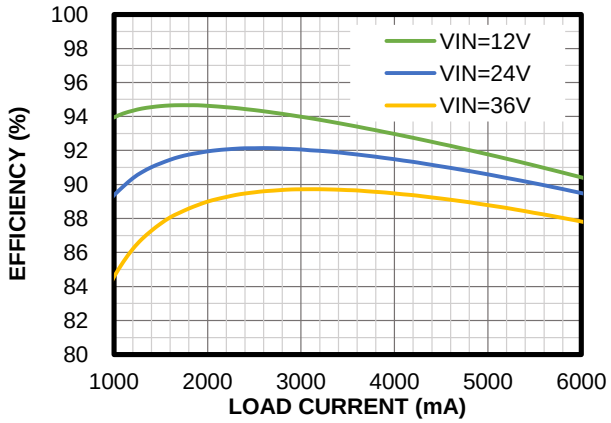
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH [8], f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

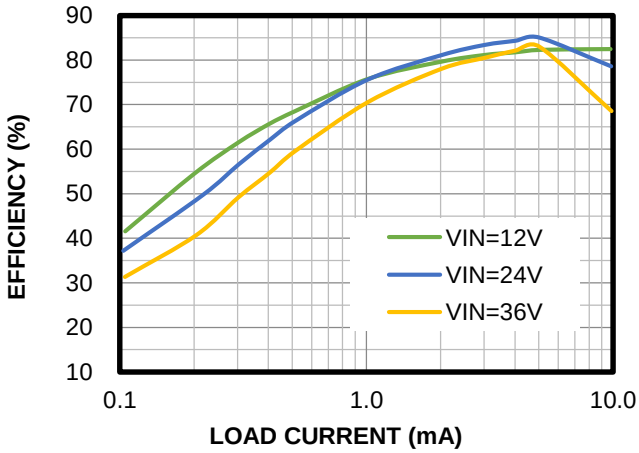
Efficiency vs. Load Current
FCCM,V_{OUT} = 3.3V



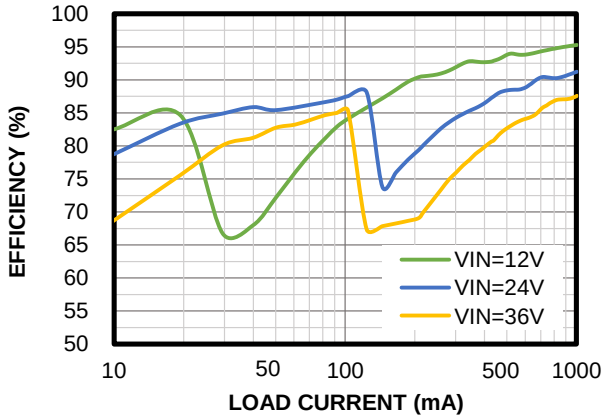
Efficiency vs. Load Current
FCCM, V_{OUT} = 3.3V



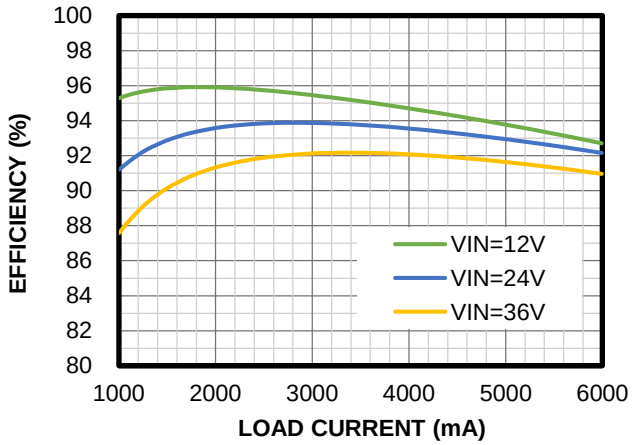
Efficiency vs. Load Current
AAM, V_{OUT} = 5V



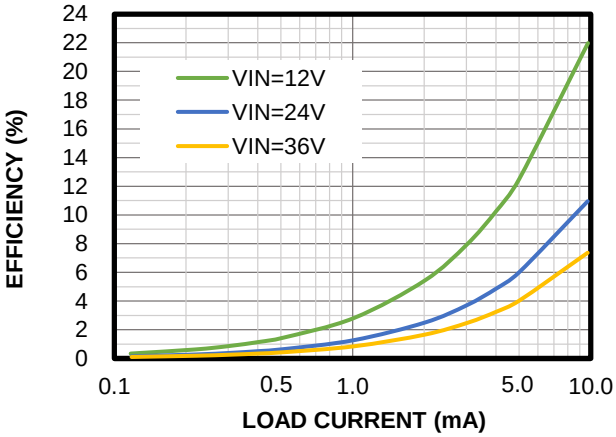
Efficiency vs. Load Current
AAM,V_{OUT} = 5V



Efficiency vs. Load Current
AAM,V_{OUT} = 5V



Efficiency vs. Load Current
FCCM, V_{OUT} = 5V

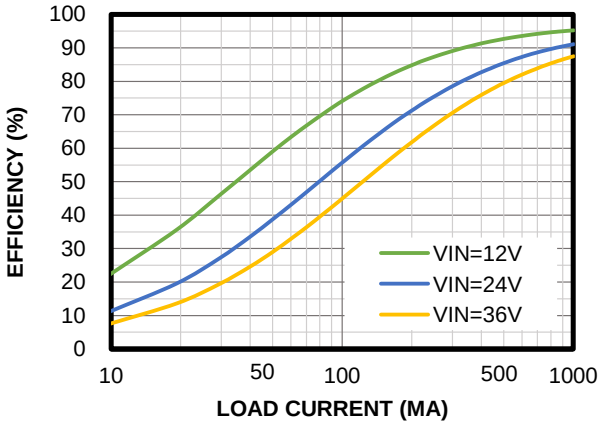


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH [8], f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

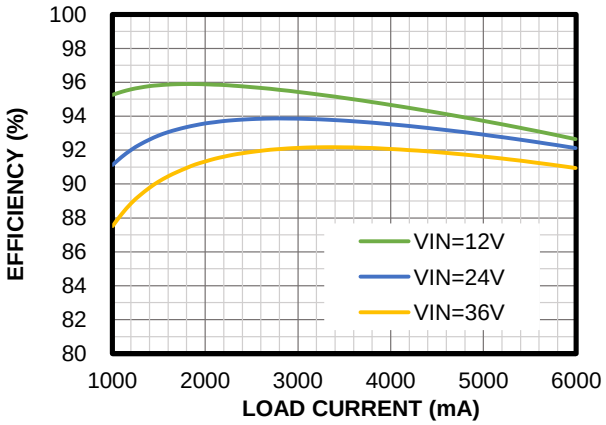
Efficiency vs. Load Current

FCCM, V_{OUT} = 5V



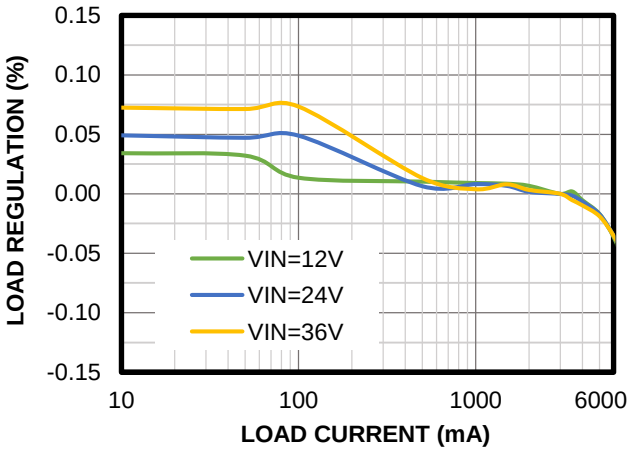
Efficiency vs. Load Current

FCCM, V_{OUT} = 5V



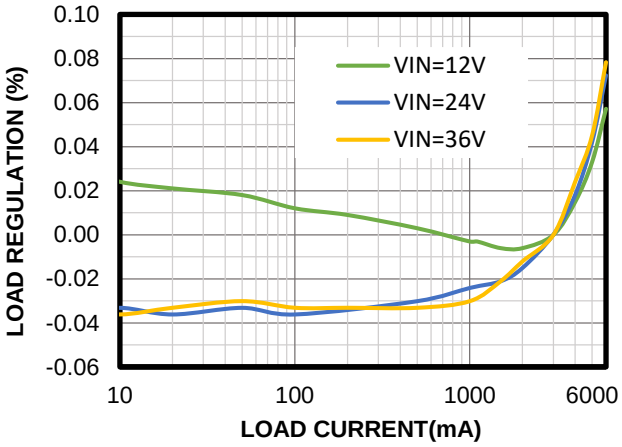
Load Regulation

AAM, V_{OUT} = 3.3V



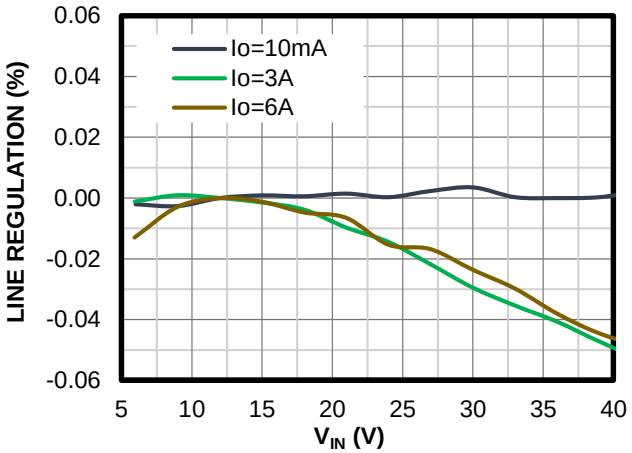
Load Regulation

FCCM, V_{OUT} = 3.3V



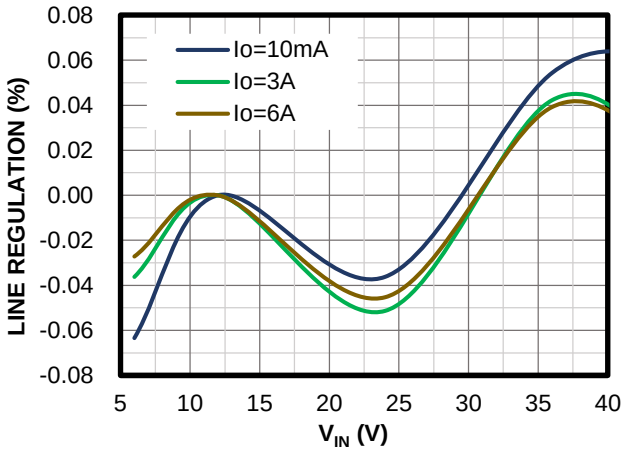
Line Regulation

AAM, V_{OUT} = 3.3V



Line Regulation

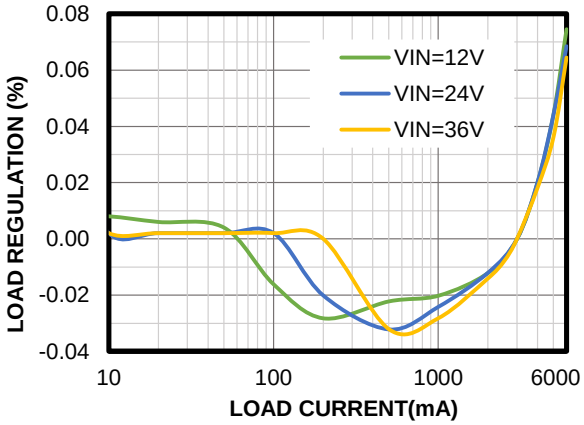
FCCM, V_{OUT} = 3.3V



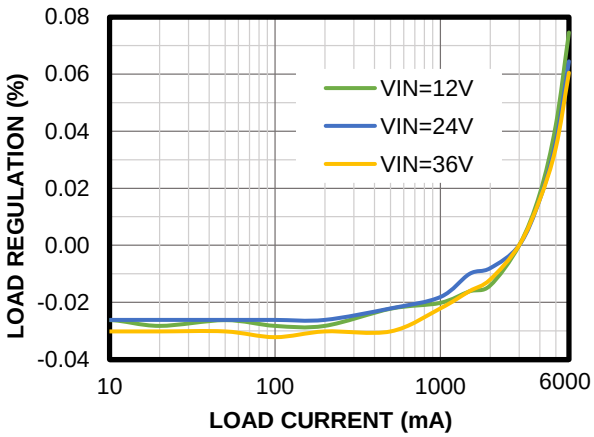
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH [8], f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

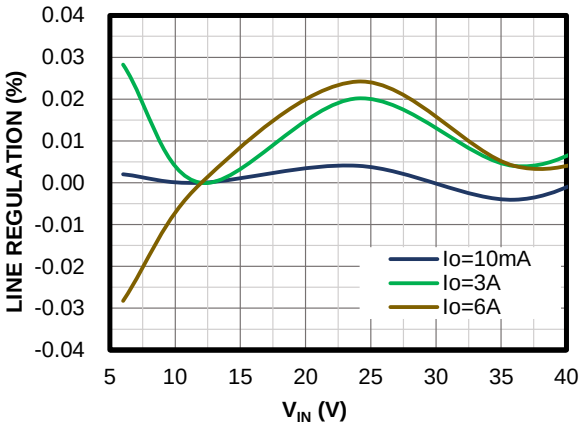
Load Regulation
AAM,V_{OUT} = 5V



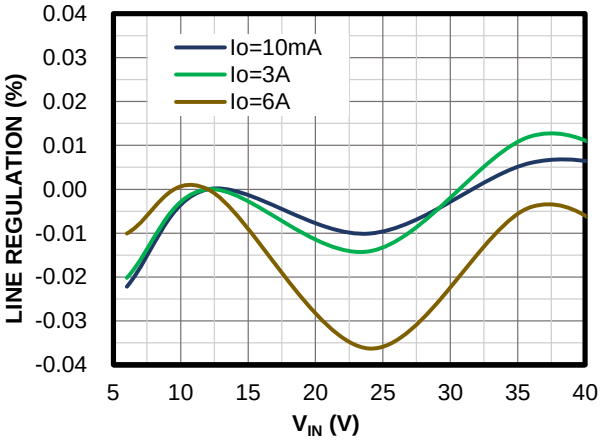
Load Regulation
FCCM, V_{OUT} = 5V



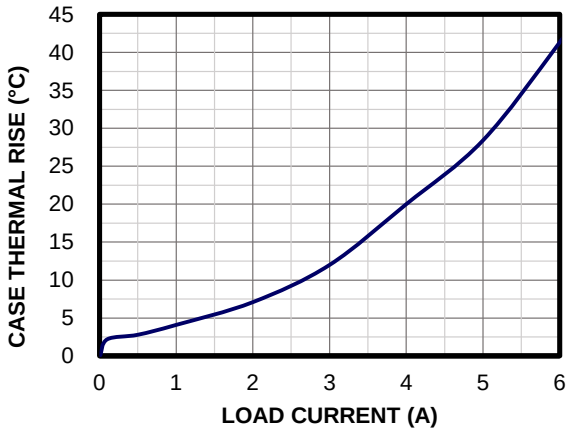
Line Regulation
AAM,V_{OUT} = 5V



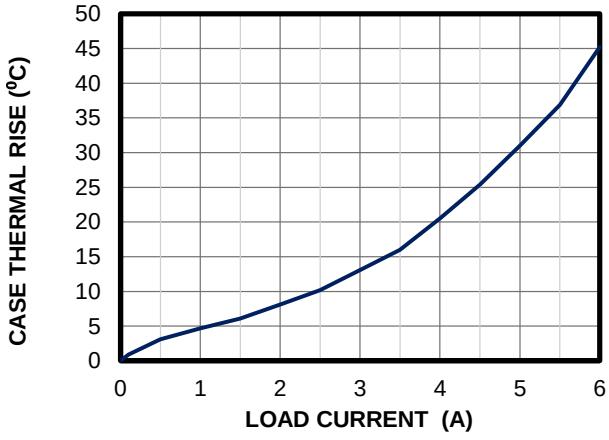
Line Regulation
FCCM, V_{OUT} = 5V



Case Thermal Rise
V_{OUT} = 3.3V



Case Thermal Rise
V_{OUT} = 5V

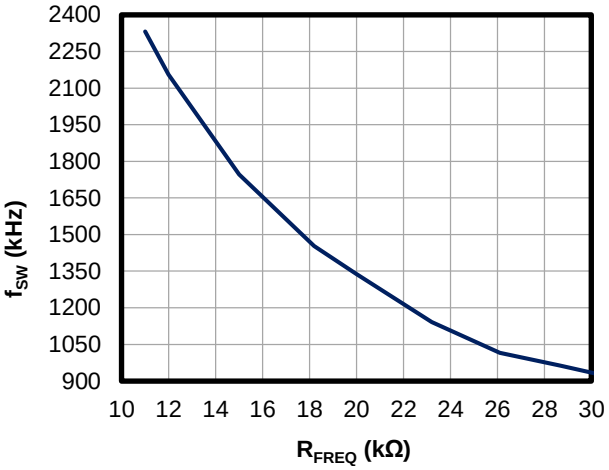


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH [8], f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

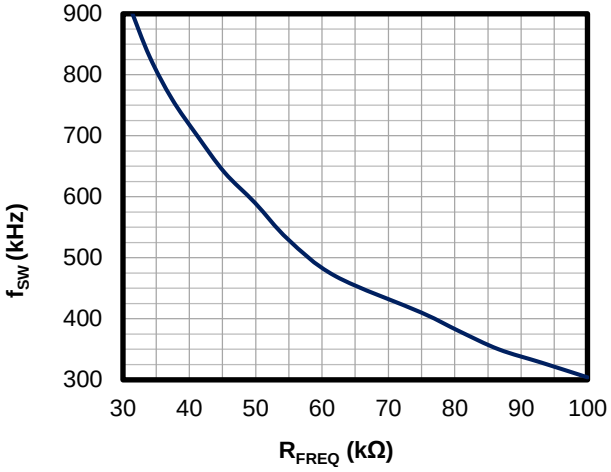
f_{SW} vs. R_{FREQ}

R_{FREQ} = 10kΩ to 30kΩ

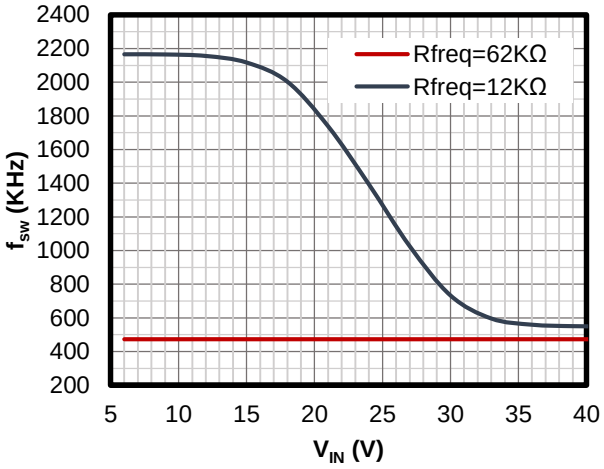


f_{SW} vs. R_{FREQ}

R_{FREQ} = 30kΩ to 100kΩ

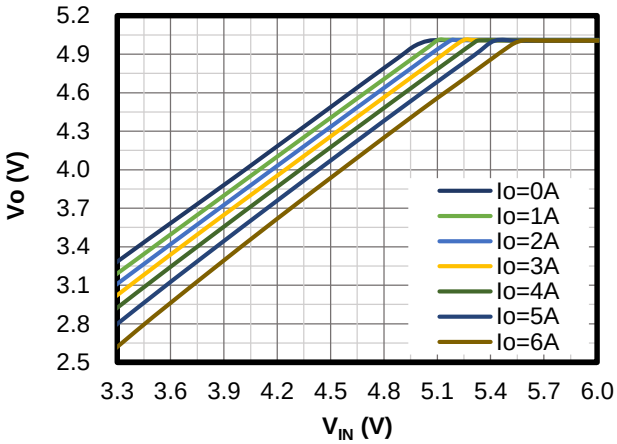


f_{SW} vs. V_{IN}



Low Dropout

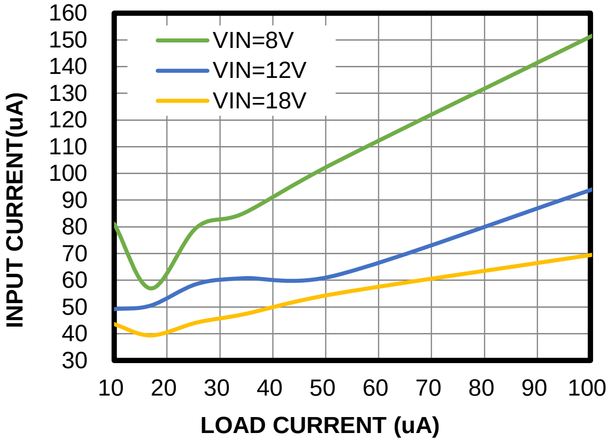
V_{OUT} = 5V



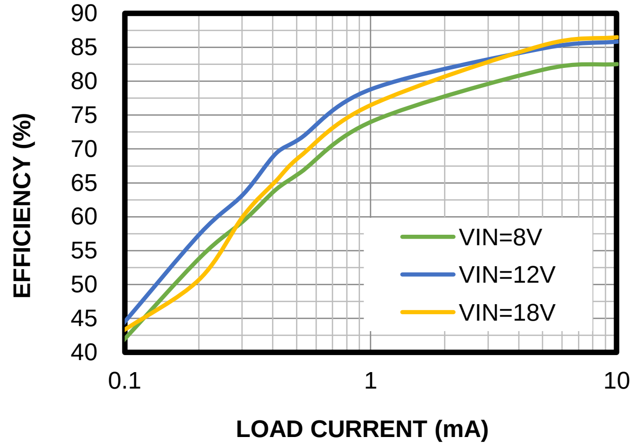
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH [9], f_{SW} = 2.2MHz, AAM, T_A = 25°C, unless otherwise noted.

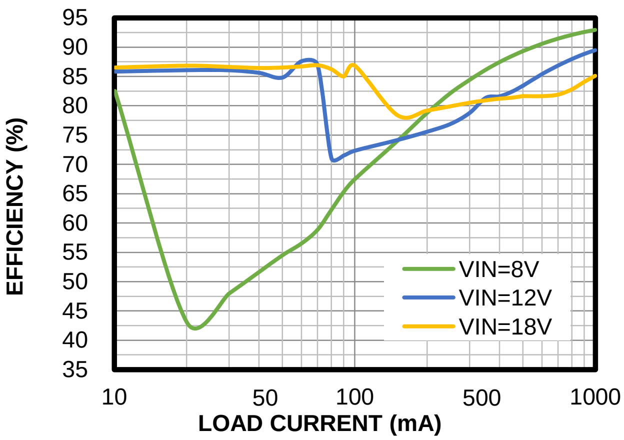
Input Current vs. Load Current
AAM



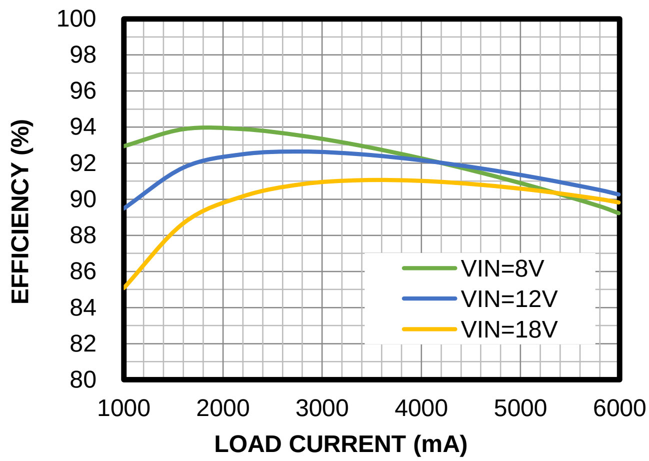
Efficiency vs. Load Current
AAM



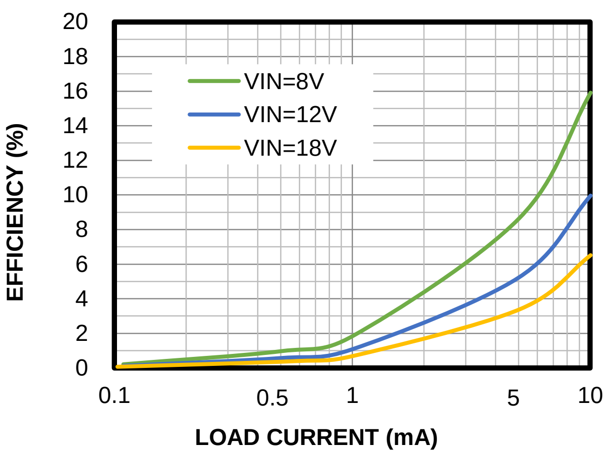
Efficiency vs. Load Current
AAM



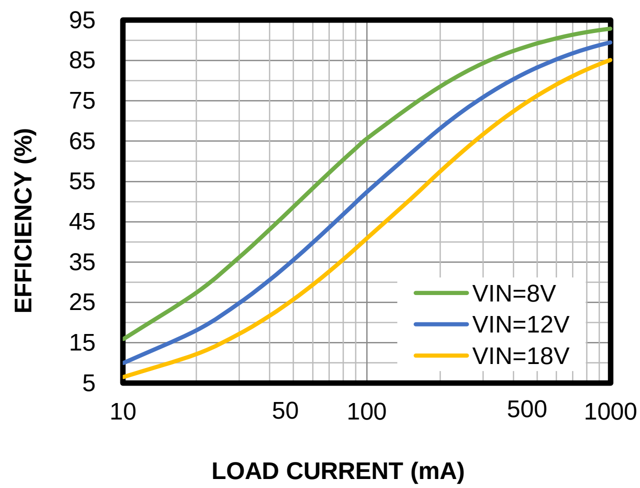
Efficiency vs. Load Current
AAM



Efficiency vs. Load Current
FCCM



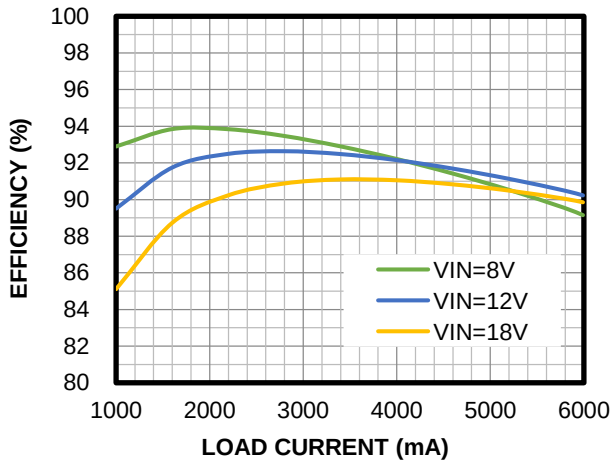
Efficiency vs. Load Current
FCCM



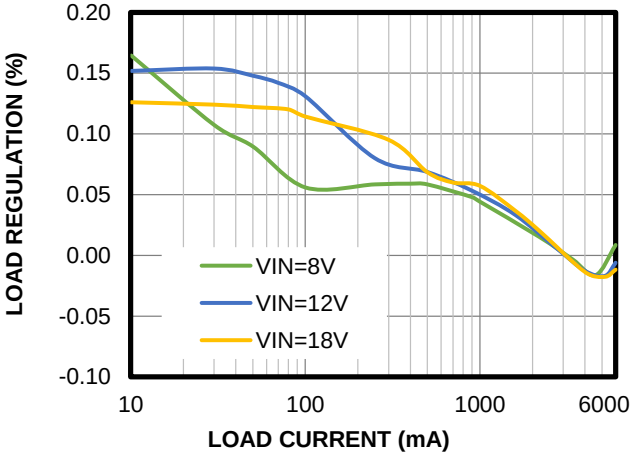
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH [9], f_{SW} = 2.2MHz, AAM, T_A = 25°C, unless otherwise noted.

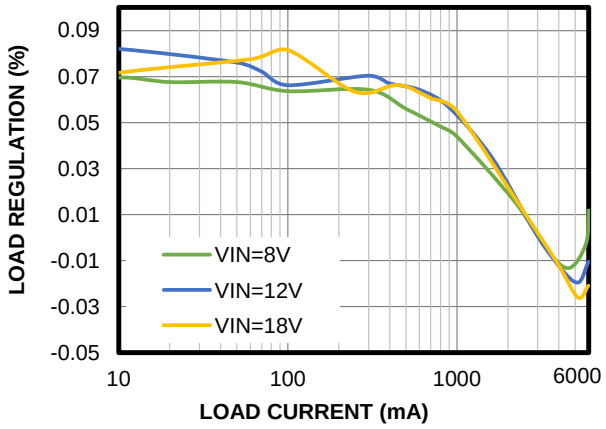
Efficiency vs. Load Current
FCCM



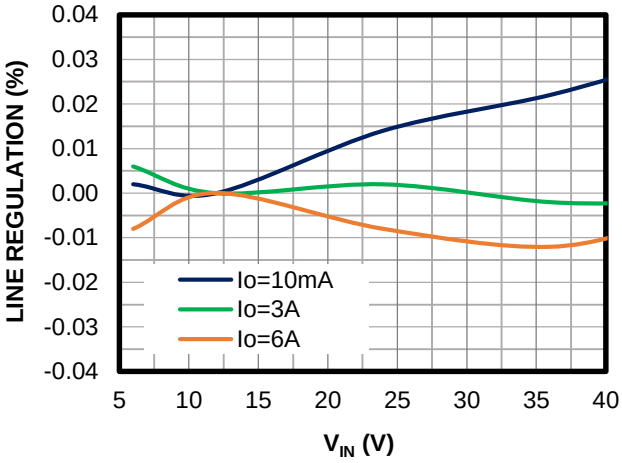
Load Regulation
AAM



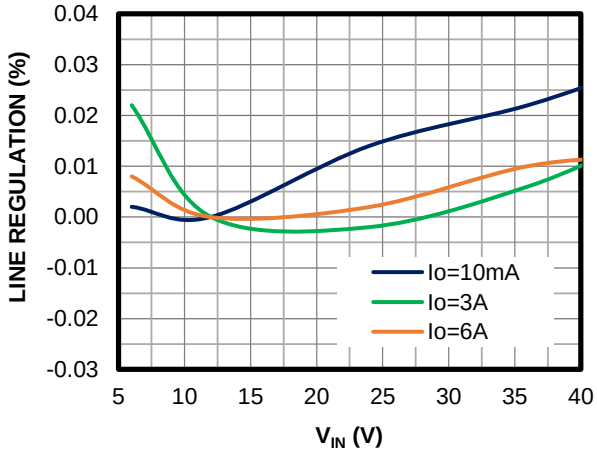
Load Regulation
FCCM



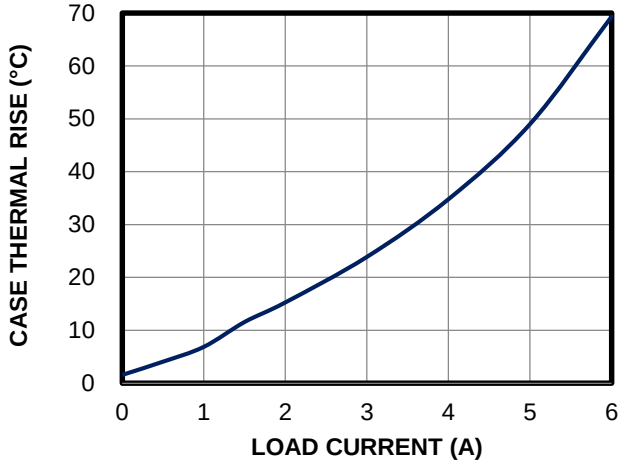
Line Regulation
AAM



Line Regulation
FCCM



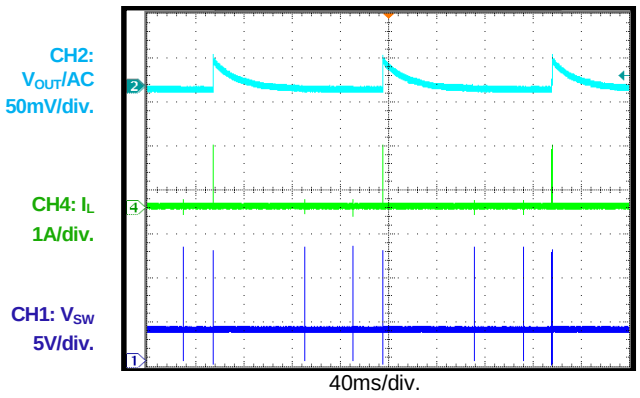
Case Thermal Rise
V_{OUT} = 5V



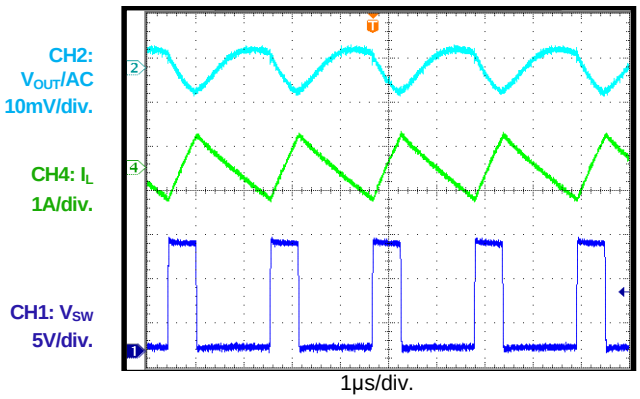
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH [8], f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

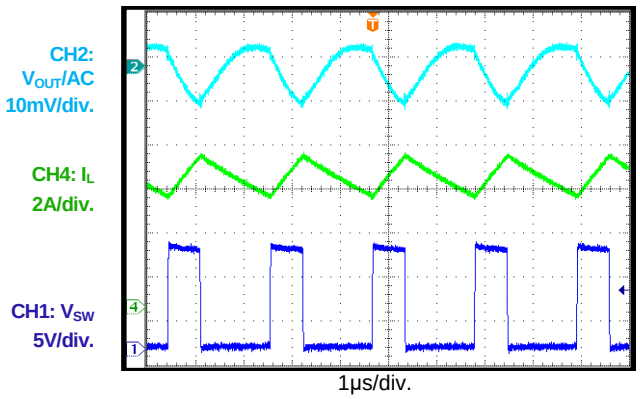
Steady State
I_{OUT} = 0A, AAM



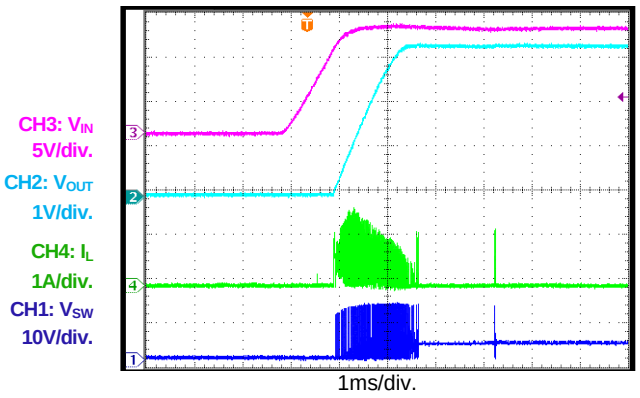
Steady State
I_{OUT} = 0A, FCCM



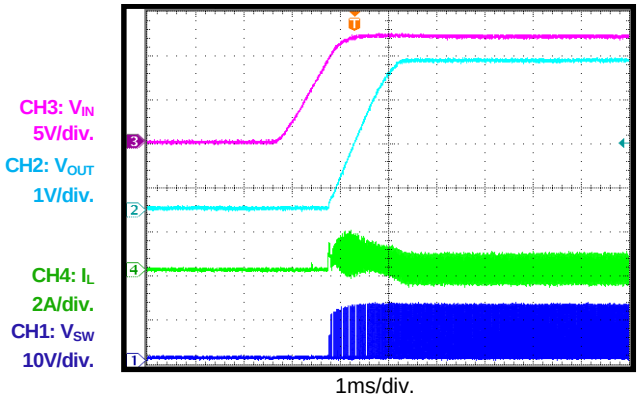
Steady State
I_{OUT} = 6A



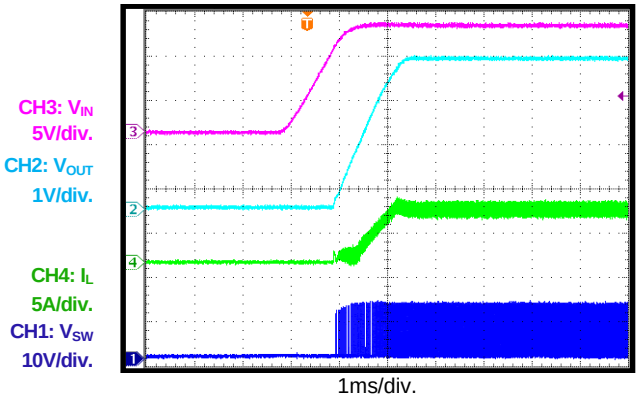
Start-up through VIN
I_{OUT} = 0A, AAM



Start-Up through VIN
I_{OUT} = 0A, FCCM



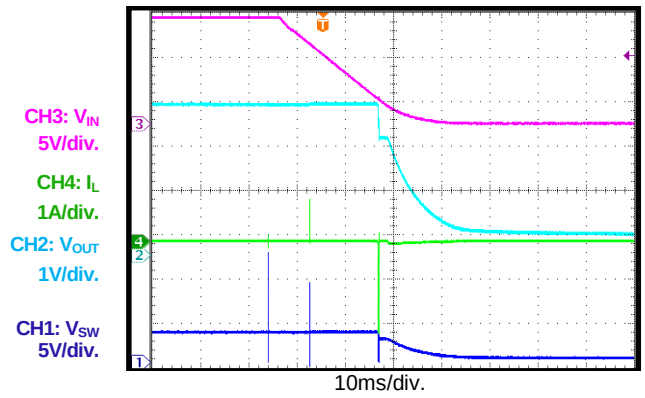
Start-Up through VIN
I_{OUT} = 6A



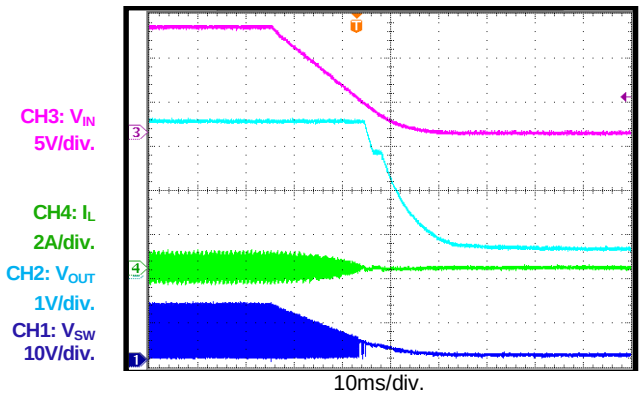
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH [8], f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

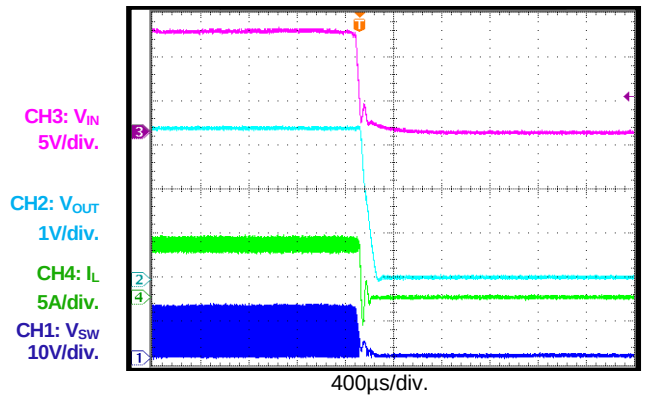
Shutdown through VIN
I_{OUT} = 0A, AAM



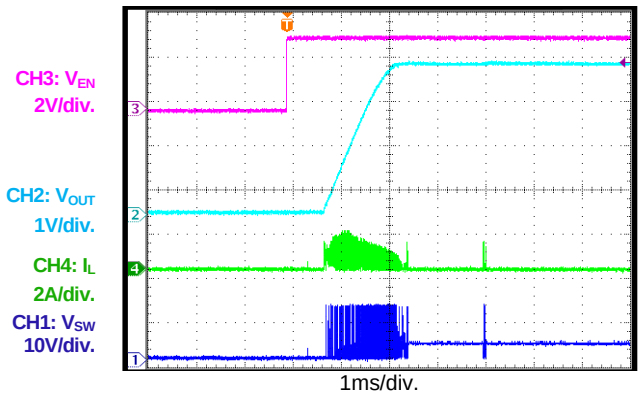
Shutdown through VIN
I_{OUT} = 0A, FCCM



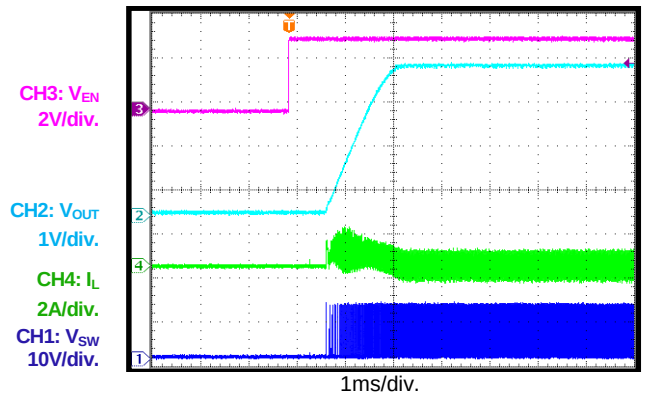
Shutdown through VIN
I_{OUT} = 6A



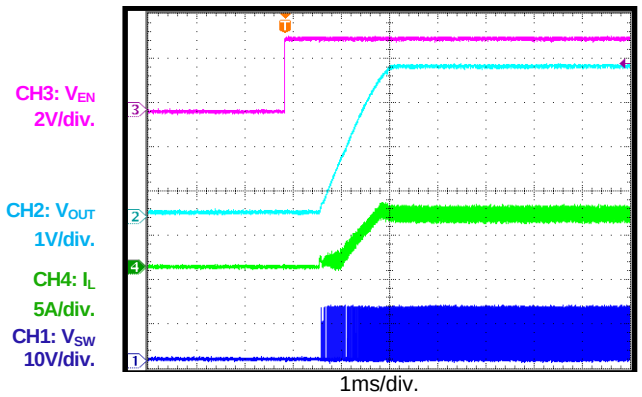
Start-Up through EN
I_{OUT} = 0A, AAM



Start-Up through EN
I_{OUT} = 0A, FCCM



Start-Up through EN
I_{OUT} = 6A

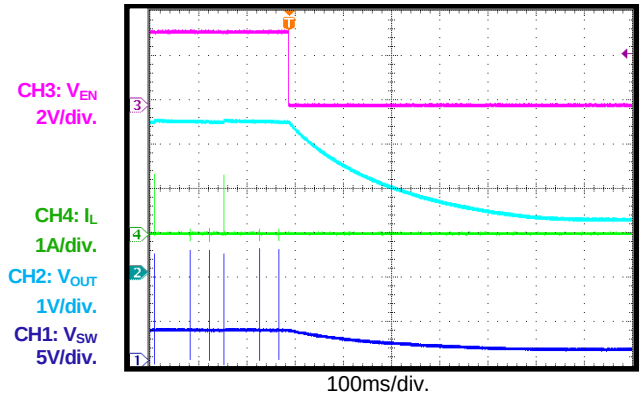


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH [8], f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

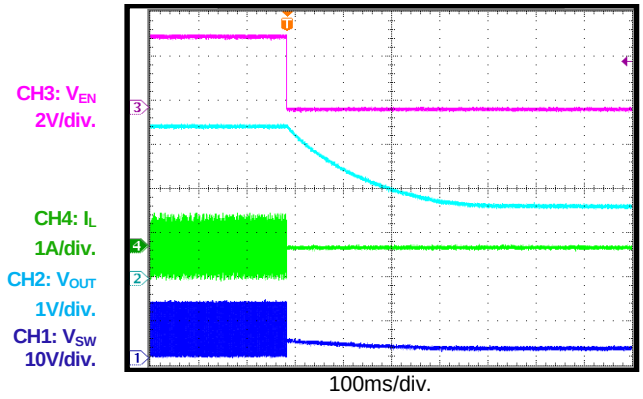
Shutdown through EN

I_{OUT} = 0A, AAM



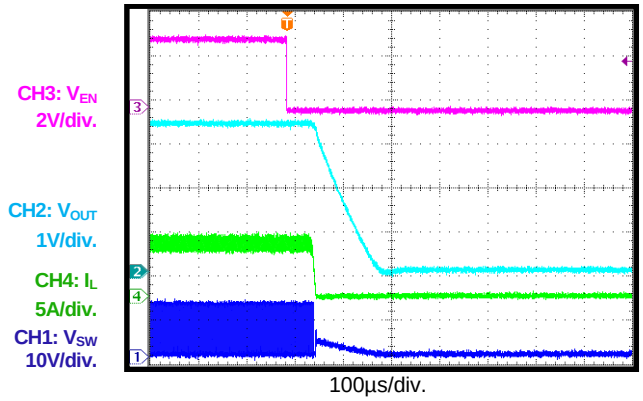
Shutdown through EN

I_{OUT} = 0A, FCCM



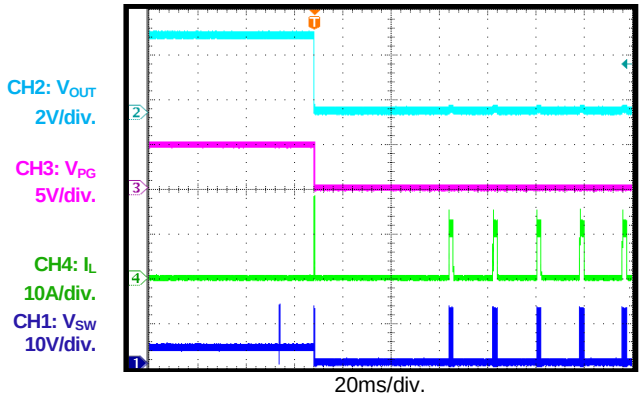
Shutdown through EN

I_{OUT} = 6A



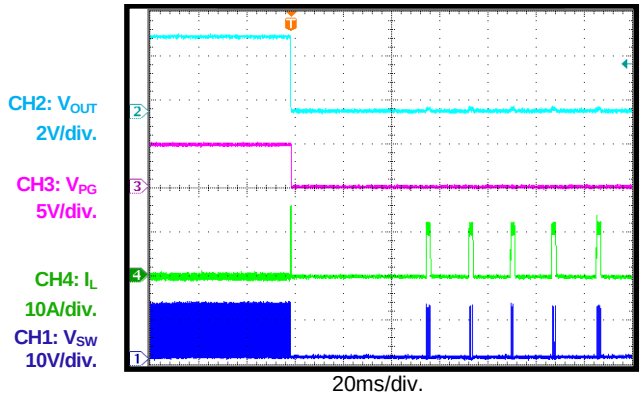
SCP Entry

I_{OUT} = 0A, AAM



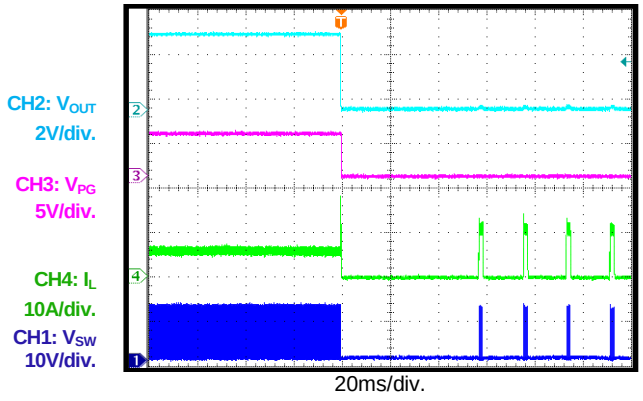
SCP Entry

I_{OUT} = 0A, FCCM



SCP Entry

I_{OUT} = 6A

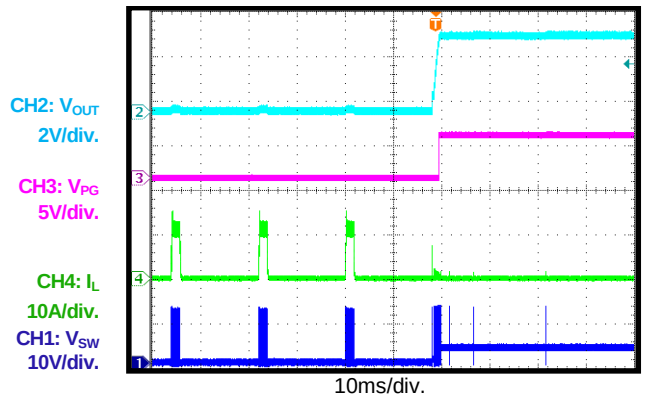


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH [8], f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

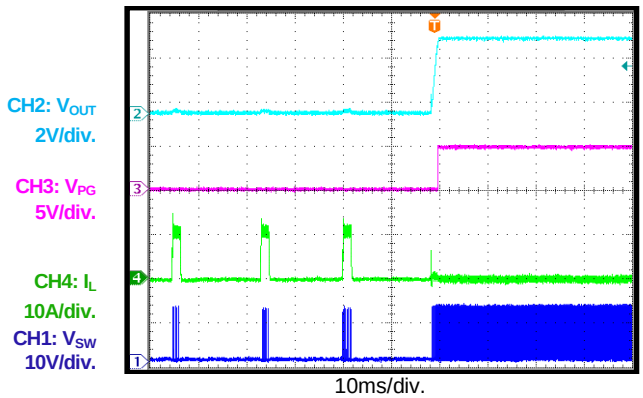
SCP Recovery

I_{OUT} = 0A, AAM



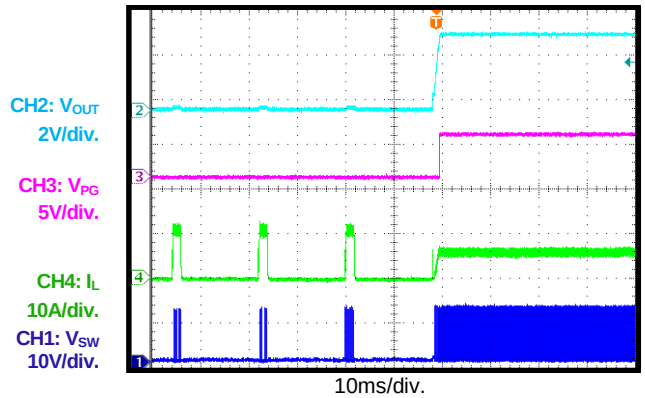
SCP Recovery

I_{OUT} = 0A, FCCM

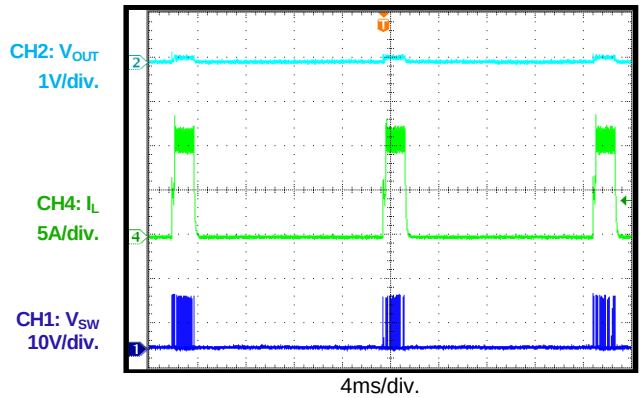


SCP Recovery

I_{OUT} = 6A

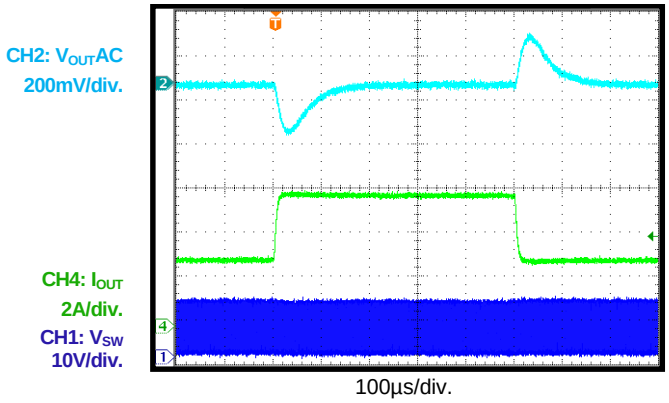


SCP Steady State



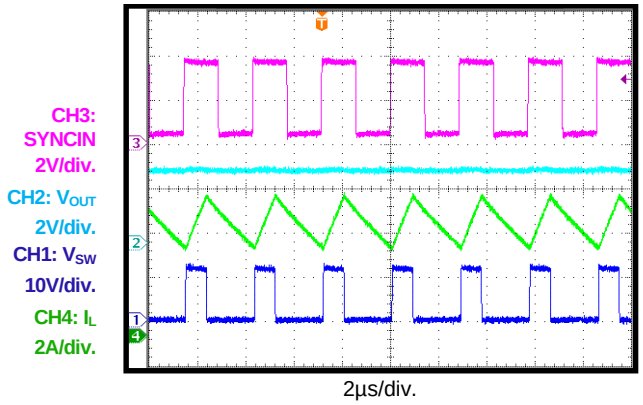
Load Transient

I_{OUT} = 3A to 6A, 1.6A/µs



SYNC Operation

I_{OUT} = 6A, SYNC frequency = 350kHz

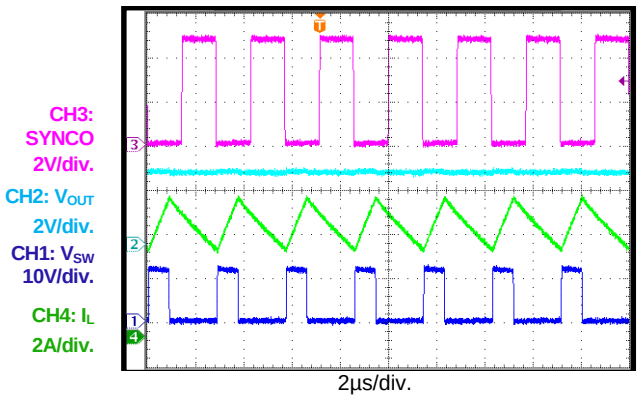


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH [8], f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

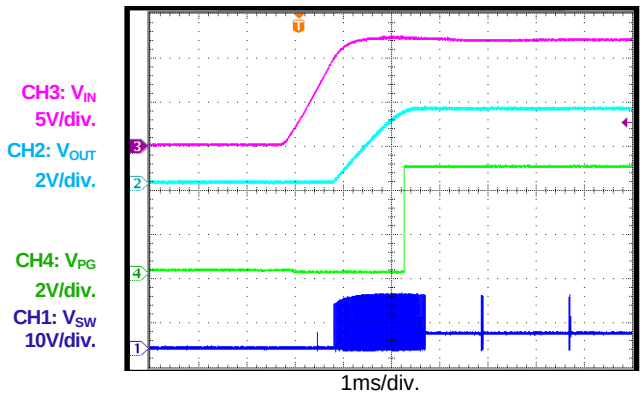
SYNCO Operation

I_{OUT} = 6A, SYNC frequency = 350kHz



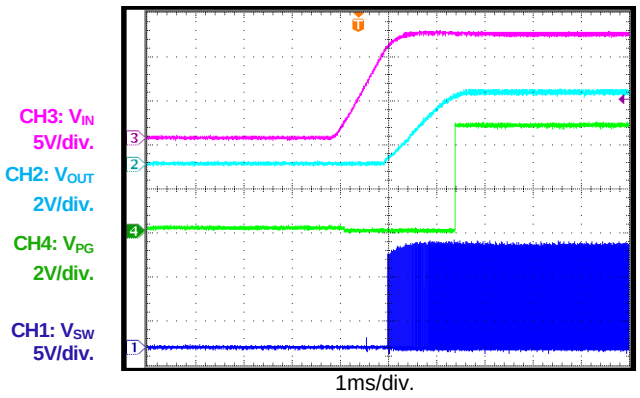
PG Start-Up through VIN

I_{OUT} = 0A



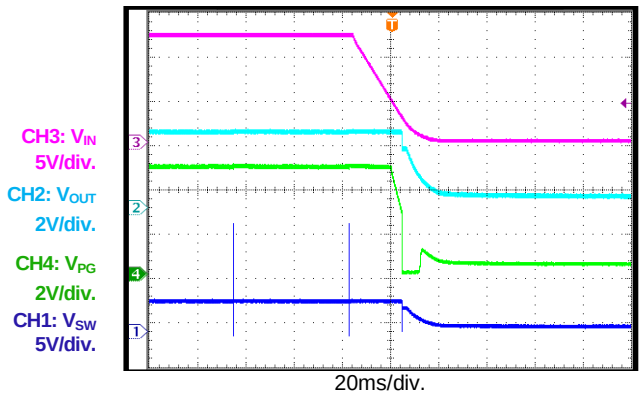
PG Start-Up through VIN

I_{OUT} = 6A



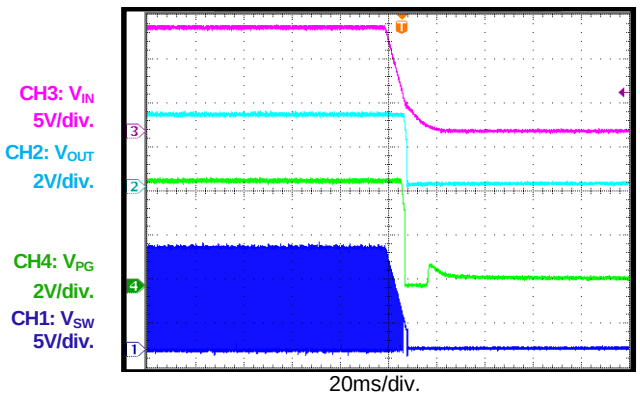
PG Shutdown through VIN

I_{OUT} = 0A



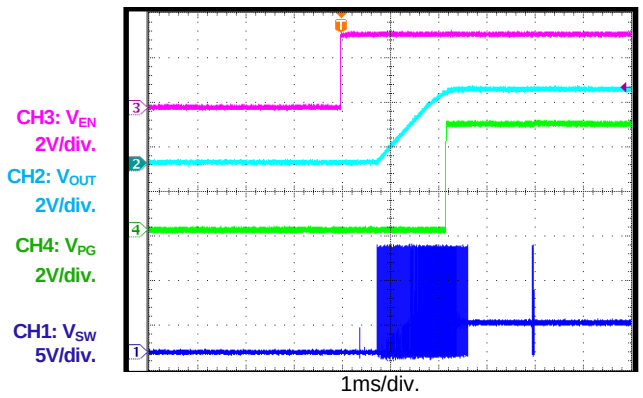
PG Shutdown through VIN

I_{OUT} = 6A



PG Start-Up through EN

I_{OUT} = 0A

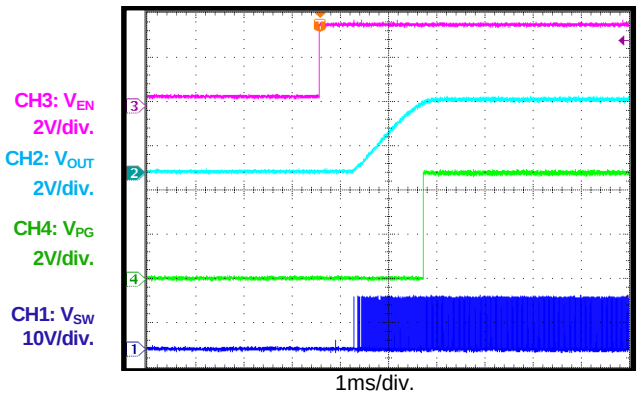


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH [8], f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

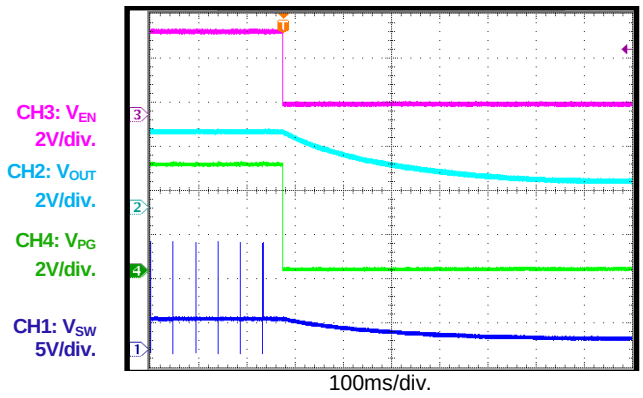
PG Start-up through EN

I_{OUT} = 6A



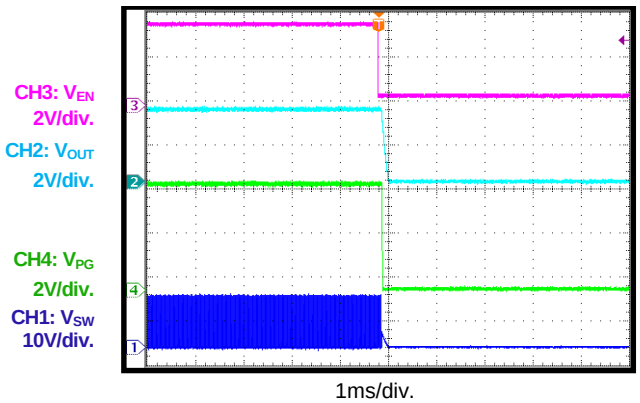
PG Shutdown through EN

I_{OUT} = 0A



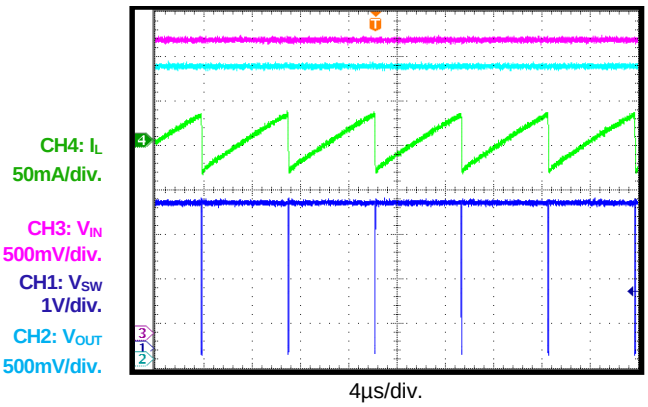
PG Shutdown through EN

I_{OUT} = 6A



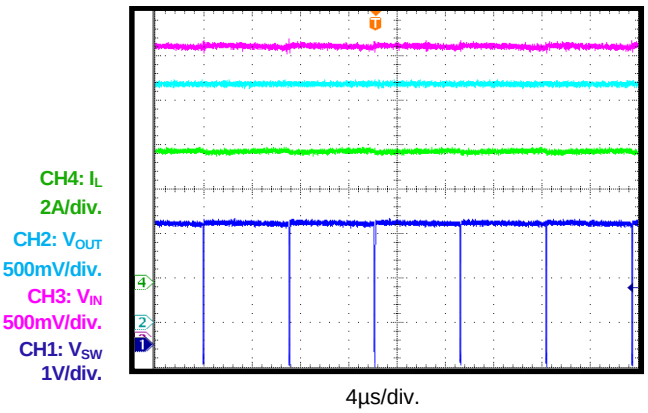
Dropout Operation

V_{IN} = 3.3V, V_{OUT} set to 3.3V, I_{OUT} = 0A



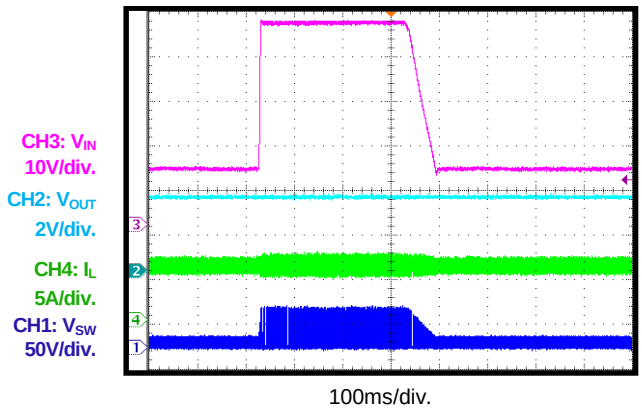
Dropout Operation

V_{IN} = 3.3V, V_{OUT} set to 3.3V, I_{OUT} = 6A



Load Dump

V_{IN} = 12V to 36V, I_{OUT} = 6A

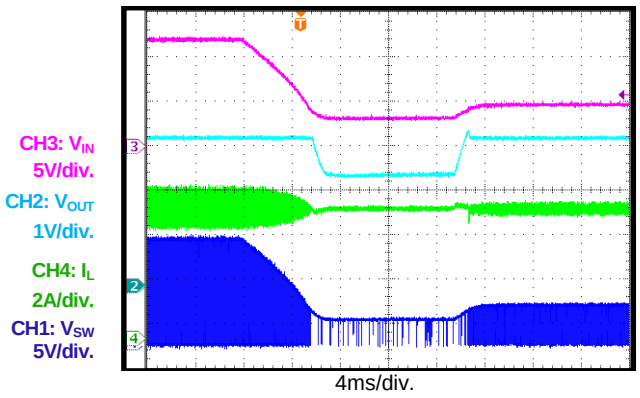


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH (8), f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

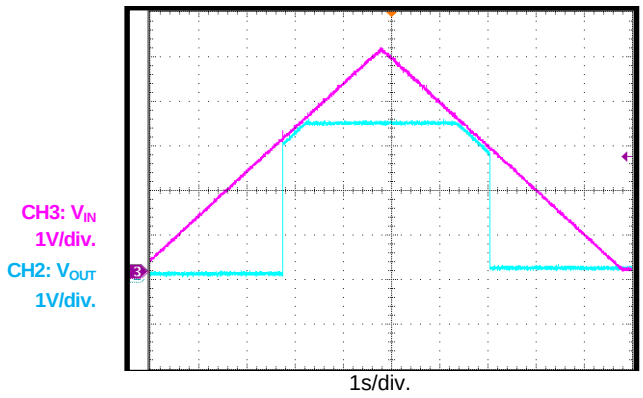
Cold Crank

V_{IN} = 12V to 3.3V to 5V, I_{OUT} = 6A



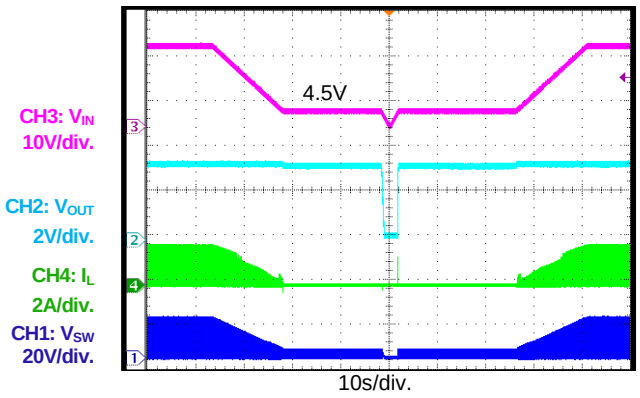
VIN Ramp Up and Down

I_{OUT} = 0.1A



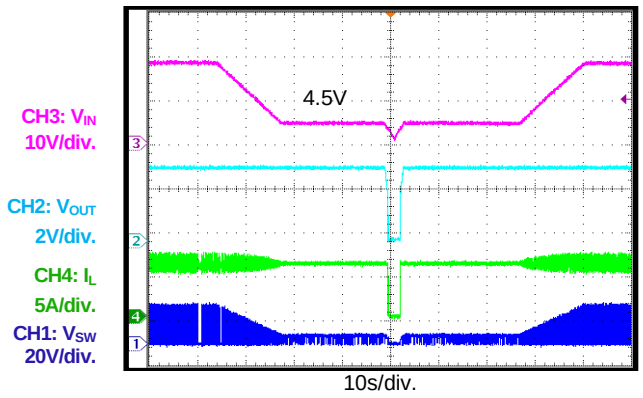
VIN Ramp Down and Up

I_{OUT} = 1mA



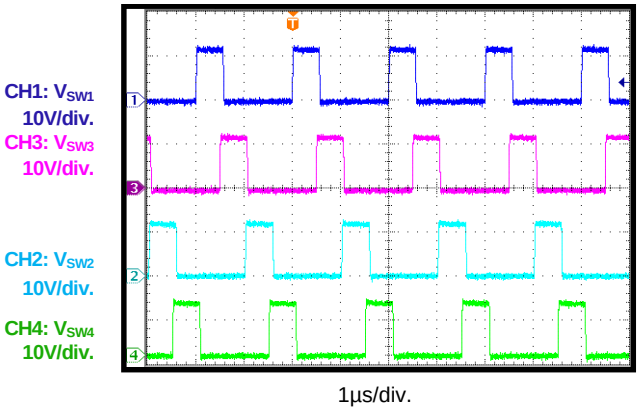
VIN Ramp Down and Up

I_{OUT} = 6A



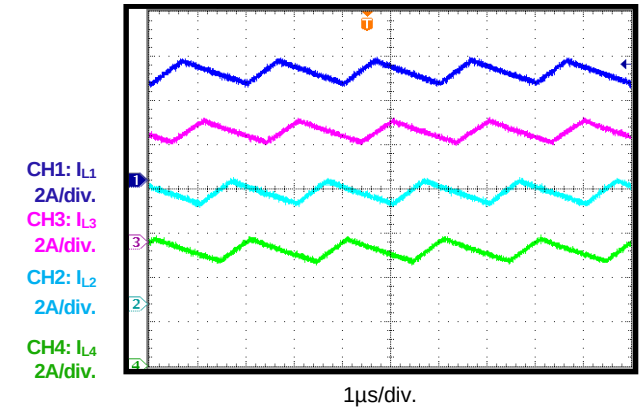
Steady State

V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 20A, 4-phase



Steady State

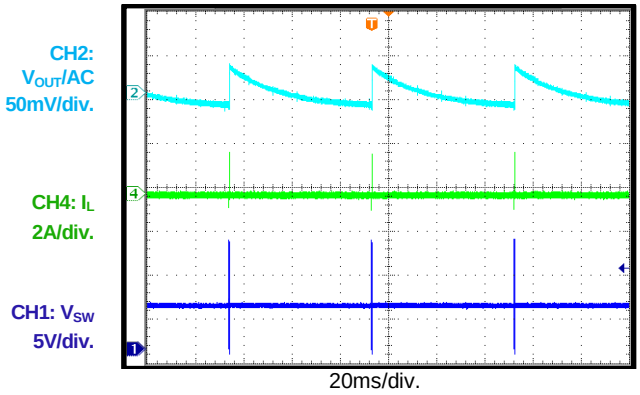
V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 20A, 4-phase



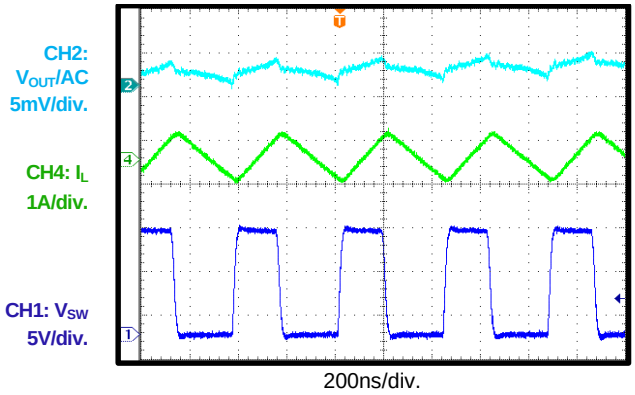
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH (9), f_{SW} = 2.2MHz, AAM, T_A = 25°C, unless otherwise noted.

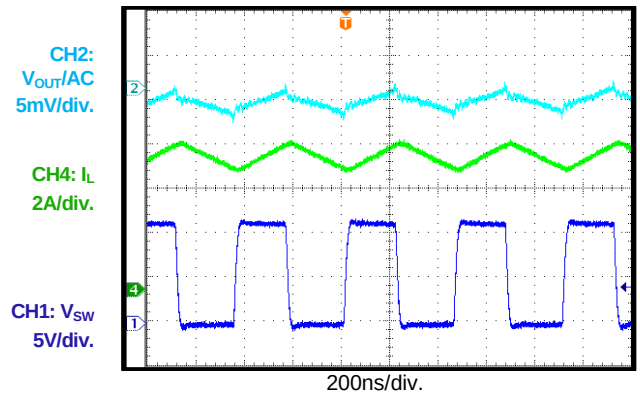
Steady State
I_{OUT} = 0A, AAM



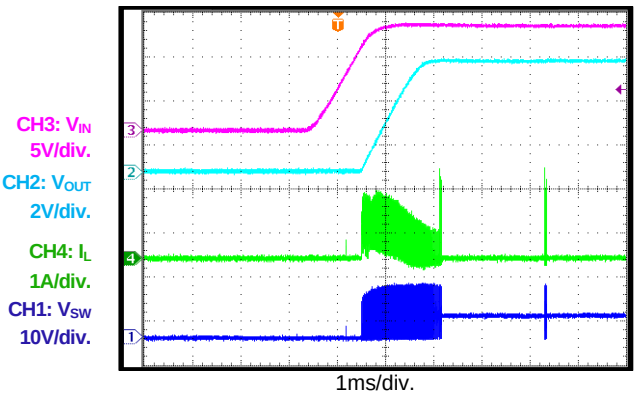
Steady State
I_{OUT} = 0A, FCCM



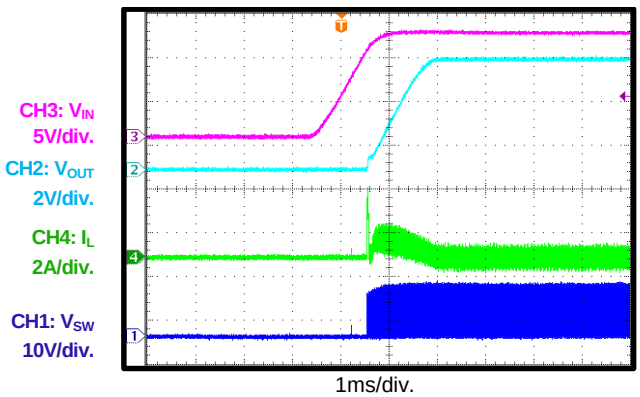
Steady State
I_{OUT} = 6A



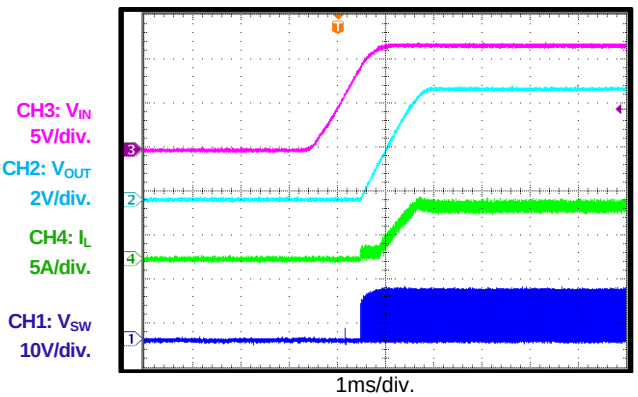
Start-Up through VIN
I_{OUT} = 0A, AAM



Start-Up through VIN
I_{OUT} = 0A, FCCM



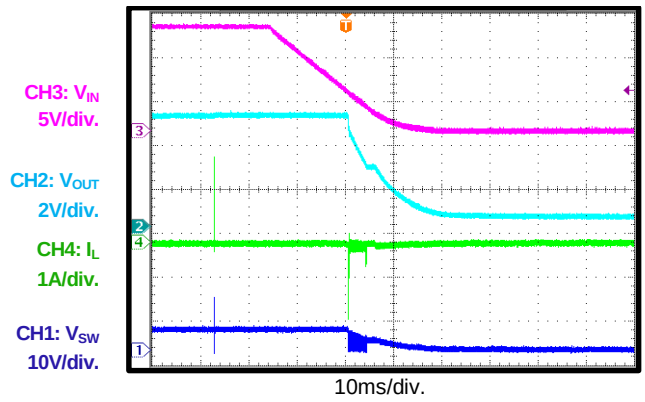
Start-Up through VIN
I_{OUT} = 6A



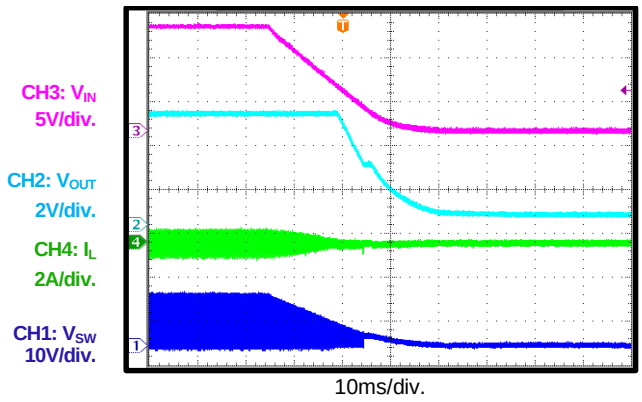
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH (9), f_{SW} = 2.2MHz, AAM, T_A = 25°C, unless otherwise noted.

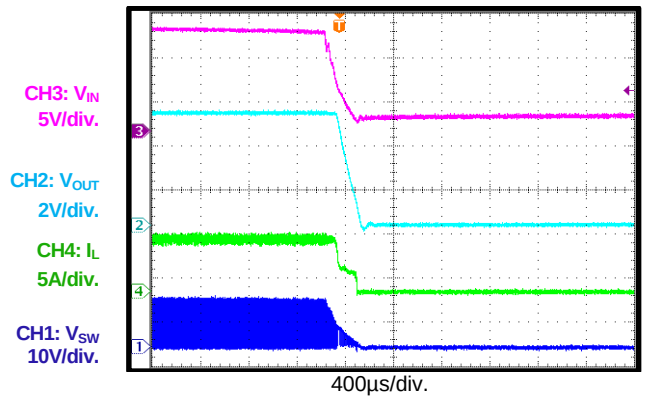
Shutdown through VIN
I_{OUT} = 0A, AAM



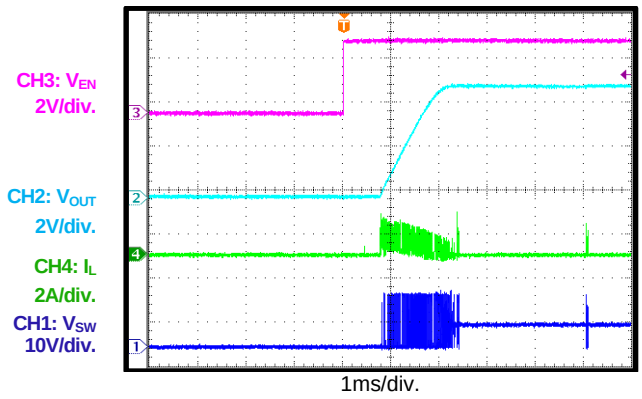
Shutdown through VIN
I_{OUT} = 0A, FCCM



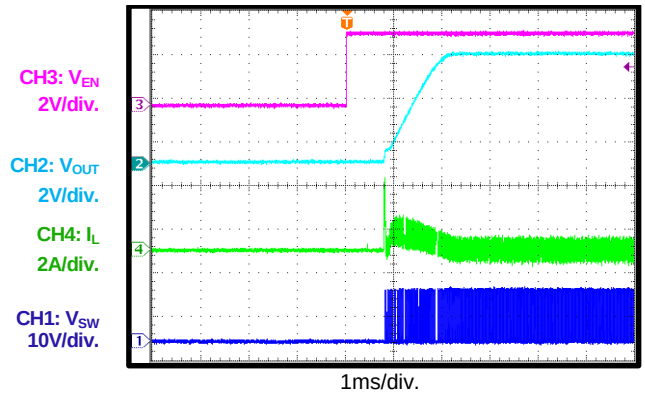
Shutdown through VIN
I_{OUT} = 6A



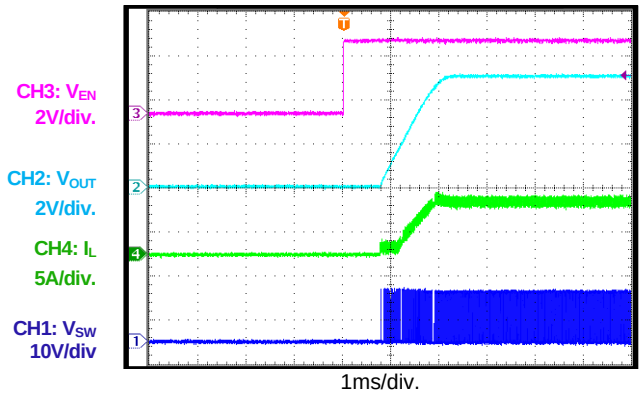
Start-Up through EN
I_{OUT} = 0A, AAM



Start-Up through EN
I_{OUT} = 0A, FCCM



Start-Up through EN
I_{OUT} = 6A

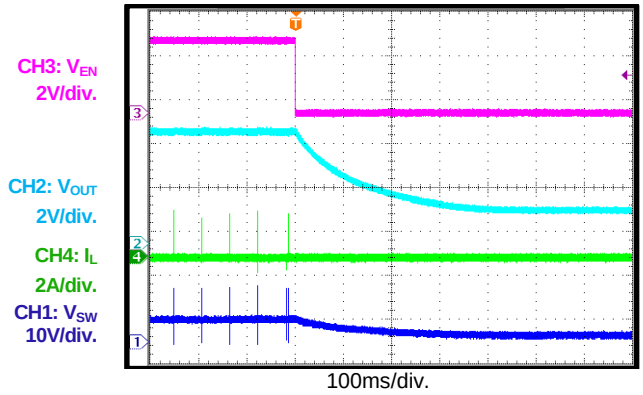


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH [9], f_{SW} = 2.2MHz, AAM, T_A = 25°C, unless otherwise noted.

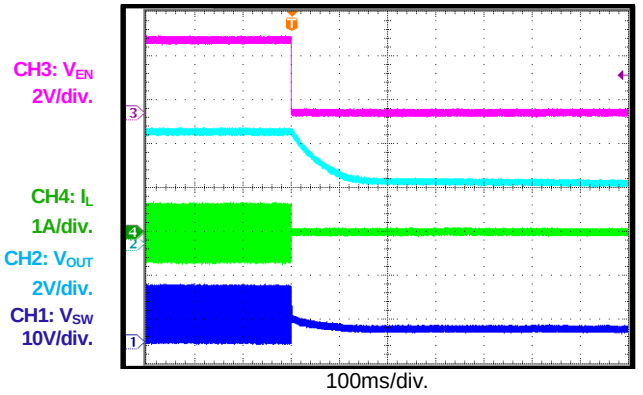
Shutdown through EN

I_{OUT} = 0A, AAM



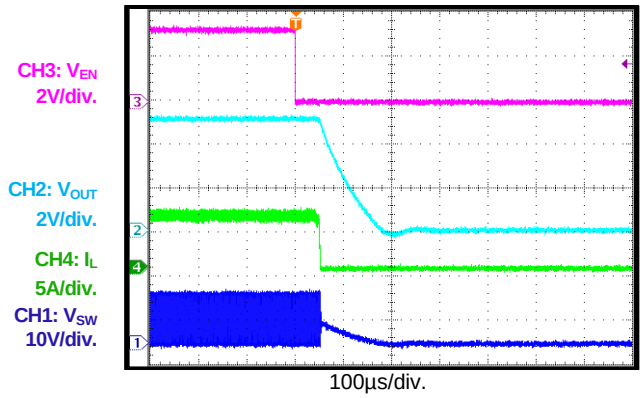
Shutdown through EN

I_{OUT} = 0A, FCCM



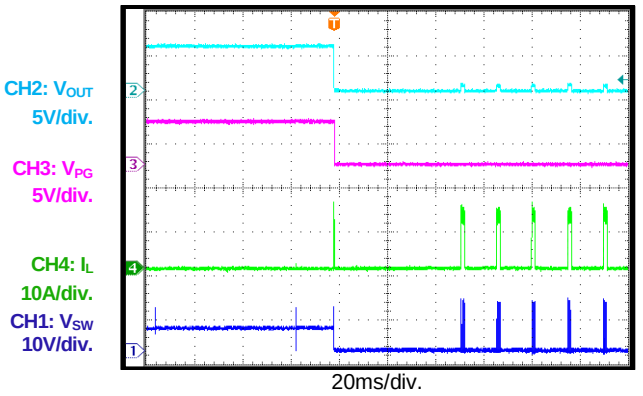
Shutdown through EN

I_{OUT} = 6A



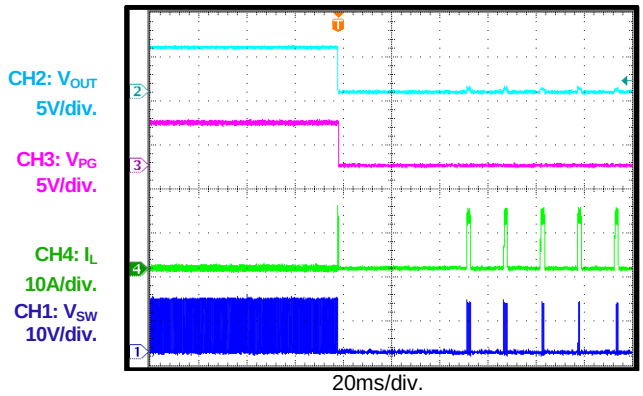
SCP Entry

I_{OUT} = 0A, AAM



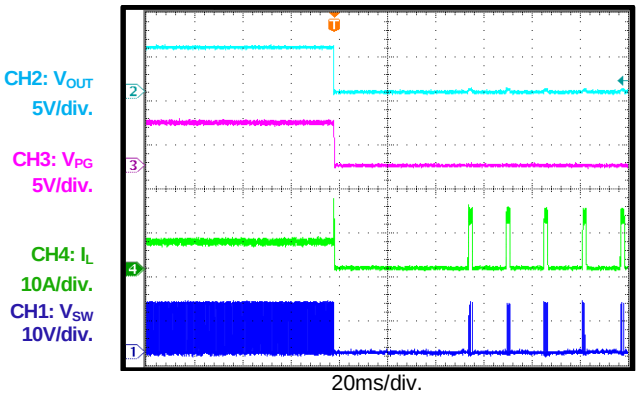
SCP Entry

I_{OUT} = 0A, FCCM



SCP Entry

I_{OUT} = 6A

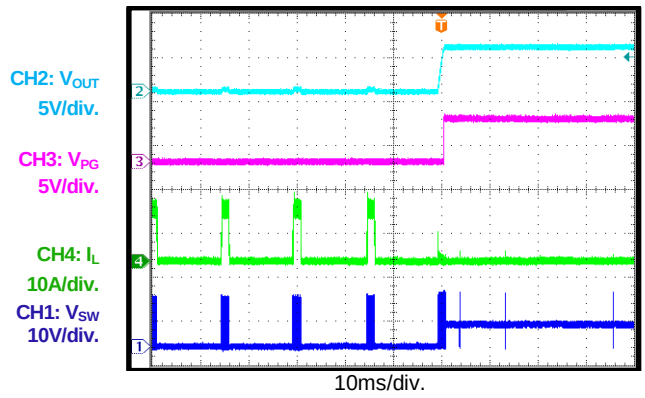


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH [9], f_{SW} = 2.2MHz, AAM, T_A = 25°C, unless otherwise noted.

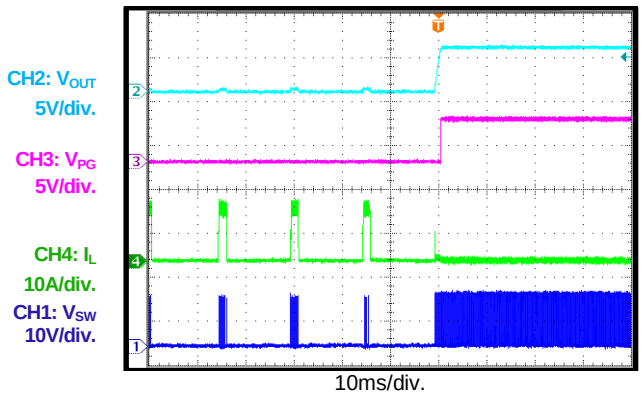
SCP Recovery

I_{OUT} = 0A, AAM



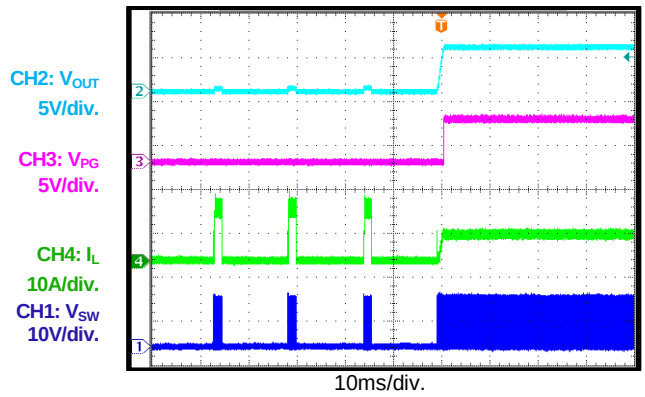
SCP Recovery

I_{OUT} = 0A, FCCM

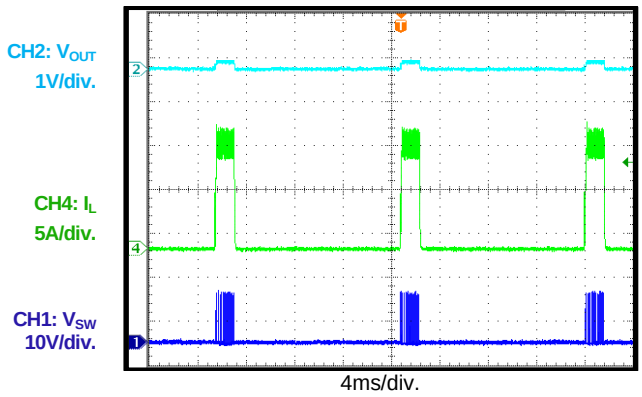


SCP Recovery

I_{OUT} = 6A

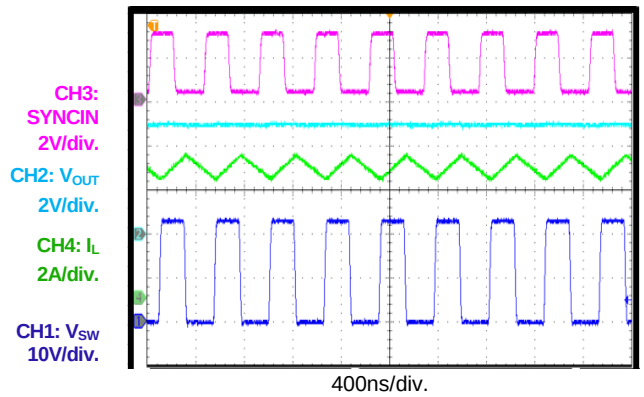


SCP Steady State



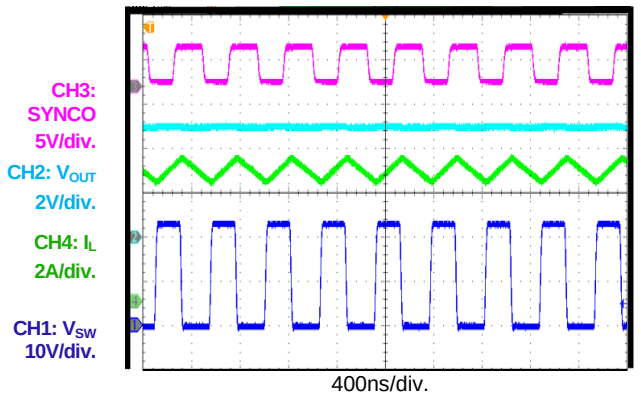
SYNC Operation

I_{OUT} = 6A, SYNC frequency = 2.2MHz



SYNCO Operation

I_{OUT} = 6A, SYNC frequency = 2.2MHz

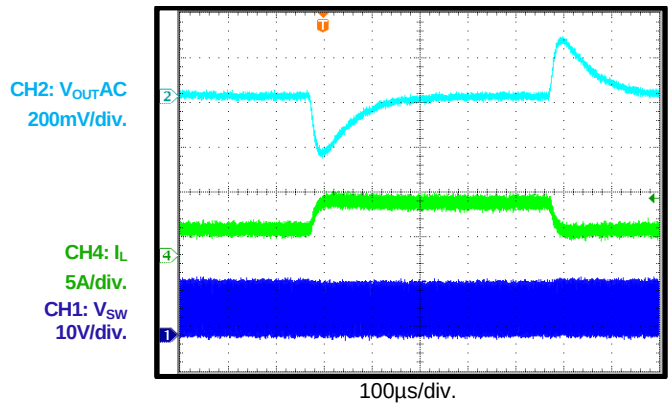


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH [9], f_{SW} = 2.2MHz, AAM, T_A = 25°C, unless otherwise noted.

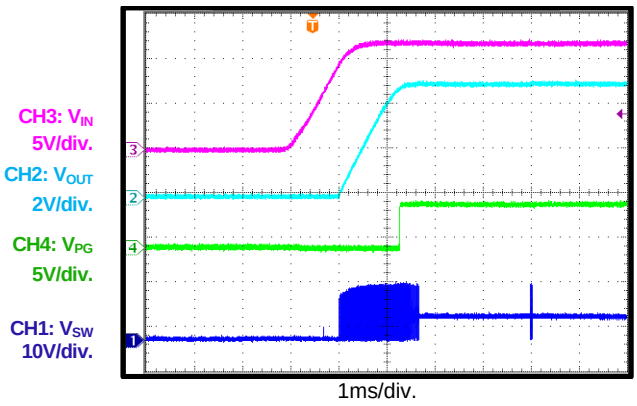
Load Transient

I_{OUT} = 3A to 6A, 1.6A/µs



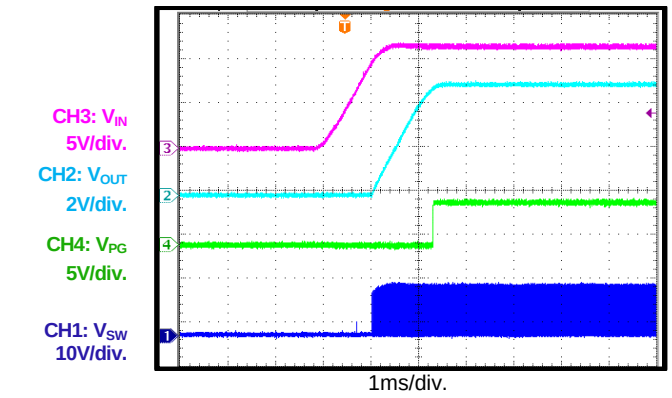
PG Start-Up through VIN

I_{OUT} = 0A, AAM



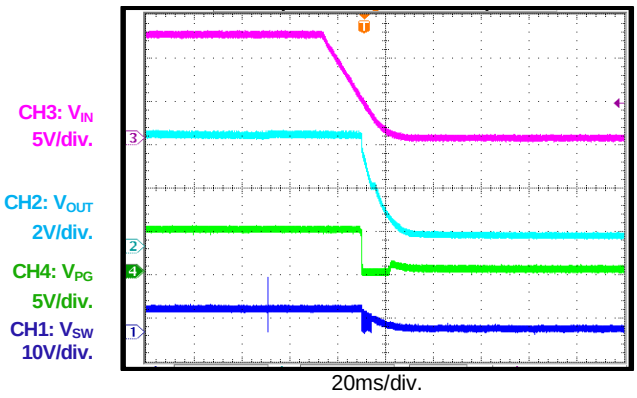
PG Start-Up through VIN

I_{OUT} = 6A



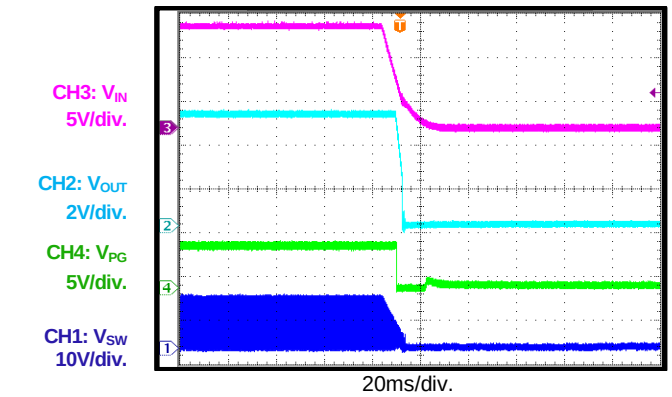
PG Shutdown through VIN

I_{OUT} = 0A, AAM



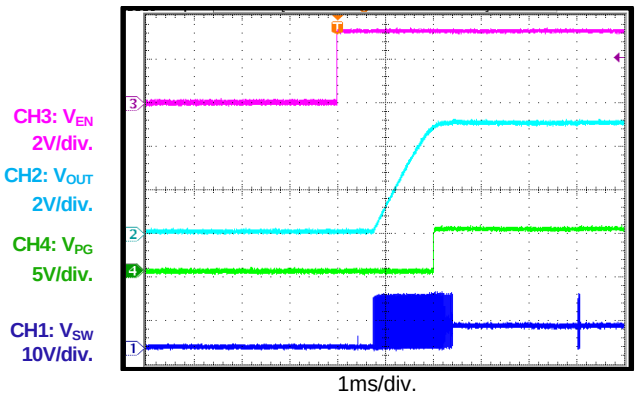
PG Shutdown through VIN

I_{OUT} = 6A



PG Start-Up through EN

I_{OUT} = 0A

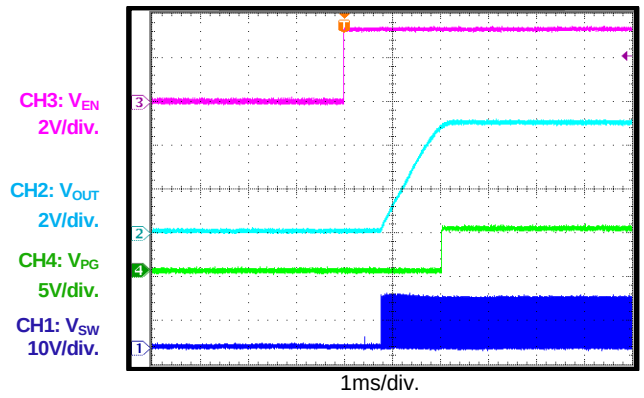


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH [9], f_{SW} = 2.2MHz, AAM, T_A = 25°C, unless otherwise noted.

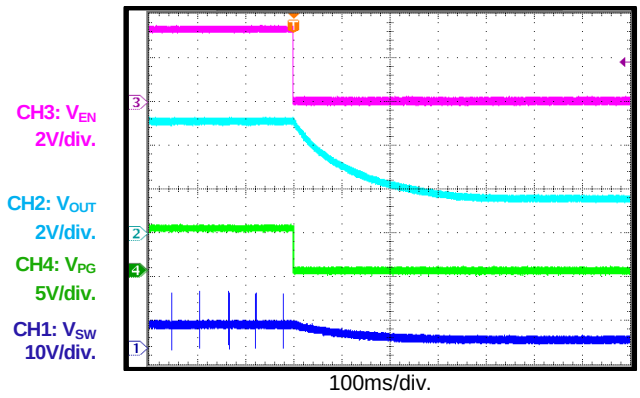
PG Start-Up through EN

I_{OUT} = 6A



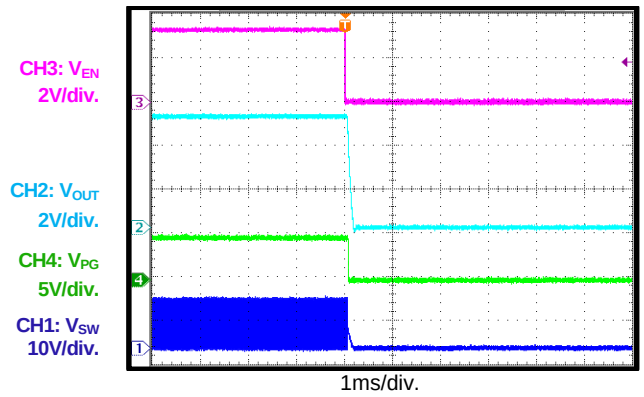
PG Shutdown through EN

I_{OUT} = 0A



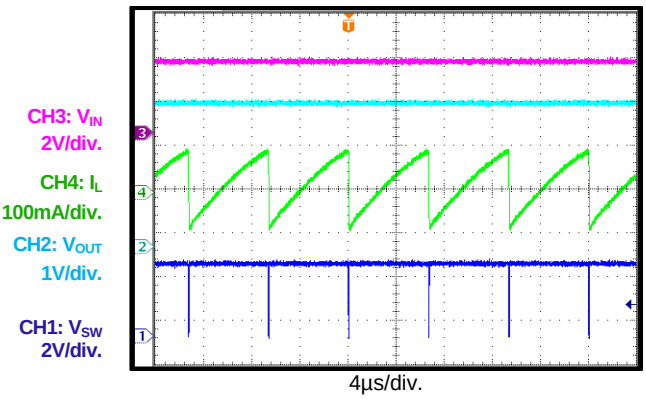
PG Shutdown through EN

I_{OUT} = 6A



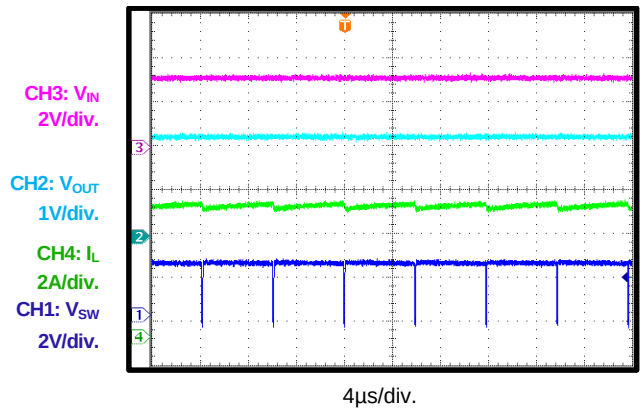
Dropout Operation

V_{IN} = 3.3V, V_{OUT} set to 5V, I_{OUT} = 0A



Dropout Operation

V_{IN} = 3.3V, V_{OUT} set to 5V, I_{OUT} = 6A



Notes:

8) Inductor part number: XAL6060-472MEC. DCR = 15mΩ.
9) Inductor part number: XAL5030-102MEB. DCR = 8.5mΩ.

FUNCTIONAL BLOCK DIAGRAM

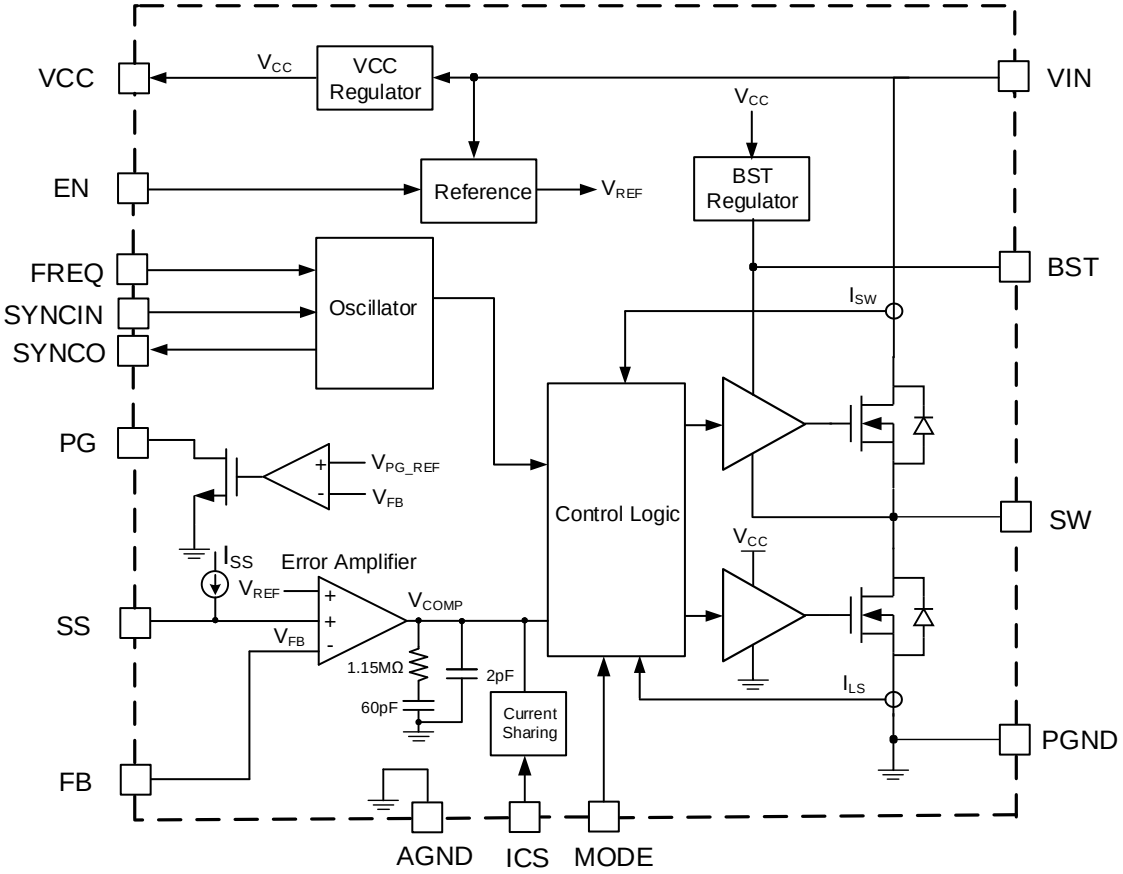


Figure 1: Functional Block Diagram

Timing Sequence

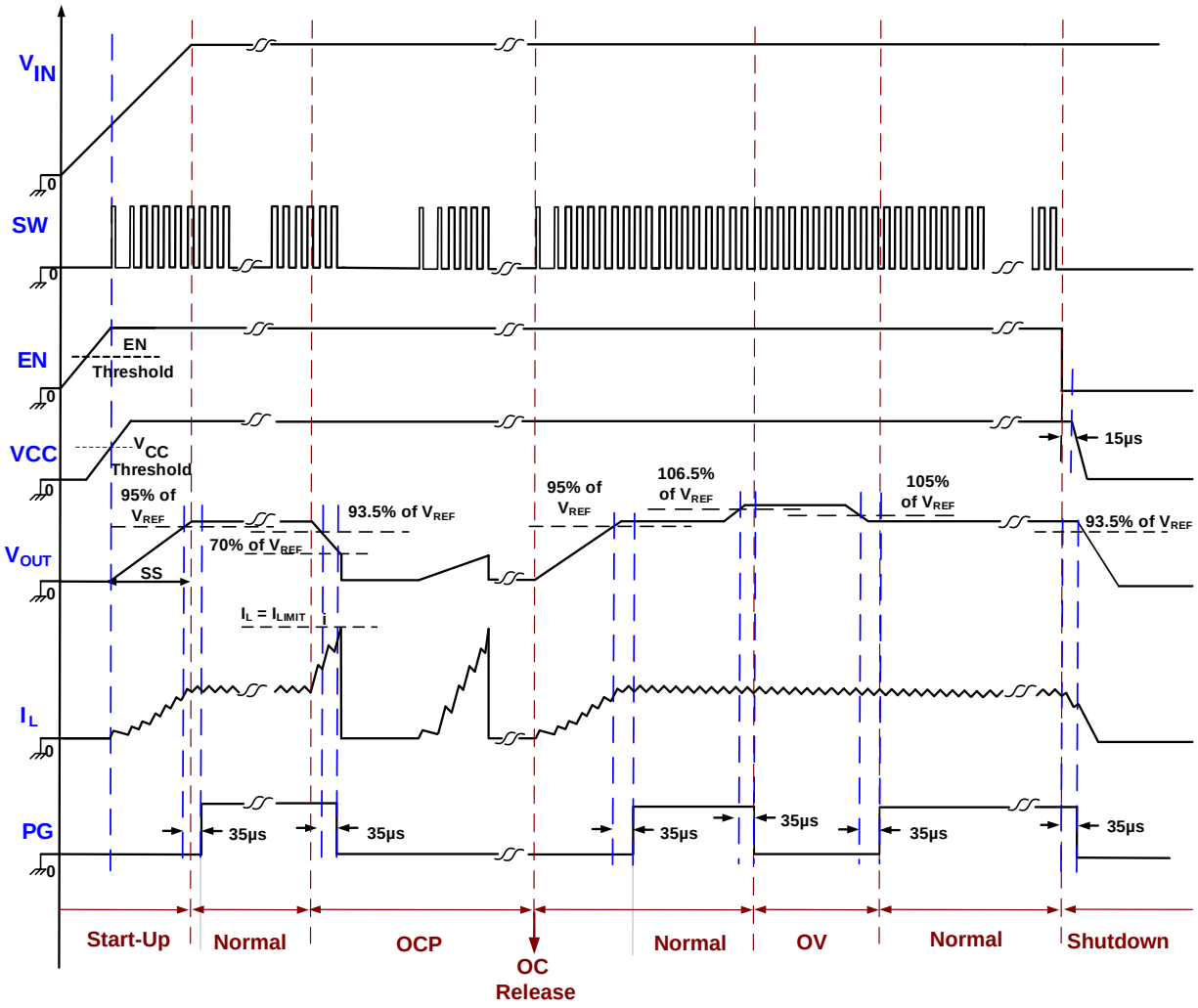


Figure 2: Timing Sequence

OPERATION

The MPQ4360 is a synchronous, step-down switching converter with integrated, internal high-side and low-side power MOSFETs. It provides 6A of highly efficient output with current mode control.

The device features a wide input voltage range, configurable switching frequency, external soft start, and precision current limiting. Its low operational quiescent current makes it well-suited for battery-powered applications.

PWM Control

At moderate to high output currents, the MPQ4360 operates in fixed-frequency, peak current control mode to regulate the output voltage. A PWM cycle is initiated by the internal clock. At the rising edge of the clock, the high-side MOSFET (HS-FET) turns on and remains on until its current reaches the value set by the internal COMP voltage (V_{COMP}). Once the HS-FET is on, it remains on for at least 100ns.

When the HS-FET is off, the low-side MOSFET (LS-FET) turns on immediately and remains on until the next cycle starts. Once the LS-FET is on, it remains on for at least 80ns before the next cycle starts.

If the current in the HS-FET does not reach the value set by COMP in one PWM period, the HS-FET remains on, saving a turn-off operation. The HS-FET is forced off if the on time lasts about 10µs, even if the COMP value is not reached.

Light-Load Operation

Under light-load conditions, the MPQ4360 can be forced to operate in two different operation modes via the MODE pin.

The MPQ4360 works in forced continuous conduction mode (FCCM) when the MODE pin is pulled above 1.8V. The part works with fixed frequency from no-load to full-load conditions in FCCM. FCCM provides a controllable frequency and lower output ripple at light loads.

The MPQ4360 works in advanced asynchronous modulation (AAM) mode when MODE is pulled below 0.4V. AAM optimizes efficiency during light-load and no-load conditions.

When AAM is enabled, the MPQ4360 first enters non-synchronous operation as long as the inductor current approaches zero under light loads. If the load is further decreased or there is no load, and V_{COMP} drops to the set value, the MPQ4360 enters AAM. In AAM, the internal clock is reset every time V_{COMP} crosses over the set value. The crossover time is used as the benchmark for the next clock. When the load increases and V_{COMP} exceeds the set value, the operation mode is discontinuous conduction mode (DCM) or FCCM, which both have a constant switching frequency (see Figure 3).

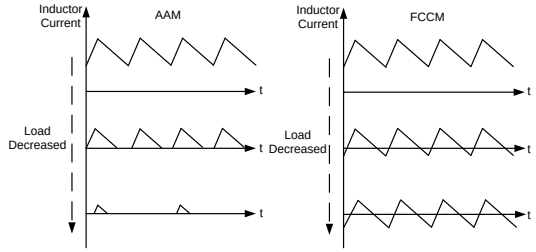


Figure 3: AAM and FCCM

Error Amplifier

The error amplifier compares the FB pin voltage to the internal reference (0.815V), and outputs a current that is proportional to the difference between the two. This output current is then used to charge the compensation network to form V_{COMP}, which is used to control the power MOSFET current.

During operation, the minimum V_{COMP} is clamped to 0.9V, and the maximum is clamped to 2.0V. COMP is internally pulled down to GND in shutdown mode.

Internal Regulator VCC

Most of the internal circuitry is powered by the internal 4.9V VCC regulator. This regulator takes VIN as the input and operates in the full V_{IN} range. When V_{IN} exceeds 4.9V, VCC is in full regulation. When V_{IN} is below 4.9V, the output VCC degrades.

Bootstrap Charging

The bootstrap capacitor is charged and regulated to about 5V by the dedicated internal bootstrap regulator. When the voltage between the BST and SW nodes is below the regulated value, a P-channel MOSFET pass transistor connected from VCC to BST turns on to charge the bootstrap capacitor.

External circuitry should provide sufficient voltage headroom to facilitate the charging. When the HS-FET is on, BST is above VCC, so the bootstrap capacitor cannot be charged.

Under higher duty cycle operation, the bootstrap has less time to charge, so the bootstrap capacitor may not be charged sufficiently. If the external circuit does not have a sufficient voltage and time to charge the bootstrap capacitor, use additional, external circuitry to ensure that the bootstrap voltage is in the normal operation range.

Low-Dropout Operation and BST Refresh

To improve dropout, the MPQ4360 is designed to operate at close to 100% duty cycle as long as the BST-to-SW voltage exceeds 2.5V. When the voltage from BST to SW drops below 2.5V, the HS-FET turns off using an under-voltage lockout (UVLO) circuit, which allows the LS-FET to conduct and refresh the charge on the BST capacitor. In DCM or power-save mode (PSM), the LS-FET is forced on to refresh the BST voltage.

Since the supply current sourced from the BST capacitor is low, the HS-FET remains on for more switching cycles than are required to refresh the capacitor. Therefore, the effective duty cycle of the switching regulator is high.

The effective duty cycle during regulator dropout is mainly influenced by the voltage drops across the power MOSFET, the inductor resistance, the low-side diode, and PCB resistance.

Enable (EN) Control

The EN pin is a digital control pin that turns the regulator on and off (see Figure 4). The EN pin provides two main features.

Enabled by External Logic H/L Signal

When EN is pulled below its falling threshold (0.85V), the chip is put into the lowest shutdown current mode. Forcing EN above its rising threshold (1V) turns the MPQ4360 on.

Configurable V_{IN} Under-Voltage Lockout (UVLO)

When V_{IN} is sufficiently high, the chip can be enabled and disabled via the EN pin. With the internal current source, this circuit can generate a configurable V_{IN} UVLO and hysteresis.

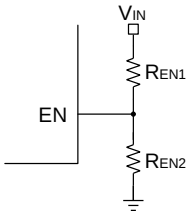


Figure 4: Enable Divider Circuit

Configurable Frequency and Foldback

The MPQ4360 oscillating frequency is configured either by an external resistor (R_{FREQ}) connected from the FREQ pin to ground, or by a logic level SYNC signal. To select the switching frequency (f_{SW}), select the R_{FREQ} value following the f_{SW} vs. R_{FREQ} curve in the Typical Performance Characteristics section on page 15.

Note that f_{SW} will foldback at high input voltages to avoid triggering the minimum on time and forcing V_{OUT} out of regulation. Frequency foldback is disabled when there is an external sync clock. The f_{SW} vs. V_{IN} curve on page 15 shows an example when R_{FREQ} is 12kΩ. The MPQ4360 can support switching frequencies up to 2.2MHz, unless V_{OUT} is below 5V.

For applications where V_{OUT} is below 5V, the minimum on time is triggered at high input voltages, and V_{OUT} goes out of regulation, which should be avoided.

To avoid this, it is recommended for f_{SW} to be between 350kHz to 1000kHz for car battery applications. Higher frequencies are supported for applications that do not have critical limits on the switching frequency, or for applications with relatively low, stable input voltages. Table 1 lists recommended R_{FREQ} values for common frequencies.

Table 1: Resistor Selection for Frequency

R_{FREQ} (kΩ)	f_{SW} (kHz)
86.6	350
75	410
62	470
54.9	530
45.3	640
37.4	760
34	830
26.1	1000
20	1300
15	1750
12	2200

Soft Start (SS)

Soft start (SS) is implemented to prevent the converter output voltage from overshooting during start-up.

When the soft-start period starts, an internal current source begins charging the external soft-start capacitor. When the soft-start voltage (V_{SS}) is below the internal reference voltage (V_{REF}), V_{SS} overrides V_{REF} so the error amplifier uses V_{SS} as the reference. When V_{SS} exceeds V_{REF}, V_{REF} regains control. C_{SS} can be calculated with Equation (1):

$$C_{SS}(nF) = \frac{t_{SS}(ms) \times I_{SS}(\mu A)}{V_{REF}(V)} = 6.25 \times t_{SS}(ms) \quad (1)$$

The SS pins can be used for tracking and sequencing.

Pre-Biased Start-Up

If $V_{FB} > V_{SS}$ - 150mV at start-up (which means the output has a pre-biased voltage), neither the HS-FET nor LS-FET turn on until V_{SS} exceeds V_{FB}.

Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from thermal runaway. When the silicon die temperature exceeds its upper threshold, the device shuts down the power MOSFETs. When the temperature falls below its lower threshold, the chip is enabled again.

Current Comparator and Current Limit

The power MOSFET current is accurately sensed via a current-sense MOSFET. It is then fed to the high-speed current comparator for current mode control. The current comparator takes this sensed current as one of its inputs.

When the HS-FET turns on, the comparator is blanked until the end of the turn-on transition to avoid the noise. Then the comparator compares the power switch current to V_{COMP}. When the sensed current exceeds V_{COMP}, the comparator outputs low to turn off the HS-FET. The maximum current of the internal power MOSFET is internally limited cycle by cycle.

Hiccup Protection

When the output is shorted to ground, and the output voltage drops below 70% of its nominal output, the IC is shut down momentarily and begins discharging the soft-start capacitor. The device restarts with a full soft start when the soft-start capacitor is fully discharged. This hiccup process is repeated until the fault is removed.

Start-Up and Shutdown

If both VIN and EN exceed their respective thresholds, the chip starts. The reference block starts first, generating a stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

While the internal supply rail is up, an internal timer holds the power MOSFET off for about 50µs to blank the start-up glitches. When the soft-start block is enabled, it first holds its SS output low to ensure the remaining circuitries are ready, then slowly ramps up.

Three events shut down the chip: EN going low, V_{IN} going low, and thermal shutdown. In the shutdown procedure, the signaling path is blocked first to avoid any fault triggering. V_{COMP} and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command, but its charging path is disabled.

Power Good (PG) Output

The MPQ4360 includes an open-drain power good output that indicates the output voltage status. Connect PG to a power source via a pull-up resistor if it is used. PG goes high if the output voltage is within 95% to 105% of the nominal voltage PG goes low when the output voltage is above 106.5% or below 93.5% of the nominal voltage.

SYNCIN and SYNCO

The switching frequency can be synced to the rising edge of the clock signal applied at SYNCIN. The recommended SYNCIN frequency range is 350kHz to 2.2MHz (except if V_{OUT} is below 5V). Ensure that the off time for SYNCIN is shorter than the internal oscillator period, or the internal clock may turn on the HS-FET before the rising edge of SYNCIN. There is no limit for the pulse width of SYNCIN, but there is always parasitic capacitance at SYNCIN. If the pulse width is too short, a clear rising and falling edge may not be seen due to the parasitic capacitance. A pulse longer than 100ns is recommended.

When applying SYNCIN in AAM, drive SYNCIN below its specified threshold (0.4V) or leave SYNCIN floating before the MPQ4360 starts up. When there is an external SYNCIN clock, do not float the SYNCIN pin; instead, connect a resistor to GND. Considering the SYNCIN's drive capability, the resistor is recommended to be between 10kΩ and 51kΩ.

The SYNCO pin provides a default 180° phase-shift clock to the internal oscillator when there is no SYNCIN signal. The SYNCO pin provides a reverse clock signal to SYNCIN if an external clock signal is applied at SYNCIN (see Figure 5).

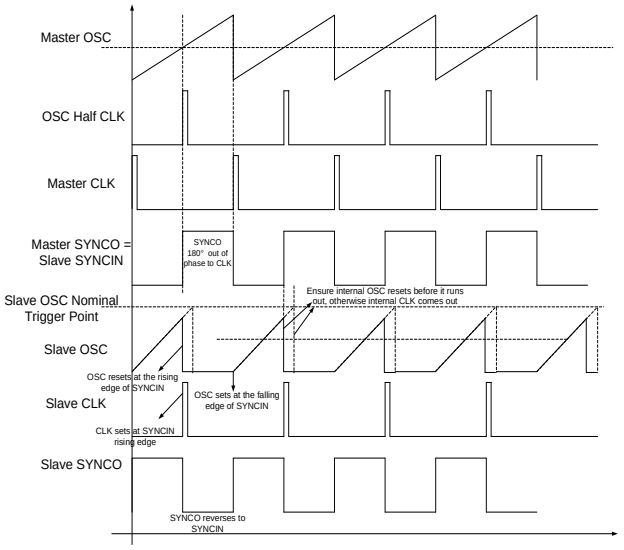


Figure 5: SYNCIN and SYNCO Scheme

The SYNCO pin allows designers to enable a dual-phase, interleaved configuration (see Figure 6).

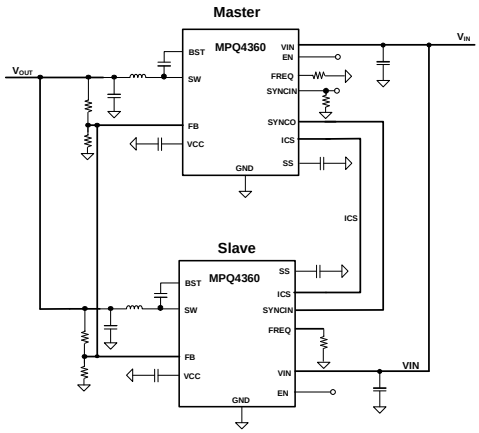


Figure 6: Dual-Phase Configuration

For multi-phase applications, the VOUT, FB, and ICS pins of parallel devices must be connected together. The master's SYNCO pin is connected to the slave's SYNCIN pin for configurations with interleaved phases (see Figure 7).

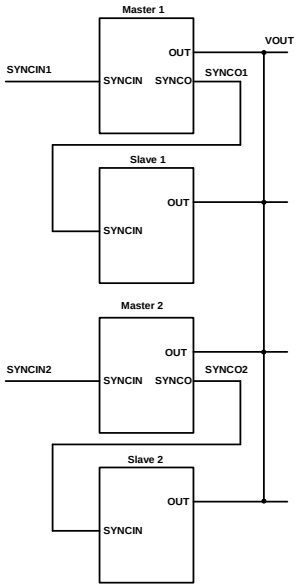


Figure 7: Four-Phase Configuration

Figure 8 shows the phase shift function.

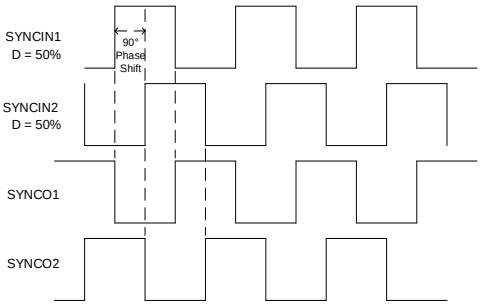


Figure 8: Phase Shift

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider connected to FB sets the output voltage (see Figure 9).

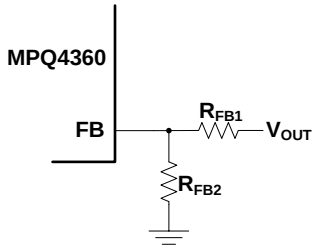


Figure 9: Feedback Network

Calculate R_{FB2} with Equation (2):

$$R_{FB2} = \frac{R_{FB1}}{\frac{V_{OUT}}{0.815V} - 1} \quad (2)$$

Table 2 lists the recommended feedback resistor values for common output voltages.

Table 2: Resistor Selection for Output Voltages

V_{OUT} (V)	R_{FB1} (kΩ)	R_{FB2} (kΩ)
3.3	100 (1%)	32.4 (1%)
5	100 (1%)	19.6 (1%)

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. For the best performance, use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients.

For most applications, use a 4.7µF to 10µF capacitor. It is strongly recommended to use an additional, lower-value capacitor (e.g. 0.1µF) with a small package size (0603) to absorb high-frequency switching noise. Place the smaller capacitor as close to VIN and GND as possible.

Since C_{IN} absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (3):

$$I_{CIN} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (3)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, calculated with Equation (4):

$$I_{CIN} = \frac{I_{LOAD}}{2} \quad (4)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1µF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated with Equation (5):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (5)$$

Selecting the Output Capacitor

The output capacitor maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For the best results, use low-ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 f_{SW} \times C_{OUT}}) \quad (6)$$

Where L is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (7)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency.

For simplification, the output voltage ripple can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (8)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MPQ4360 can be optimized for a wide range of capacitance and ESR values.

Selecting the Inductor

A 1µH to 10µH inductor with a DC current rating at least 25% higher than the maximum load current is recommended for most applications. For higher efficiency, choose an inductor with a lower DC resistance. A larger-value inductor results in less ripple current and a lower output ripple voltage, but also has a larger physical size, higher series resistance, and lower saturation current. A good rule to determine the inductor value is to allow the inductor ripple current to be approximately 30% of the maximum load current. The inductance value can be calculated with Equation (9):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (9)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (10):

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

V_{IN} Under-Voltage Lockout (UVLO) Setting

The MPQ4360 has an internal, fixed under-voltage lockout (UVLO) threshold. The rising threshold is 3V, while the falling threshold is about 2.7V. For applications that require a higher UVLO point, place an external resistor divider between VIN and EN to raise the equivalent UVLO threshold (see Figure 10).

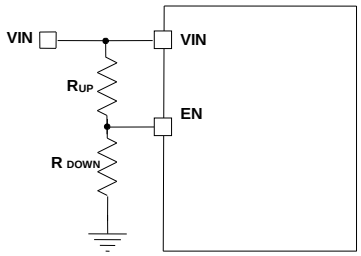


Figure 10: Adjustable UVLO Using EN Divider

The UVLO rising and falling thresholds can be calculated with Equation (11) and Equation (12), respectively:

$$INUV_{RISING} = (1 + \frac{R_{UP}}{R_{DOWN}}) \times V_{EN\_RISING} \quad (11)$$

$$INUV_{FALLING} = (1 + \frac{R_{UP}}{R_{DOWN}}) \times V_{EN\_FALLING} \quad (12)$$

Where V_{EN_RISING} is 1V, and $V_{EN\_FALLING}$ is 0.85V.

External BST Diode and Resistor

An external BST diode can improve regulator efficiency when the duty cycle is high. A power supply between 2.5V and 5V can power the external bootstrap diode. It is recommended for V_{CC} or V_{OUT} to be this power supply in the circuit (see Figure 10).

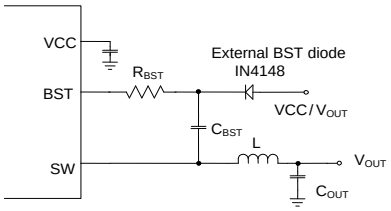


Figure 10: Optional External Bootstrap Diode to Enhance Efficiency

The recommended external BST diode is the IN4148, and the recommended BST capacitor is between 0.1µF and 1µF. A resistor (R_{BST}) in series with the BST capacitor can reduce the SW rising rate and voltage spikes. This helps enhance EMI performance and reduce voltage stress at a high V_{IN}. A higher resistance improves SW spike reduction but compromises efficiency. To make a tradeoff between EMI and efficiency, a ≤20Ω R_{BST} is recommended.

Setting the VCC Capacitor

The VCC capacitor should be 10 times greater than the boost capacitor, and at least 4.7µF nominal. A VCC capacitor exceeding 68µF is not recommended.

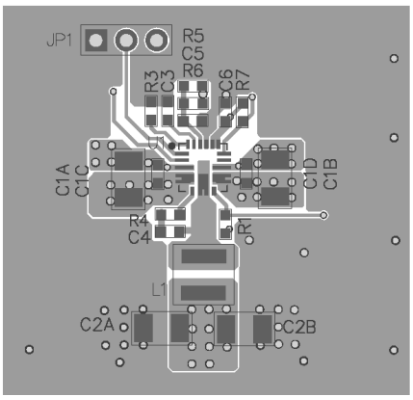
PCB Layout Guidelines [10]

Efficient PCB layout, especially for input capacitor placement, is critical for stable operation. A 4-layer layout is strongly recommended to improve thermal performance. For the best results, refer to Figure 11 and follow the guidelines below:

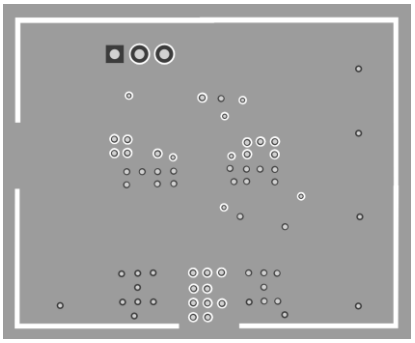
1. Place symmetric input capacitors as close to VIN and GND as possible.
2. Use a large ground plane to connect directly to PGND.
3. Add vias near PGND if the bottom layer is a ground plane.
4. Ensure that the high-current paths at GND and VIN have short, direct, and wide traces.
5. Place the ceramic input capacitor, especially the small package size (0603) input bypass capacitor, as close to VIN and PGND as possible to minimize high-frequency noise.
6. Keep the connection of the input capacitor and VIN as short and wide as possible.
7. Place the VCC capacitor as close to VCC and GND as possible.
8. Route SW and BST away from sensitive analog areas, such as FB.
9. Place the feedback resistors close to the chip to ensure the trace that connects to FB is as short as possible.
10. Use multiple vias to connect the power planes to the internal layers.

Note:

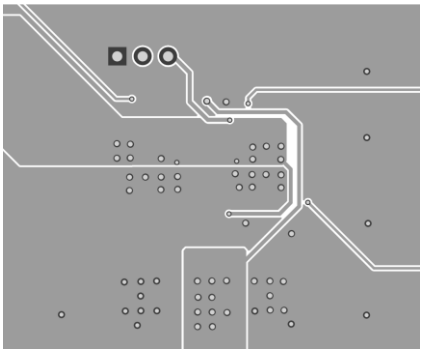
10) The recommended PCB layout is based on Figure 12 on page 40.



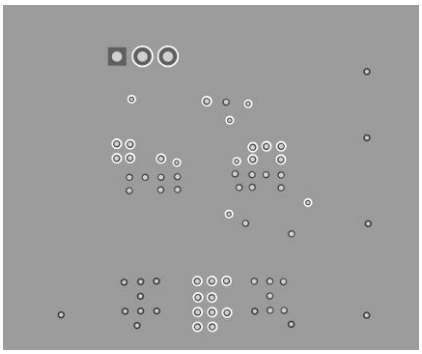
Top Layer



Inner Layer 1



Inner Layer 2



Bottom Layer

Figure 11: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

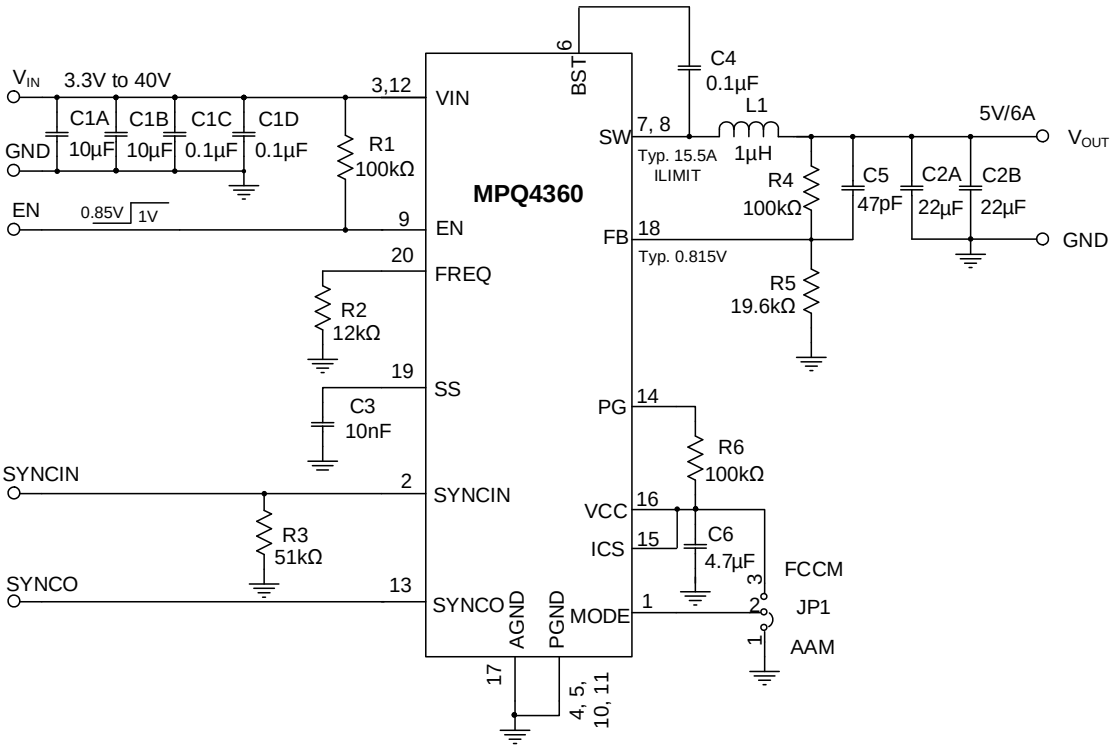


Figure 12: Single-Phase Operation, V_{OUT} = 5V, f_{SW} = 2.2MHz

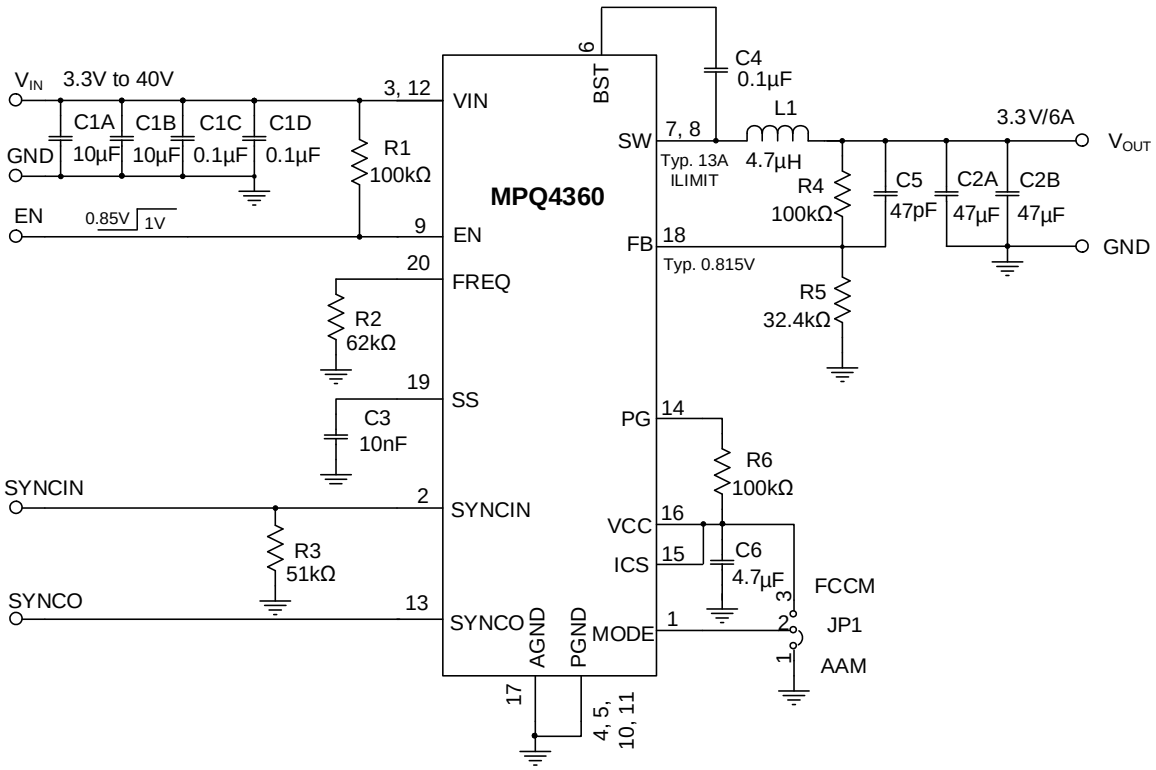


Figure 13: Single-Phase Operation, V_{OUT} = 3.3V, f_{SW} = 470kHz

TYPICAL APPLICATION CIRCUITS *(continued)*

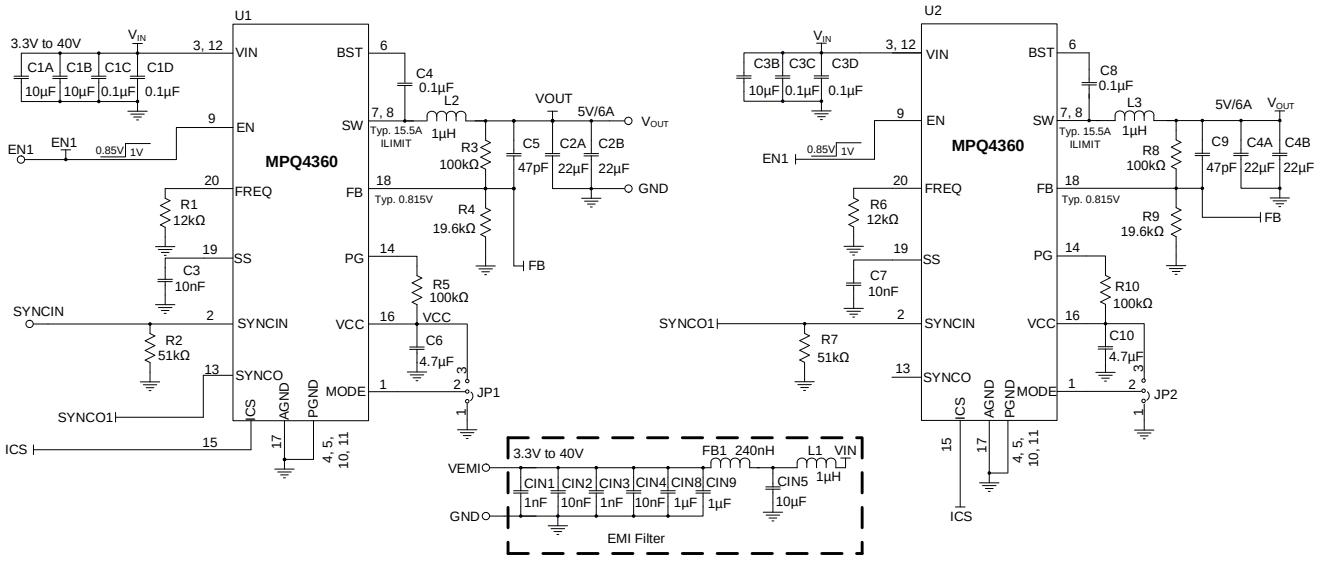


Figure 14: Dual-Phase Operation, V_{OUT} = 5V, f_{SW} = 2.2MHz

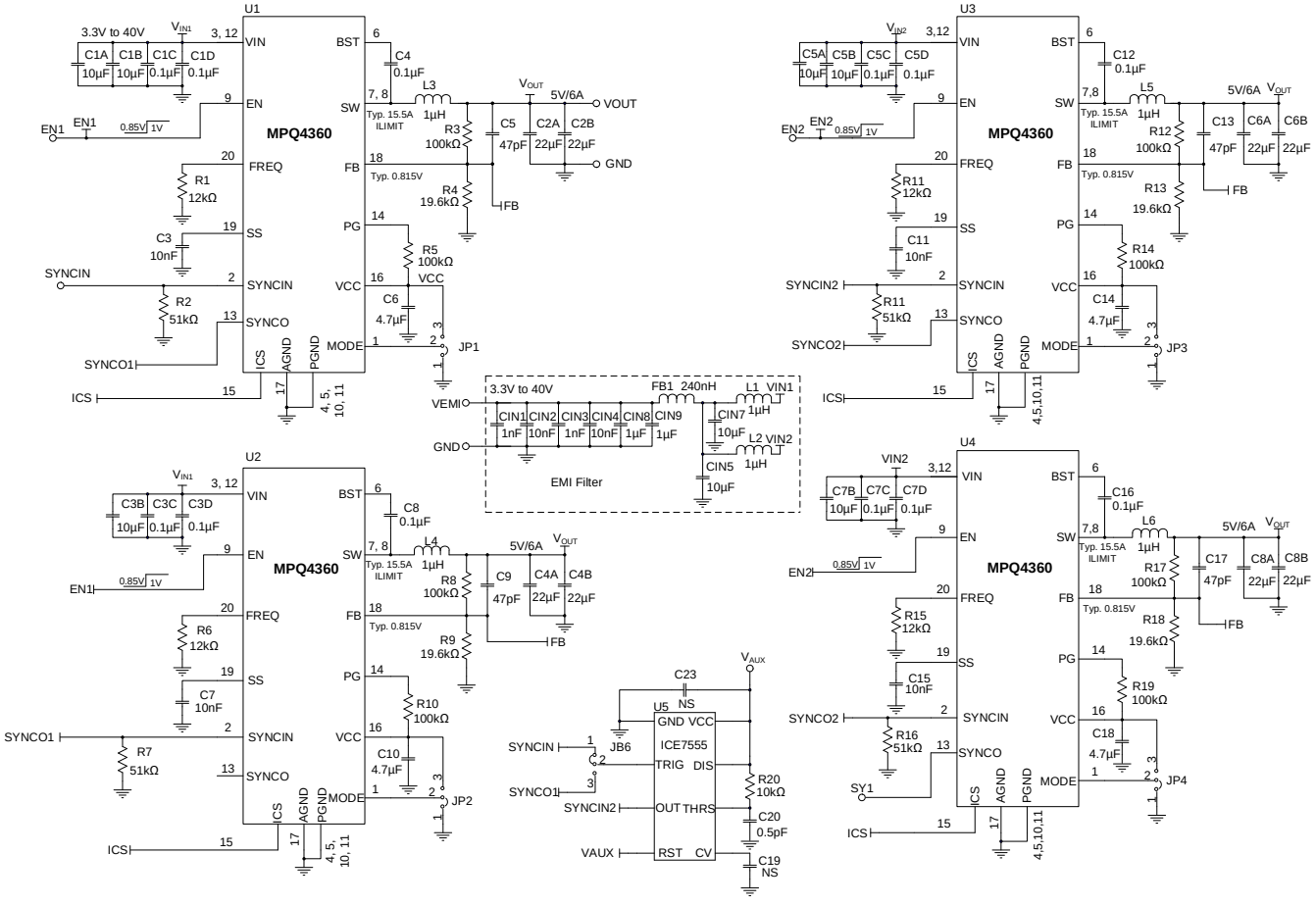
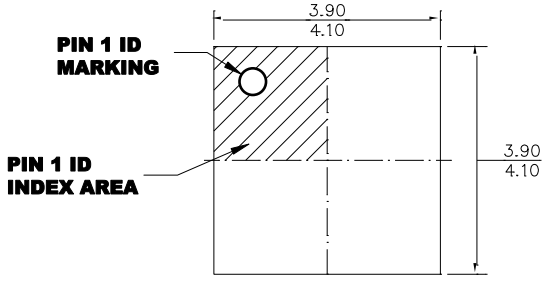


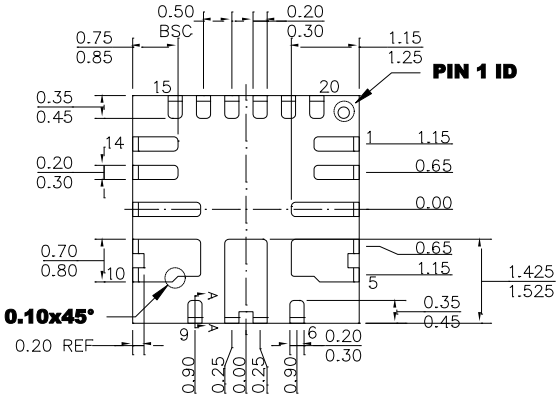
Figure 15: Four-Phase Operation, V_{OUT} = 5V, f_{SW} = 2.2MHz

PACKAGE INFORMATION

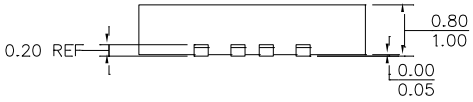
QFN-20 (4mmx4mm)
Wettable Flank



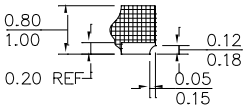
TOP VIEW



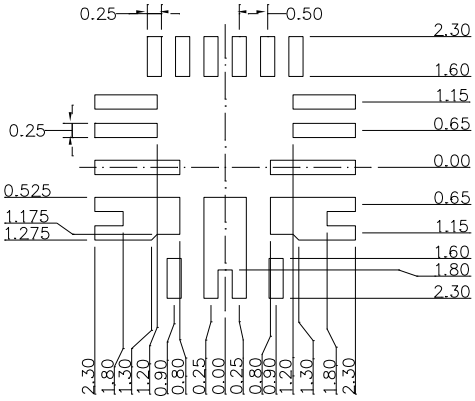
BOTTOM VIEW



SIDE VIEW



SECTION A-A

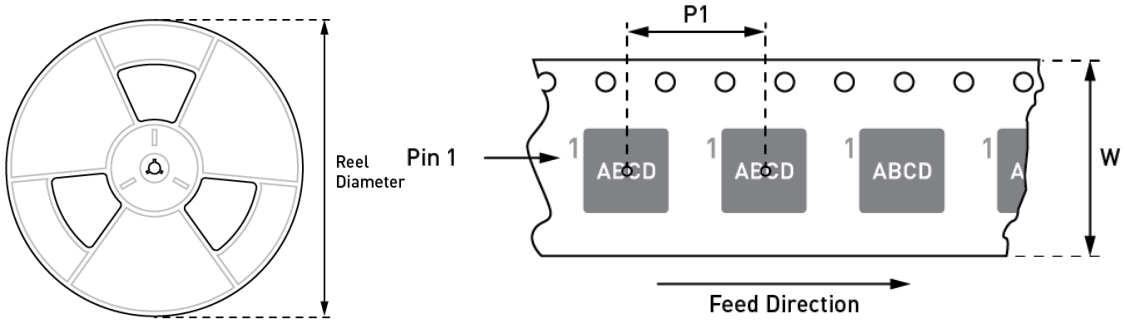


RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube (11)	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ4360GRE-AEC1-Z	QFN-20 (4mmx4mm)	5000	N/A	13in	12mm	8mm

Note:

11) N/A indicates “not available” in tubes. For 500 piece tape & reel prototype quantities, see the factory. (Order code for 500 piece partial reel is “-P”, tape & reel dimensions are the same as the full reel.)

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	9/27/2021	Initial Release	-