ADVANCE

CYPD319X-24LDXS

USB Type-C Port Controller

General Description

EZ-PD™ CYPD319X devices are Cypress' highly integrated USB Type-C port controllers that comply with the latest USB Type-C and Power Delivery (PD) standards and are targeted for automotive charger applications such as rear seat chargers, infotainment head unit chargers, and rear seat entertainment chargers. In such applications, CYPD319X devices provide additional functionalities and BOM integration advantages. CYPD319X uses Cypress' proprietary M0S8 technology with a 32-bit Arm® Cortex®-M0 processor, 64-KB flash, a complete Type-C USB-PD transceiver, all termination resistors required for a Type-C port, an integrated feedback control circuitry for voltage (VBUS) regulation, and system-level ESD protection. They are available in 24-pin QFN wettable flank packages. The inclusion of a fully programmable MCU with analog and digital peripherals allows the implementation of custom system management functions such as power throttling, load sharing, and temperature monitoring.

Features

Type-C Support and USB-PD Support

- Supports USB PD3.0 Version 1.1 including Programmable Power Supply Mode
- Configurable resistors R_P and R_D
- Supports one USB Type-C port and one Type-A port

2x Legacy/Proprietary Charging Blocks

- Supports QC 4.0, Apple charging 2.4A, AFC, BC 1.2
- Integrates all required terminations on DP/DM lines

Integrated Voltage (VBUS) Regulation and Current Sense Amplifier

- Integrated shunt regulator function for VBUS control
- Constant current or constant voltage mode
- Supports current sensing for constant current control

System-Level Fault Protection

- VBUS-to-CC Short Protection
- On-chip VBUS, OVP, OCP, UVP, and SCP
- Supports OTP through integrated ADC circuit and internal temperature sensor

32-bit MCU Subsystem

- Arm Cortex-M0 CPU
- 64-KB Flash
- 8-KB SRAM

Clocks and Oscillators

- Integrated oscillator eliminating the need for external clock

Power

- 3.0-V to 24.5-V operation (30-V tolerant)

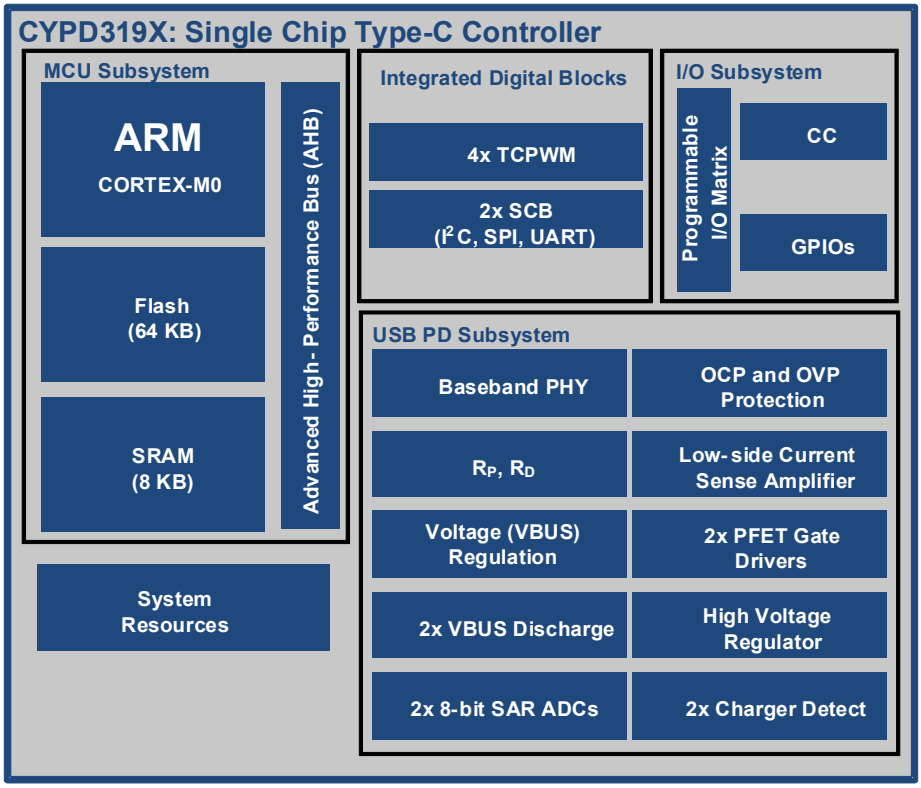
System-Level ESD Protection

- On CC, VBUS_C_MON_DISCHARGE, DP0, DM0, P2.2, and P2.3 pins
- ±8-kV Contact Discharge and ±15-kV Air Gap Discharge based on IEC61000-4-2 level 4C

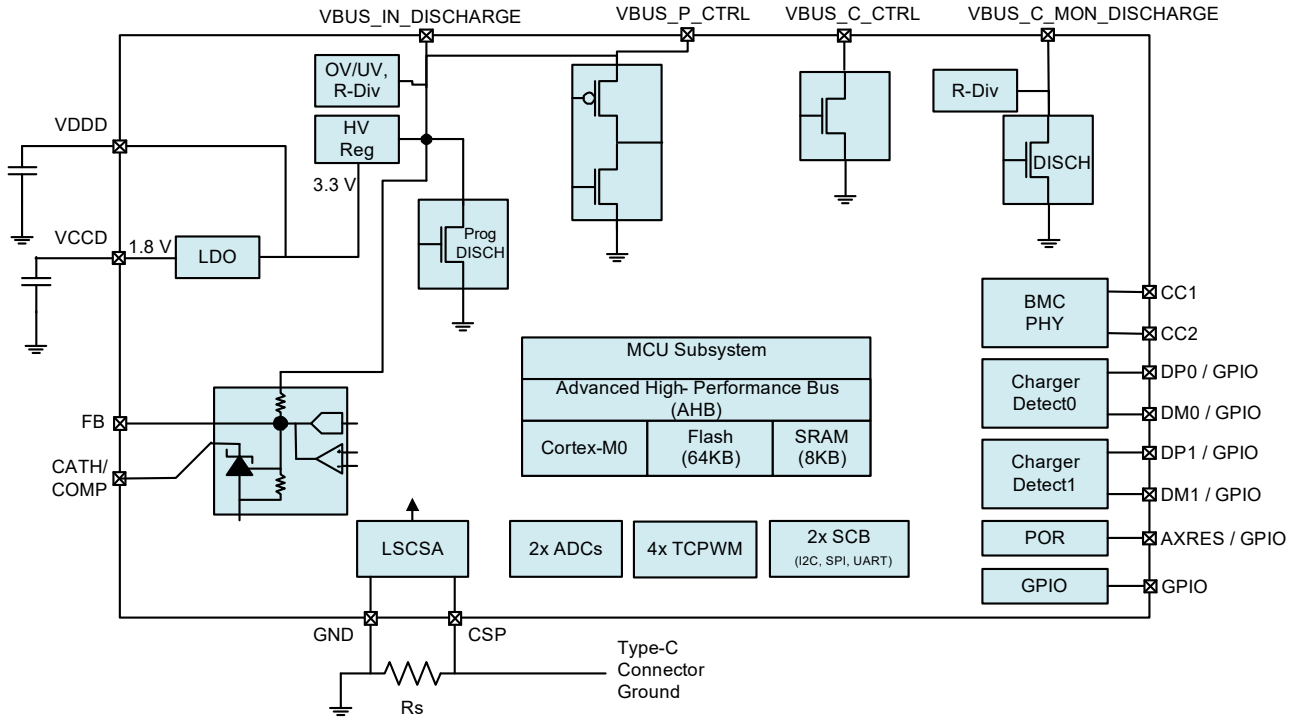
Packages

- 24-pin QFN, wettable flank, AEC-Q100
- Supports automotive temperature range (–40 °C to +105 °C)

Logic Block Diagram



Internal Block Diagram



Contents

Functional Overview

MCU Subsystem

CPU

The Cortex-M0 CPU in CYPD319X devices is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating.

The CPU also includes a serial wire debug (SWD) interface, which is a two-wire form of JTAG. The debug configuration used for CYPD319X devices has four break-point (address) comparators and two watchpoint (data) comparators.

Flash

CYPD319X devices have a flash module with one bank of 64-KB flash, a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block.

SROM

A supervisory ROM that contains boot and configuration routines is provided.

USB-PD Subsystem (SS)

The USB-PD subsystem provides the interface to the Type-C USB port. This subsystem comprises a current sense amplifier, a high-voltage regulator, overvoltage protection (OVP), overcurrent protection (OCP), and supply switch blocks. This subsystem also includes all ESD required and supported on the Type-C port.

USB-PD Physical Layer

The USB-PD Physical Layer consists of a transmitter and receiver that communicate BMC-encoded data over the CC channel based on the PD 3.0 standard. All communication is half-duplex. The Physical Layer or PHY practices collision avoidance to minimize communication errors on the channel.

The USB-PD block includes all termination resistors (R_P and R_D) and their switches as required by the USB-PD specification. R_P and R_D resistors are required to implement connection detection and plug orientation detection, and establish USB DFP/UFP roles. The R_P resistor is implemented as a current source.

According to the USB Type-C specification, Type-C controllers such as CYPD319X devices must present certain termination resistors depending on its role in its unpowered state. As a car charger, CYPD319X devices are in a DFP role (as a power source), which requires both CC lines to be open.

ADC

The ADC is a low-footprint 8-bit SAR ADC that is available for general-purpose A/D conversion applications in the device. This ADC can be accessed from all GPIOs and the DP/DM pins through an on-chip analog mux. CYPD319X devices contain two instances of the ADC.

The voltage reference for the ADCs is generated either from the VDDD supply or from internal bandgap. When sensing the GPIO pin voltage with an ADC, the pin voltage cannot exceed the VDDIO supply value.

Charger Detection

The two charger detection blocks connected to the two pairs of DP/DM pins allow CYPD319X devices in DFP mode to detect conventional battery chargers conforming to BC 1.2, and the following proprietary charger specifications: Apple, Qualcomm's QuickCharge 4.0, and Samsung AFC.

VBUS Overcurrent and Overvoltage Protection

CYPD319X devices have an integrated hardware block for VBUS OVP/OCP with configurable thresholds and response times on the Type-C port.

VBUS Short Protection

CYPD319X devices provide four VBUS short protection pins: CC1, CC2, P2.2, and P2.3. These pins are protected from accidental shorts to high-voltage VBUS. Accidental shorts may occur because the CC1 and CC2 pins are placed next to the VBUS pins in the USB Type-C connector. A Power Delivery controller without the high-voltage VBUS short protection will be damaged in the event of accidental shorts. When the protection circuit is triggered, CYPD319X devices can handle up to 17 V forever and between 17 V to 22 VDC for 1000 hours on the OVT pins. When a VBUS short event occurs on the CC pins, a temporary high-ringing voltage is observed due to the RLC elements in the USB Type-C cable. Without the CYPD319X devices connected, this ringing voltage can be twice (44 V) the maximum VBUS voltage (21.5 V). However, when CYPD319X devices are connected, they are capable of clamping temporary high-ringing voltage and protecting the CC pin using IEC ESD protection diodes.

Current Sense Amplifier (CSA)

CYPD319X devices also have an integrated current sense amplifier that is capable of detecting current in the order of 100 mA across a 5-mΩ external resistor. It also supports constant current mode of operation in charging applications.

PFET Gate Drivers on VBUS Path

CYPD319X devices have two integrated PFET gate drivers to drive external PFETs on the VBUS provider and consumer path. The VBUS_P_CTRL gate driver has an active pull-up, and thus can drive high, low, or High-Z.

The VBUS_C_CTRL gate driver can drive only low or high-Z, thus requiring an external pull-up. These pins are VBUS voltage-tolerant.

VBUS Discharge FETs

CYPD319X devices also have two integrated VBUS discharge FETs used to discharge VBUS to meet the USB-PD specification timing on a detach condition. The VBUS discharge FET on the provider side can be used to accelerate the ramp down of VBUS to the default 5 V on the secondary side.

Voltage (VBUS) Regulation

CYPD319X devices contain an integrated feedback control circuitry with analog regulation of the feedback pin to achieve the appropriate voltage on VBUS pin according to the negotiated contract with the peer device over Type-C.

Integrated Digital Blocks

Serial Communication Blocks (SCB)

CYPD319X devices have two SCBs, which can be configured to implement an I^2C, SPI, or UART interface. The hardware I^2C blocks implement full multi-master and slave interfaces capable of multimaster arbitration. In the SPI mode, the SCB blocks can be configured to act as master or slave.

In the I^2C mode, the SCB blocks are capable of operating at speeds of up to 1 Mbps (Fast-mode Plus) and have flexible buffering options to reduce interrupt overhead and latency for the CPU. These blocks also support I^2C that creates a mailbox address range in the memory of CYPD319X devices and effectively reduces I^2C communication to reading from and writing to an array in memory. In addition, the blocks support 8-deep FIFOs for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduce the need for clock stretching caused by the CPU not having read the data on time.

The I^2C peripherals are compatible with the I^2C Standard-mode, Fast-mode, and Fast-mode Plus devices as defined in the NXP I^2C-bus specification and user manual (UM10204). The I^2C bus I/Os are implemented with GPIO in open-drain modes.

The I^2C port on the SCB blocks of CYPD319X devices is not completely compliant with the I^2C specification in the following aspects:

- GPIO cells for the SCB 1 I^2C port are not overvoltage-tolerant and, therefore, cannot be hot-swapped or powered up independent of the rest of the I^2C system.
- Fast-mode Plus has an I_{OL} specification of 20 mA at a V_{OL} of 0.4 V. The GPIO cells can sink a maximum of 8-mA I_{OL} with a V_{OL} maximum of 0.6 V.
- Fast-mode and Fast-mode Plus specify minimum fall times, which are not met with the GPIO cell; Slow strong mode can help meet this spec depending on the bus load.

Timer/Counter/PWM Block (TCPWM)

CYPD319X devices have four TCPWM blocks. Each implements a 16-bit timer, counter, pulse-width modulator (PWM), and quadrature decoder functionality. The block can be used to measure the period and pulse width of an input signal (timer), find the number of times a particular event occurs (counter), generate PWM signals, or decode quadrature signals.

I/O Subsystem

CYPD319X devices have up to 12 GPIOs some of which can be re-purposed to support SCB functions (I^2C, UART, SPI). GPIO pins P0.0 and P0.1 are overvoltage-tolerant (OVT) (up to 7 V).

The GPIO block implements the following:

- Seven drive strength modes:
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL)
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Hold mode to latch previous state (used to retain the I/O state in Deep Sleep mode)
- Selectable slew rates for dV/dt related noise control to improve EMI

During power-on and reset, I/O pins are forced to the disable state so as to not crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Port pins P1.0 and P1.1 can be configured to indicate a fault for OCP/SCP/OVP/UVP conditions. Any two fault conditions can be mapped to two GPIOs, or all four faults can be OR'ed to indicate over one GPIO.

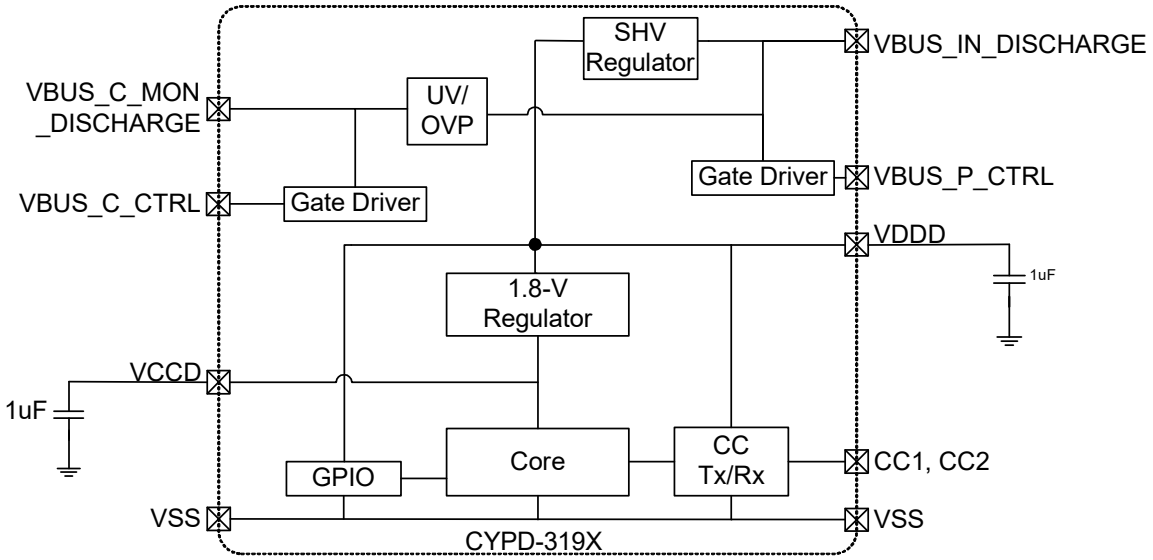
Power Systems Overview

CYPD319X devices can operate from two possible external supply sources: VBUS_IN_DISCHARGE (3.0 V–24.5 V) or VDDD (2.7 V–5.5 V). When powered through VBUS_IN_DISCHARGE, the internal regulator generates VDDD of 3.3 V for device operation. The regulated supply, VDDD, is either used directly inside some analog blocks or further regulated down to VCCD (1.8 V), which powers majority of the core using the regulators. CYPD319X devices have three different power modes: Active, Sleep, and Deep Sleep. Transitions between these power modes are managed by the power system. When powered through the VBUS_IN_DISCHARGE pin, VDDD cannot be used to power external devices and should be connected to a 1-µF capacitor for regulator stability only. These pins are not supported as power supplies. Refer to the application diagrams for capacitor connections.

Table 1. CYPD319X Power Modes

Mode	Description
Power-On Reset (POR)	Power is valid and an internal reset source is asserted, or SleepController is sequencing the system out of reset.
ACTIVE	Power is valid and CPU is executing instructions.
SLEEP	Power is valid and CPU is not executing instructions. All logic that is not operating is clock-gated to save power.
DEEP SLEEP	Main regulator and most blocks are shut off. DeepSleep regulator powers logic, but only low-frequency clock is available.

Figure 1. Power System Requirement Block Diagram

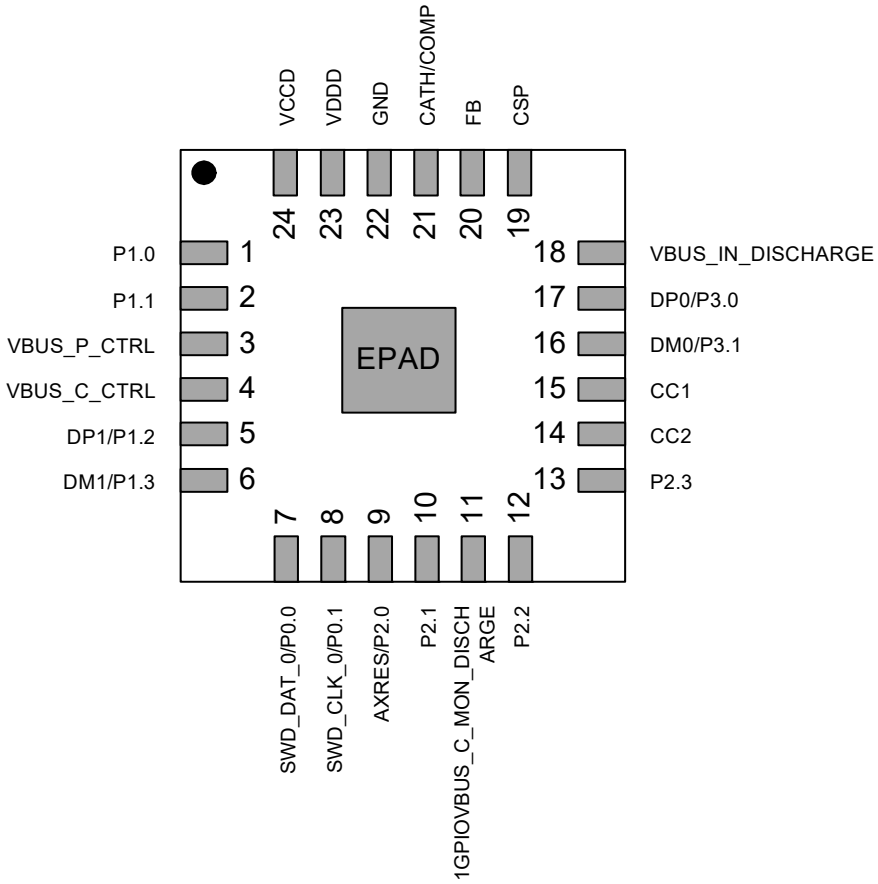


Pinouts

Table 2. Pin Descriptions

24-Pin QFN	Pin Name	Description
1	P1.0	Port 1 pin 0: GPIO/UART_1_CTS/I2C_SDA_1 / TCPWM_line_0, Programmable SCP/OCP/OVP/UVP Fault indication
2	P1.1	Port 1 pin 1: GPIO/UART_1_RTS/I2C_SCL_1 / TCPWM_line_1, Programmable SCP/OCP/OVP/UVP Fault indication
3	VBUS_P_CTRL	Provider (PMOS) FET control (30-V tolerant) 0: Path ON 1: Path OFF
4	VBUS_C_CTRL	VBUS consumer (PMOS) FET control (30-V tolerant) 0: Path ON Z: Path OFF
5	DP1/P1.2	USB D+/Port 1 pin 2: GPIO/UART_1_TX1/AFC/QC/BC 1.2/Apple Charging/No IEC
6	DM1/P1.3	USB D-/Port 1 pin 3: GPIO/UART_1_RX1/AFC/QC/BC 1.2/Apple Charging/No IEC
7	SWD_DAT_0/P0.0	Port 0 pin 0: GPIO/OVT/I2C_SDA_0/TCPWM_line_0/UART_0_CTS
8	SWD_CLK_0/P0.1	Port 0 pin 1: GPIO/OVT/I2C_SCL_0/TCPWM_line_1/UART_0_RTS
9	AXRES/P2.0	Port 2 pin 0: GPIO/Alternate XRES/TCPWM_line_0//UART_0_TX0
10	P2.1	Port 2 pin 1: GPIO/TCPWM_line_1//UART_0_RX0
11	VBUS_C_MON_DISCHARGE	Type-C VBUS Monitor with Internal Discharge FET
12	P2.2	Port 2 pin 2: GPIO with open drain with pull-up assist. Configurable as GPIO_20VT/I2C_SDA_1/IEC. Tolerant to temporary short to VBUS pin.
13	P2.3	Port 2 pin 3: GPIO with open drain with pull-up assist. Configurable as GPIO_20VT/I2C_SCL_1/IEC. Tolerant to temporary short to VBUS pin.
14	CC2	Communication Channel 2 with Dead-battery Rd Bonding Option/IEC. Tolerant to temporary short to VBUS pin.
15	CC1	Communication Channel 1 with Dead-battery Rd Bonding Option/IEC. Tolerant to temporary short to VBUS pin.
16	DM0/P3.1	USB D–/Port 3 pin 1: GPIO/UART_1_RX0/AFC/QC/BC 1.2/Apple Charging/IEC
17	DP0/P3.0	USB D+/Port 3 pin 0: GPIO/UART_1_TX0/AFC/QC/BC 1.2/Apple Charging/IEC
18	VBUS_IN_DISCHARGE	VBUS power IN (3.0 V–24.5 V) with internal discharge FET
19	CSP	CS+: Current sense input
20	FB	Voltage regulation feedback pin
21	CATH/COMP	Cathode of voltage regulation and compensation for other applications
22	GND	Ground
23	VDDD	Power input: 2.7 V–5.5 V
24	VCCD	1.8-V core voltage pin (not intended for use as a power source)
–	EPAD	Ground

Figure 2. 24-QFN Package Pinout (Top View)



CYPD319X Programming and Bootloading

There are two ways to program the application firmware into a CYPD319X device:

- Programming the device flash over the SWD Interface
- Application firmware update over the CC interface

Generally, CYPD319X devices are programmed over the SWD interface only during development or during the manufacturing process of the end product. After the end product is manufactured, the CYPD319X device's application firmware can be updated via the CC bootloader interface.

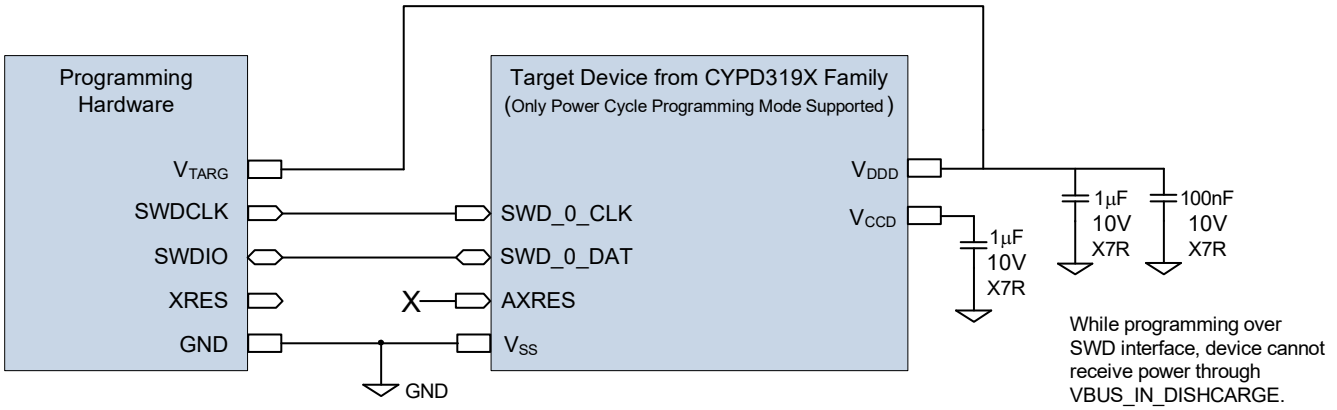
Programming the Device Flash over SWD Interface

CYPD319X devices can be programmed using the SWD interface. Cypress provides a programming kit, CY8CKIT-002 MiniProg3 Kit and PSoC Programmer Software, which can be used to program the flash as well as debug firmware. The flash is programmed by downloading the information from a hex file. This hex file is a binary file generated as an output of building the firmware project in PSoC Creator Software. Click here for more information on how to use the MiniProg3 programmer. There are many third-party programmers that support mass programming in a manufacturing environment.

As shown in the block diagram in Figure 3, the SWD_0_DAT and SWD_0_CLK pins are connected to the host programmer's SWDIO (data) and SWDCLK (clock) pins respectively. During SWD programming, CYPD319X devices must be powered by the host programmer by connecting its VTARG (power supply to the target device) to the VDDD pin of a CYPD319X device. While programming over the SWD interface, the CYPD319X device cannot receive power through VBUS_IN_DISCHARGE.

CYPD319X devices do not have an XRES pin. Due to that, the XRES line from the host programmer remains unconnected; therefore, programming using Reset mode is not supported. In other words, CYPD319X devices are supported by Power Cycle programming mode only because the XRES line is not used. Contact Cypress for further details on CYPD3XXX Programming Specifications.

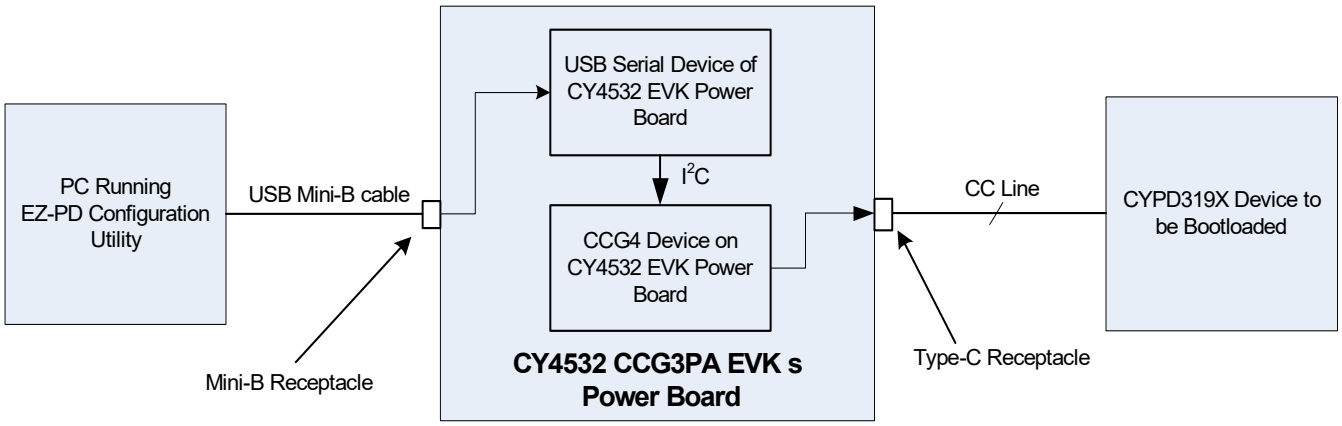
Figure 3. Connecting the Programmer to CYPD319X Device



Application Firmware Update over CC Interface

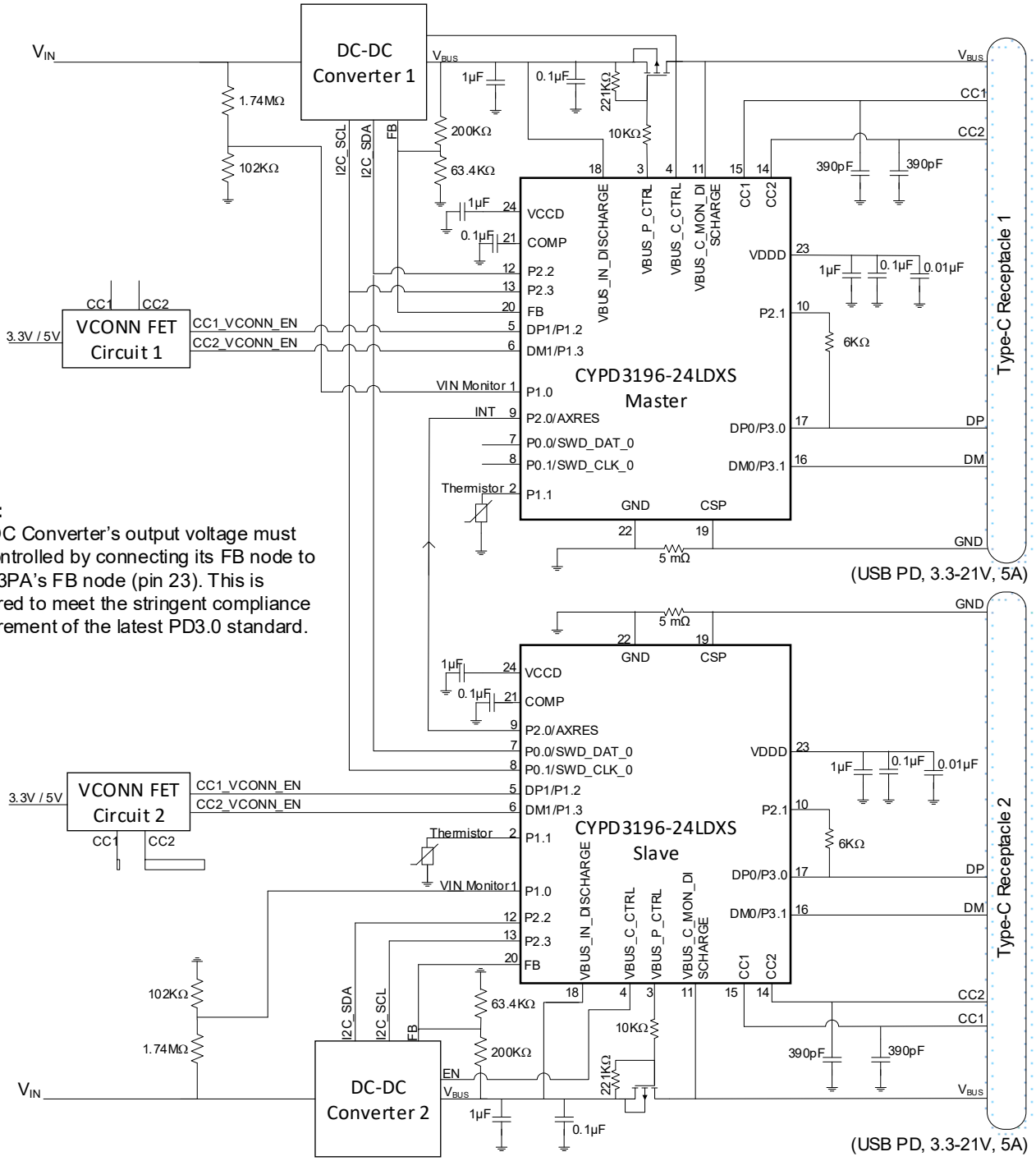
For bootloading CYPD319X device-based applications, the CY4532 CCG3PA EVK can be used to send programming and configuration data as Cypress-specific Vendor Defined Messages (VDMs) over the CC line. To bootload the CYPD319X device, the CY4532 CCG3PA EVK's power board is connected to the system containing the CYPD319X device on one end and a Windows PC running the EZ-PD™ Configuration Utility on the other end, as shown in Figure 4.

Figure 4. Application Firmware Update over CC Interface



Application Diagrams

Figure 5. Dual Port USB-PD Charge Only Application Diagram Using CYPD3196-24LDXS



Note:
DC-DC Converter's output voltage must be controlled by connecting its FB node to CCG3PA's FB node (pin 23). This is required to meet the stringent compliance requirement of the latest PD3.0 standard.

Note: Refer to Cypress 2x100W Auto reference design files for a detailed schematic and layout

Table 3. Pin Descriptions Specific to Application Diagram in Figure 5

24-Pin QFN	Pin Name	Description
1	P1.0	VIN Monitoring GPIO
2	P1.1	Thermistor
3	VBUS_P_CTRL	Provider (PMOS) FET control (30-V tolerant)
4	VBUS_C_CTRL	Enable DC-DC regulator. This is an optional connection; leave this pin floating if the DC-DC converter is always enabled.
5	DP1/P1.2	Enables CC1 VCONN FET
6	DM1/P1.3	Enables CC2 VCONN FET
7	P0.0/SWD_DAT_0	Master: Free Slave: I2C Slave SDA for Load Sharing Connect to the host programmer's SWDIO (data) for programming the CCG3PA device
8	P0.1/SWD_CLK_0	Master: Free Slave: I2C Slave SCL for Load Sharing Connect to the host programmer's SWDCLK (clock) for programming the CCG3PA
9	P2.0/AXRES	Interrupt from Slave CCG3PA to Master CCG3PA
10	P2.1	GPIO drives 3.3-V output. Connect a 6-K resistor from this pin to DP to realize Apple charging. A 6-k resistor should be used if VDDD is 3.3 V and an 18-K resistor should be used if it is 5 V.
11	VBUS_C_MON_DISCH ARGE	Type-C VBUS Monitor with Internal Discharge FET
12	P2.2/SWD_DAT_1	Master: I2C Master data for DC/DC regulator and for communicating with CCG3PA Slave for Load Sharing Slave: I2C Master data for DC/DC regulator
13	P2.3/SWD_CLK_1	Master: I2C Master clock for DC/DC regulator and for communicating with CCG3PA slave for Load Sharing Slave: I2C Master clock for DC/DC regulator
14	CC2	Communication Channel 2 or VCONN
15	CC1	Communication Channel 1 or VCONN
16	DM0/P3.1	USB D- of Type-C port. Supports BC 1.2, QC, Apple Charging and AFC.
17	DP0/P3.0	USB D+ of Type-C port. Supports BC 1.2, QC, Apple Charging and AFC
18	VBUS_IN_DISCARGE	VBUS power IN (3.0 V–24.5 V) with internal discharge FET
19	CSP	CS+: Current sense input
20	FB	Voltage regulation feedback pin. Must be connected to the feedback node of DC-DC Converter. The pull-up resistor of the resistor divider network must be 200K; the pull-down resistor must be selected such that default VBUS upon power up is 5 V.
21	COMP	Compensation capacitor must be connected to this pin for PPS constant current loop.
22	GND	Ground
23	VDDD	Power input: 2.7 V–5.5 V
24	VCCD	1.8-V core voltage pin. Connect to a 1-uF capacitor.

Figure 6. Dual Port USB-PD Head Unit Application Diagram Using CYPD3195-24LDXS (Power and Data Connectivity)

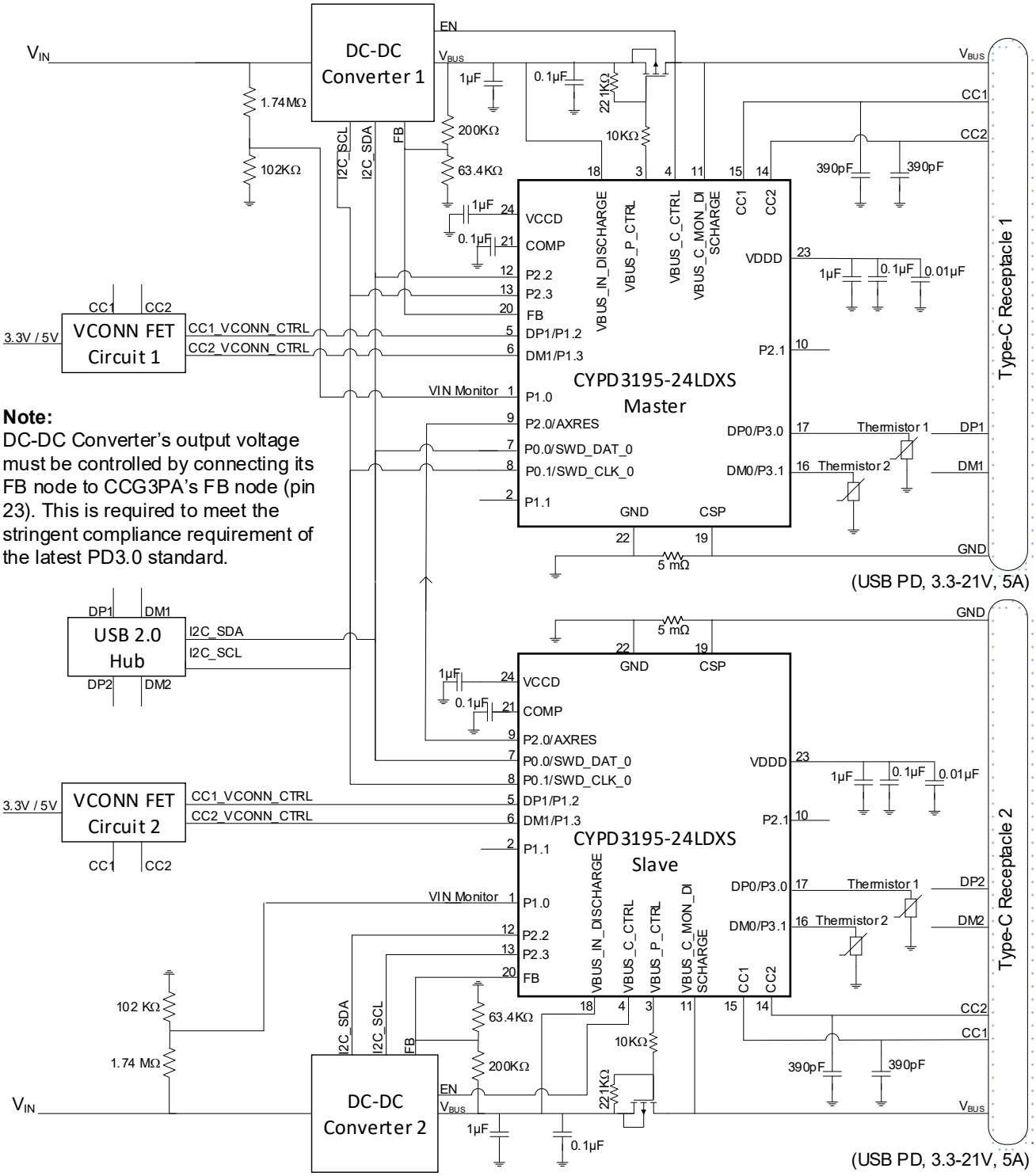
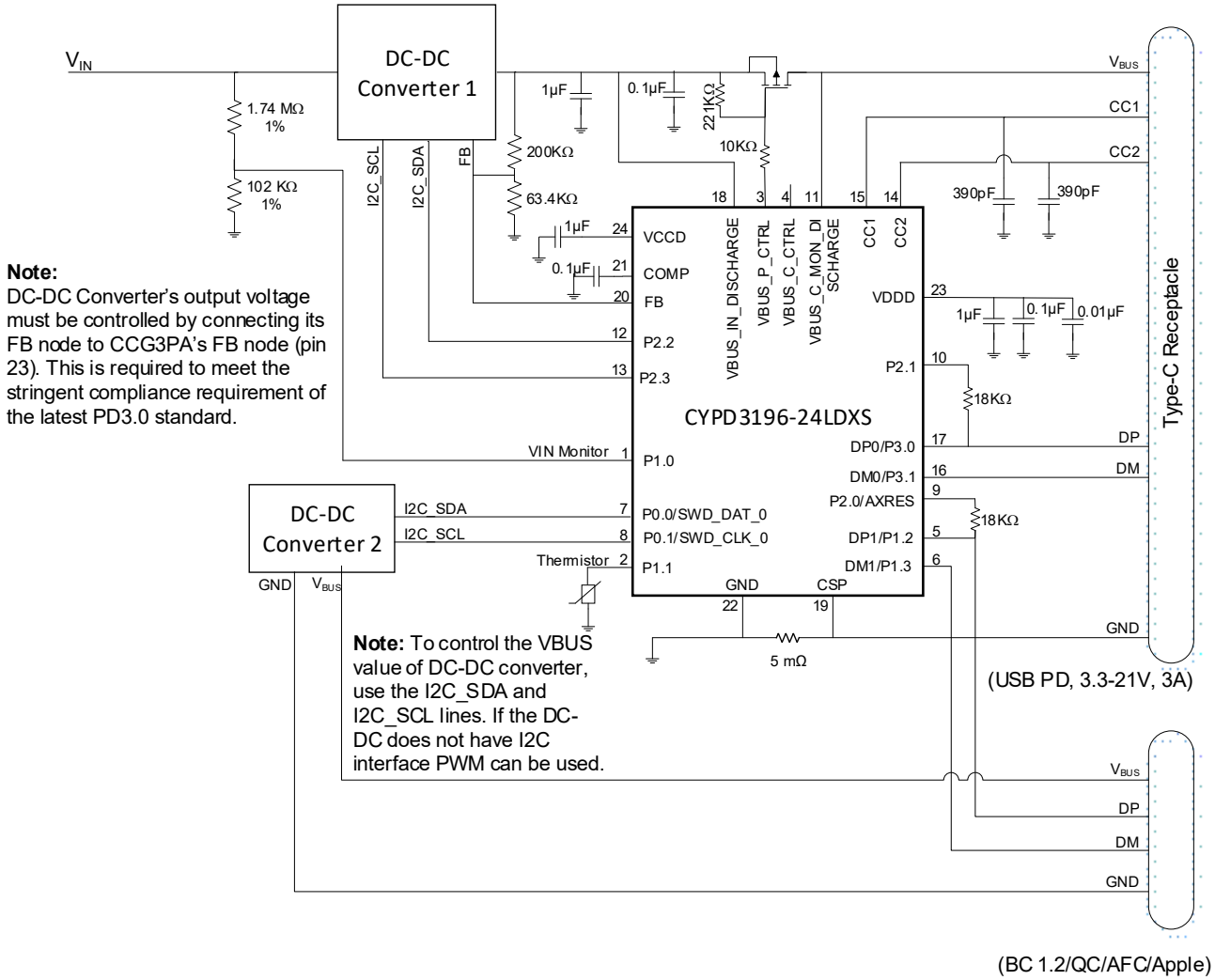


Table 4. Pin Descriptions Specific to Application Diagram in Figure 6

24-Pin QFN	Pin Name	Description
1	P1.0	VIN Monitoring GPIO
2	P1.1	Free
3	VBUS_P_CTRL	Provider (PMOS) FET control (30-V tolerant)
4	VBUS_C_CTRL	Enable DC-DC regulator. This is an optional connection; leave this pin floating if the DC-DC converter is always enabled.
5	DP1/P1.2	Enables CC1 VCONN FET
6	DM1/P1.3	Enables CC2 VCONN FET
7	P0.0/SWD_DAT_0	Master: I2C Slave SDA for communicating with the USB 2.0 Hub Slave: I2C Slave SDA for Load Sharing and for communicating with the USB 2.0 Hub Connect to the host programmer's SWDIO (data) for programming the CCG3PA device
8	P0.1/SWD_CLK_0	Master: I2C Slave SCL for communicating with the USB 2.0 Hub Slave: I2C Slave SCL for Load Sharing and for communicating with the USB 2.0 Hub Connect to the host programmer's SWDCLK (clock) for programming the CCG3PA
9	P2.0/AXRES	Interrupt from Slave CCG3PA to Master CCG3PA
10	P2.1	Free
11	VBUS_C_MON_DISC H ARGE	Type-C VBUS Monitor with Internal Discharge FET
12	P2.2/SWD_DAT_1	Master: I2C Master data for DC/DC regulator and for communicating with CCG3PA Slave for Load Sharing Slave: I2C Master data for DC/DC regulator
13	P2.3/SWD_CLK_1	Master: I2C Master clock for DC/DC regulator and for communicating with CCG3PA Slave for Load Sharing Slave: I2C Master clock for DC/DC regulator
14	CC2	Communication Channel 2 or VCONN
15	CC1	Communication Channel 1 or VCONN
16	DM0/P3.1	Thermistor 1
17	DP0/P3.0	Thermistor 2
18	VBUS_IN_DISCHARG E	VBUS power IN (3.0 V–24.5 V) with internal discharge FET
19	CSP	CS+: Current sense input
20	FB	Voltage regulation feedback pin. Must be connected to the feedback node of DC-DC Converter. The pull-up resistor of the resistor divider network must be 200K; the pull-down resistor must be selected such that default VBUS upon power up is 5 V.
21	COMP	Compensation capacitor must be connected to this pin for PPS constant current loop.
22	GND	Ground
23	VDDD	Power input: 2.7 V–5.5 V
24	VCCD	1.8-V core voltage pin. Connect to a 1-uF capacitor.

Figure 7. Dual Port (Type-C and Type-A) USB-PD Car Charger Application Diagram Using CYPD3196-24LDXS



Note:
DC-DC Converter's output voltage must be controlled by connecting its FB node to CCG3PA's FB node (pin 23). This is required to meet the stringent compliance requirement of the latest PD3.0 standard.

Note: To control the VBUS value of DC-DC converter, use the I2C_SDA and I2C_SCL lines. If the DC-DC does not have I2C interface PWM can be used.

Table 5. Pin Descriptions Specific to Application Diagram in Figure 7

24-Pin QFN	Pin Name	Description
1	P1.0	VIN monitoring GPIO
2	P1.1	Thermistor
3	VBUS_P_CTRL	Provider (PMOS) FET control (30-V tolerant)
4	VBUS_C_CTRL	Enable DC-DC regulator. This is an optional connection; leave this pin floating if the DC-DC converter is always enabled.
5	DP1/P1.2	USB D+ of Type-A port. Supports BC 1.2, QC, Apple Charging and AFC.
6	DM1/P1.3	USB D– of Type-A port. Supports BC 1.2, QC, Apple Charging and AFC.
7	P0.0/SWD_DAT_0	I2C Master SDA for controlling the DC/DC Converter for Type-A port
8	P0.1/SWD_CLK_0	I2C Master SCL for controlling the DC/DC Converter for Type-A port
9	P2.0/AXRES	GPIO drives 3.3-V output. Connect an 18-k resistor from this pin to DP to realize Apple charging. A 6-k resistor should be used if VDDD is 3.3 V and an 18-k resistor should be used if it is 5 V.
10	P2.1	GPIO drives 3.3-V output. Connect an 18-k resistor from this pin to DP to realize Apple charging. A 6-k resistor should be used if VDDD is 3.3 V and an 18-k resistor should be used if it is 5 V.
11	VBUS_C_MON_DISCH ARGE	Type-C VBUS Monitor with Internal Discharge FET
12	P2.2/SWD_DAT_1	I2C Master data for DC/DC regulator
13	P2.3/SWD_CLK_1	I2C Master clock for DC/DC regulator
14	CC2	Communication Channel 2
15	CC1	Communication Channel 1
16	DM0/P3.1	USB D- of Type-C port. Supports BC 1.2, QC, Apple Charging and AFC.
17	DP0/P3.0	USB D+ of Type-C port. Supports BC 1.2, QC, Apple Charging and AFC.
18	VBUS_IN_DISCHARGE	VBUS power IN (3.0 V–24.5 V) with internal discharge FET
19	CSP	CS+: Current sense input
20	FB	Voltage regulation feedback pin. Must be connected to the feedback node of DC-DC Converter. The pull-up resistor of the resistor divider network must be 200K; the pull-down resistor must be selected such that default VBUS upon power up is 5 V.
21	COMP	Compensation capacitor must be connected to this pin for PPS constant current loop.
22	GND	Ground
23	VDDD	Power input: 2.7 V–5.5 V
24	VCCD	1.8-V core voltage pin. Connect to a 1-uF capacitor.

Electrical Specifications

Absolute Maximum Ratings

Table 6. Absolute Maximum Ratings

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{BUS_MAX}	Max supply voltage relative to V_{SS} on VBUS_IN_DISCHARGE and VBUS_C_MON_DISCHARGE pins	–	–	30	V	Absolute max
V_{DDD_MAX}	Max supply voltage relative to V_{SS}	–	–	6	V	
$V_{CC\_PIN\_ABS}$	Max voltage on CC1, CC2 pins and port pins P2.2 and P2.3 for applicable devices	–	–	22[1]	V	
V_{GPIO_ABS}	GPIO voltage	–0.5	–	V_{DDD} +0.5	V	
I_{GPIO_ABS}	Maximum current per GPIO	–25	–	25	mA	
$I_{GPIO\_injection}$	GPIO injection current, Max for $V_{IH} > V_{DDD}$, and Min for $V_{IL} < V_{SS}$	–0.5	–	0.5	mA	Absolute max, current injected per pin
$V_{GPIO\_OVT\_ABS}$	OVT GPIO voltage	–0.5	–	6	V	Applicable to port pins P0.0 and P0.1
ESD_HBM	Electrostatic discharge human body model	2200	–	–	V	–
ESD_CDM	Electrostatic discharge charged device model	500	–	–	V	–
LU	Pin current for latch-up	–100	–	100	mA	–
ESD_IEC_CON	Electrostatic discharge IEC61000-4-2	8000	–	–	V	Contact discharge on CC1, CC2, VBUS, P2.2, and P2.3 pins
ESD_IEC_AIR	Electrostatic discharge IEC61000-4-2	15000	–	–	V	Air discharge for DPLUS, DMINUS, CC1, CC2, VBUS, P2.2, and P2.3 pins

Device-Level Specifications

All device-level specifications will be added in a future version of this document.

Note
1. As per USB PD specification, maximum allowed VBUS = 21.5 V.

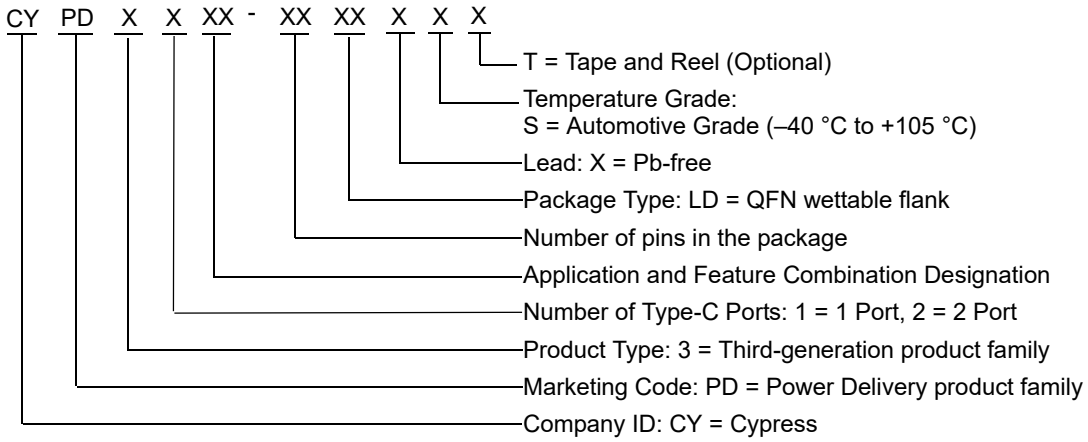
Ordering Information

Table 7 lists the CYPD319X part numbers and features.

Table 7. CYPD319X Ordering Information

MPN	Application	Termination Resistor	Role	Bootloader	Package Type
CYPD3193-24LDXS	Rear-Seat Entertainment	R_P	DFP (Power Source Only)	I^2C Bootloader (Supports External Bill-Board)	24-Pin QFN
CYPD3194-24LDXS				CC Bootloader (Supports External Bill-Board)	
CYPD3195-24LDXS	Head Units/Infotainment			I^2C Bootloader	
CYPD3196-24LDXS	Charge Only Ports			CC Bootloader	

Ordering Code Definitions



Packaging

Table 8. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A	Operating ambient temperature	Automotive S-Grade	-40	25	105	°C
T_J	Operating junction temperature	Automotive S-Grade	-40	25	120	°C
T_{JA}	Package θ_{JA} (24-QFN)	–	–	–	19.98	°C/W
T_{JC}	Package θ_{JC} (24-QFN)	–	–	–	4.78	°C/W

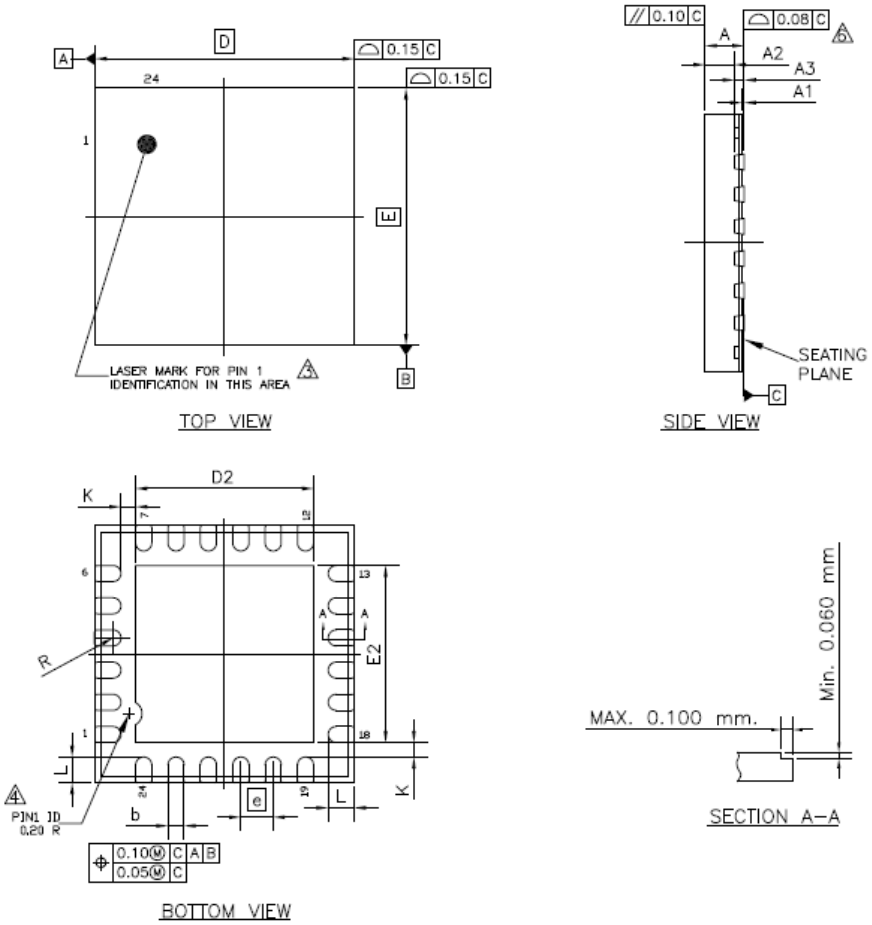
Table 9. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time within 5° C of Peak Temperature
24-pin QFN	260 °C	30 seconds

Table 10. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
24-pin QFN	MSL3

Figure 8. 24-pin QFN Package Outline



SYMBOL	DIMENSIONS		
	MIN	NOM	MAX
A	–	–	0.60
A1	0.00	–	0.05
A2	–	0.400	0.425
A3	0.152 REF		
b	0.18	0.25	0.30
D	4.00 BSC		
E	4.00 BSC		
D2	2.65	2.75	2.85
E2	2.65	2.75	2.85
e	0.50 BSC		
L	0.30	0.40	0.50
K	0.225	–	–
R	0.09	–	–

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. –1994.
3. THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
4. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
5. PACKAGE WARPAGE MAX 0.08 mm.
6. APPLIED FOR EXPOSED PAD AND TERMINALS.
7. JEDEC SPECIFICATION NO. REF. : N/A.

002-23807 Rev**

Acronyms

Table 11. Acronyms Used in this Document

Acronym	Description
ADC	analog-to-digital converter
AES	advanced encryption standard
API	application programming interface
Arm®	advanced RISC machine, a CPU architecture
CC	configuration channel
CCG3	Cable Controller Generation 3
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
CS	current sense
DFP	downstream facing port
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DRP	dual role port
EEPROM	electrically erasable programmable read-only memory
EMCA	electronically marked cable assembly, a USB cable that includes an IC that reports cable characteristics (such as current rating) to the Type-C ports
EMI	electromagnetic interference
ESD	electrostatic discharge
FS	full-speed
GPIO	general-purpose input/output
IC	integrated circuit
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
I/O	input/output, see also GPIO
LDO	low-dropout regulator
LVD	low-voltage detect
LVTTL	low-voltage transistor-transistor logic
MCU	microcontroller unit
NC	no connect
NMI	nonmaskable interrupt
NVIC	nested vectored interrupt controller
opamp	operational amplifier
OCP	overcurrent protection

Table 11. Acronyms Used in this Document

Acronym	Description
OTP	over temperature protection
OVP	overvoltage protection
OVT	overvoltage tolerant
PCB	printed circuit board
PD	power delivery
PGA	programmable gain amplifier
PHY	physical layer
POR	power-on reset
PRES	precise power-on reset
PSoC®	Programmable System-on-Chip™
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RX	receive
SAR	successive approximation register
SCL	I^2C serial clock
SCP	short circuit protection
SDA	I^2C serial data
S/H	sample and hold
SHA	secure hash algorithm
SPI	Serial Peripheral Interface, a communications protocol
SRAM	static random access memory
SWD	serial wire debug, a test protocol
TX	transmit
Type-C	a new standard with a slimmer USB connector and a reversible cable, capable of sourcing up to 100 W of power
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
USB	Universal Serial Bus
USBIO	USB input/output, CCG2 pins used to connect to a USB port
UVP	undervoltage protection
XRES	external reset I/O pin

Document Conventions

Units of Measure

Table 12. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
Hz	hertz
KB	1024 bytes
kHz	kilohertz
kΩ	kilo ohm
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	mega samples per second
µA	microampere
µF	microfarad
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
V	volt

Document History Page

Document Title: CYPD319X-24LDXS, USB Type-C Port Controller (Advance) Document Number: 002-23856				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	6245648	VGT	11/09/2018	New datasheet

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