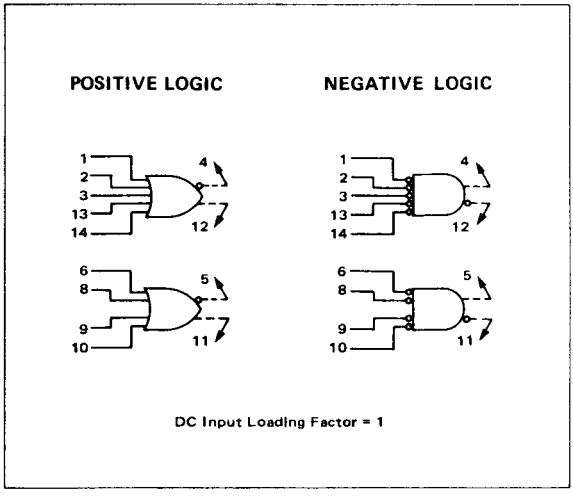
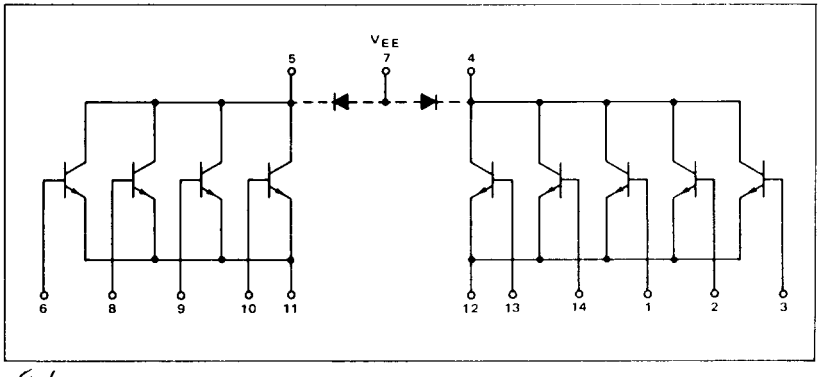
MC1025
MC1225

Dual expander arrays, with a 4-transistor array isolated from a 5-transistor array. The collectors and emitters from both arrays may be connected to form a 9-transistor array. With each base available, a 4, 5, or 9-input expander may be obtained.

Designed specifically for use with MC1024/MC1224 Dual 2-Input Gates.

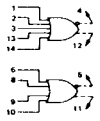


CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one expander.
The other expander is tested in the same manner.



@ All Temperatures

TEST VOLTAGE/CURRENT VALUES					
Vdc ±1.0%					mAdc
V_{EE}	V_{CC}	V_{BB}	V_{CB}	V_{BE}	I_E
-2.0	+2.0	-5.2	+0.7	+0.3	-1.33

Characteristic	Symbol	Pin Under Test	MC1225 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC1025 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{EE}	V_{CC}	V_{BB}	V_{CB}	V_{BE}	I_E	Gnd
Input Leakage Current	I_{IH}	1 2 3 13 14	-	0.5	-	0.5	-	2.0	μAdc	-	0.5	-	0.5	-	2.0	μAdc	11, 12	-	1 2 3 13 14	-	-	-	4, 5, 7
Collector Leakage Current	I_{CBX}	1 2 3 13 14	-	1.0	-	1.0	-	100	μAdc	-	1.0	-	1.0	-	15.0	μAdc	-	4, 5, 7	-	-	1 2 3 13 14	-	11, 12
Input Voltage	V_{IH}	12	-0.860	-0.810	-0.710	-0.760	-0.520	-0.570	Vdc	-0.760	-0.810	-0.710	-0.760	-0.610	-0.660	Vdc	-	-	-	4, 5	-	12	1 2 3 13 14

APPLICATIONS INFORMATION

The MC1025/MC1225 dual 4-5 input expander is designed to work with the MC1024/MC1224 expandable gate. The transistors are manufactured with the same buried layer process used on all MECL II devices and are typical of MECL II gate transistors. BV_{CEO} is 12 V or greater, $f_T \approx 600$ MHz, and β is typically from 100 to 150. An example of two 20-input NOR gates and a 40-input OR gate made from an MC1024/MC1224 expandable gate and four MC1025/MC1225 expanders is shown.

Two 20-input NOR gates and one 40-input OR gate generated using one MC1024/MC1224 expandable gate and four MC1025/MC1225 expanders.