HARRIS Semiconductor

# HIP5020

## Integrated-Power Buck Converter Controller with Synchronous Rectification

January 1997

### Features

- **High Efficiency - Above 95%**
- **Integrated N-Channel Synchronous Rectifier and Upper MOSFETs - 75mΩ Each**
- **Wide Input Voltage and Load Range**
  - **4.5VDC to 18VDC (5 to 12 NiCd Battery Cells)**
  - **Up to 3.5ADC**
- **Automatically Switches Regulation Mode**
  - **Current Mode Control for Excellent Performance at High Load Currents**
  - **Hysteretic Control for High Efficiency at Light Load Currents**
- **Flexible and Easy to Use**
  - **Ready-to-Use Example Applications**
  - **Custom Optimization with Small Components**
  - **Design and Simulation Software Available**
- **Integrated, Low-Loss Current Sensing**
- **Over-Current Protection**
- **Adaptive Dead-Time - Eliminates Shoot-Through**
- **100kHz to 1MHz PWM Switching Frequency**
- **Thermally Enhanced SOIC Package**

### Applications

- **Notebook Computers**
- **Portable Telecommunications**
- **Portable Instruments**

### Description

The HIP5020 is a high-efficiency, buck converter controller with synchronous rectification and integral power MOSFETs. Integrated current sensing eliminates the external resistor and saves power. The controller combines two methods of regulation: Current mode control for outstanding regulation response to large signal load transients, and Hysteretic mode control for high efficiency at low output currents.

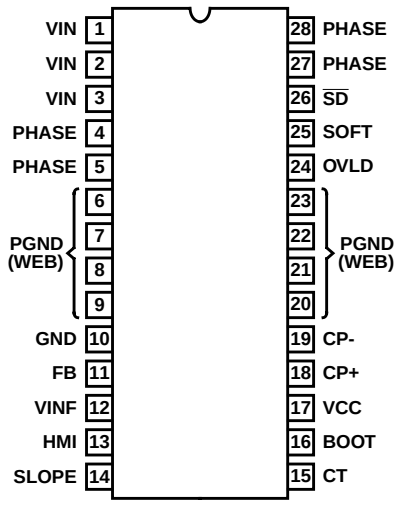
The HIP5020 controller offers a high degree of flexibility. Small components set the switching frequency, the soft-start interval and the load current boundary between Run and Hysteretic modes. These adjustments enable the designer to best optimize the trade-offs of cost, efficiency and size. The example application guide section illustrates these trade-offs with component and vendor suggestions for three circuit designs. These designs are suitable for use without modification. However, the block diagram, detailed description and HIP5020 component specifications enable further optimization to meet specific requirements

### Ordering Information

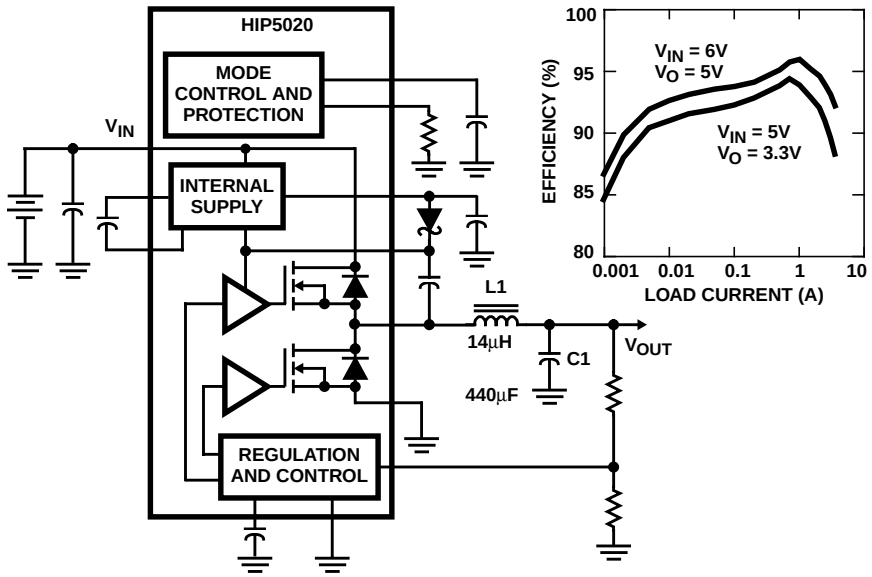
| PART NUMBER | TEMP. RANGE ($^{O}$C) | PACKAGE | PKG. NO. |
|---|---|---|---|
| HIP5020DB | 0 to 70 | 28 Ld SOIC | M28.3 |

### Pinout

**HIP5020 (SOIC)**
TOP VIEW




### Typical Application

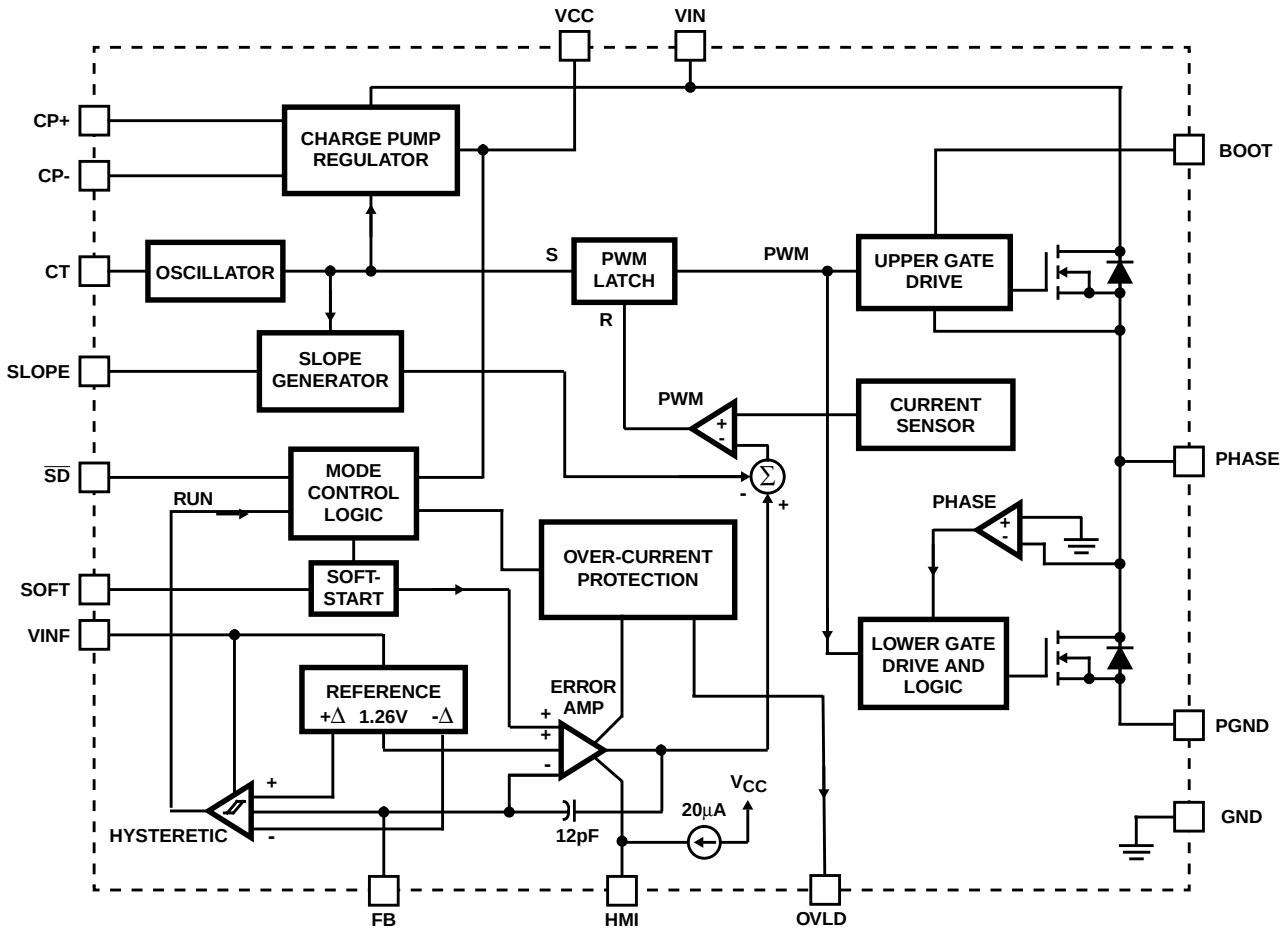



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.



File Number **4243**

## Functional Block Diagram




## Pin Description

| PIN # | DESIGNATOR | FUNCTION | DESCRIPTION |
|---|---|---|---|
| 1, 2, 3 | VIN | Input Voltage | Connection to the power source (Battery). Operates from 4.5VDC to 18VDC |
| 4, 5, 27, 28 | PHASE | Switch Node | Connect to output Inductor |
| 6, 7, 8, 9, 20, 21, 22, 23 | PGND | Power Ground | Power Return and thermal interface. Solder these pins to a large copper ground plane. |
| 10 | GND | Signal Ground | Connect to the output load return. |
| 11 | FB | Voltage Sense | A divider network scales the output voltage to 1.26VDC. |
| 12 | VINF | Filtered Input | Connect a low-pass (R-C) filter from $V_{IN}$. |
| 13 | HMI | Hysteretic Current | A resistor to the HMI pin sets the peak inductor current level during hysteretic mode. |
| 14 | SLOPE | Ramp Set | A capacitor to ground sets the compensation ramp for current mode control. |
| 15 | CT | Frequency Set | A capacitor to ground sets the oscillator frequency. |
| 16 | BOOT | Bootstrap Bias | A capacitor to Phase pin stores energy for the upper MOSFET drive. |
| 17 | VCC | Bias Voltage | Output of charge pump regulator. Use bypass capacitor to ground. |
| 18 | CP+ | Charge Pump Capacitor | Connect a capacitor between these pins for the charge pump to generate bias power. The internal charge pump inverter is synchronized to the oscillator. |
| 19 | CP- | | |
| 24 | OVLD | Over-Load | A high level on this pin signals activation of the current limit protection. |
| 25 | SOFT | Soft Start | A capacitor to ground sets the soft start interval. |
| 26 | SD | Shutdown | A low level suspends operation for a low-dissipation shutdown mode. |

## Absolute Maximum Ratings

Input Voltage, $V_{IN}$ . . . . . -0.3V to +20.0V
Supply Voltage, $V_{CC}$ . . . . . -0.3V to +20.0V
Shutdown Voltage . . . . . -0.3V to $V_{CC}$+0.3V
Voltage on PGND . . . . . -2V to +2V (Transient)

NOTE: All voltages are relative to GND, unless otherwise specified.

## Operating Conditions

Voltage Range, $V_{IN}$ . . . . . +4.5V to +18.0V
Temperature Range . . . . . .$0^oC$ to $70^oC$
Oscillator Frequency Range . . . . . 100kHz to 1MHz

## Thermal Information

| Thermal Resistance (Typical, Note 1) | $\theta_{JA}$ ($^oC/W$) |
|---|---|
| Plastic SOIC Package | 51 |
| Plastic SOIC Package (with 1$in^2$ copper) | 42 |
| Plastic SOIC Package (with 3$in^2$ copper) | 39 |

Maximum Junction Temperature (Plastic Package) . . . . . $125^oC$
Maximum Storage Temperature Range . . . . . $-65^oC$ to $150^oC$
Maximum Lead Temperature (Soldering 10s) . . . . . $300^oC$
(SOIC - Lead Tips Only)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTE:

1. $\theta_{JA}$ is measured with the component mounted on an evaluation PC board in free air.

## Electrical Specifications

$V_{IN}$ = 6.3VDC, Components referenced from Figure 1. TYP values at $T_J = 25^oC$ and MIN, MAX limits are for $T_J$ from $0^oC$ to $125^oC$; Unless Otherwise Specified

| PARAMETER | SYMBOL | TEST CONDITIONS | $T_J = 25^oC$ | $0^oC < T_J < 125^oC$ | | UNITS |
|---|---|---|---|---|---|---|
| | | | TYP | MIN | MAX | |
| **REFERENCE** | | | | | | |
| Reference Voltage | $V_{FB}$ | Total Variation, $I_O > I_{HMI}$ | 1.26 | 1.235 | 1.285 | V |
| Temperature Stability | | | - | - | 0.2 | mV |
| Hysteresis Width | $2\Delta$ | Hysteresis Mode; $I_O < I_{HMI}$ | 20 | 10 | 30 | mV |
| **MODE CONTROL LOGIC** | | | | | | |
| Under-Voltage Lockout Threshold | $VCC_{UV}$ | | 7.6 | 7.2 | 7.9 | V |
| Under-Voltage Lockout Hysteresis | $\Delta VCC_{UV}$ | | 0.3 | - | - | V |
| Shutdown Threshold | $V_{SD}$ | | 1.2 | 0.9 | 1.5 | V |
| HMI Current Source | $I_{HMI}$ | | 20 | 16 | 29 | µA |
| **POWER MOSFETs** | | | | | | |
| Drain Leakage Current | $I_{DSS}$ | $V_{DSS}$ = 20V, $V_{PHASE}$ = 0 | 0.35 | - | 10 | µA |
| On State Resistance | $r_{DS(ON)}$ | $V_{BOOT}$ - $V_{PHASE}$ = 12.6V; $I_{PHASE}$ = 2A | 75 | 60 | 125 | mΩ |
| Phase Rise and Fall Time | $t_r$, $t_f$ | $I_O$ = 2ADC | 10 | - | - | ns |
| **CHARGE PUMP REGULATOR** | | | | | | |
| $V_{CC}$ Regulation | $V_{CC}$ | $V_{IN}$ = 8.65V; $F_S$ = 100kHz; C4 = C5 = 1.0µF | 14.8 | 14.0 | 16.0 | V |
| Charge Pump Disable | $V_{INCPN}$ | | 9.8 | - | - | V |
| VCC Current - Run Mode | $I_{CC}$ | $F_S$ = 100kHz | 4 | - | - | mA |
| VINF Current - Hysteretic Mode | $I_{CC}$ - Idle | $V_{FB}$ = 5V, $V_{CT}$ = 0 | 78 | - | 110 | µA |
| VCC Current - Shutdown | $I_{CC}$ | $V_{\overline{SD}}$ = GND, $V_{IN}$ = 12V | 2 | - | 17 | µA |

**Electrical Specifications** $V_{IN}$ = 6.3VDC, Components referenced from Figure 1. TYP values at $T_J$ = 25°C and MIN, MAX limits are for $T_J$ from 0°C to 125°C; Unless Otherwise Specified **(Continued)**

| PARAMETER | SYMBOL | TEST CONDITIONS | $T_J$ = 25°C | 0°C < $T_J$ < 125°C | | UNITS |
|---|---|---|---|---|---|---|
| | | | TYP | MIN | MAX | |
| **ERROR AMPLIFIER** | | | | | | |
| Internal Integration Capacitor | | | 12 | - | - | pF |
| Open-Loop Voltage Gain | AV | | 89 | - | - | dB |
| Gain-Bandwidth Product | GBW | | 7.2 | - | - | MHz |
| Input Bias Current | $I_{FB}$ | $V_{FB}$ = 1.26VDC | 3 | -70 | 70 | nA |
| **SOFT START** | | | | | | |
| Current Source | $I_{SOFT}$ | | 10 | 6 | 14 | µA |
| **OSCILLATOR** | | | | | | |
| CT Charging Current | | | 126 | 110 | 140 | µA |
| Initial Frequency Accuracy | | | ±3 | - | - | % |
| Total Frequency Variation | | $V_{IN}$ = 4.5 to 18V | ±7 | - | ±10 | % |
| **PROTECTIVE FUNCTION** | | | | | | |
| Current Limit Threshold | $I_{O\ PK}$ | | 4.5 | 4 | - | A |
| **PWM MODULATOR** | | | | | | |
| Modulator Gain | | | 1.7 | - | - | A/V |
| Minimum On Time | | | 100 | - | - | ns |
| Minimum Off Time | | | 115 | - | - | ns |
| **HYSTERETIC COMPARATOR** | | | | | | |
| Propagation Delay | | Step $V_{FB}$ | 3 | - | - | µs |
| **SLOPE GENERATOR** | | | | | | |
| Slope Capacitor Charge Current | $I_{SLOPE}$ | | 80 | - | - | µA |

## Example Application Guide

The HIP5020 provides the flexibility to meet differing needs. This section illustrates the trade-off of component selection for three DC-DC converter circuit designs. Each circuit is optimized for a specific goal: Circuit 1 is optimized for high efficiency, Circuit 2 is optimized for small size, and Circuit 3 is optimized for low cost. Figure 1 shows the schematic common to all three converter designs. Table 1 shows the expected performance parameters for each circuit. Table 2 gives the value of each component referenced in Figure 1. Table 3 provides a listing of suggested vendors for the major (or critical) components. Figures 2, 3 and 4 show the efficiency and transient performance of each circuit.

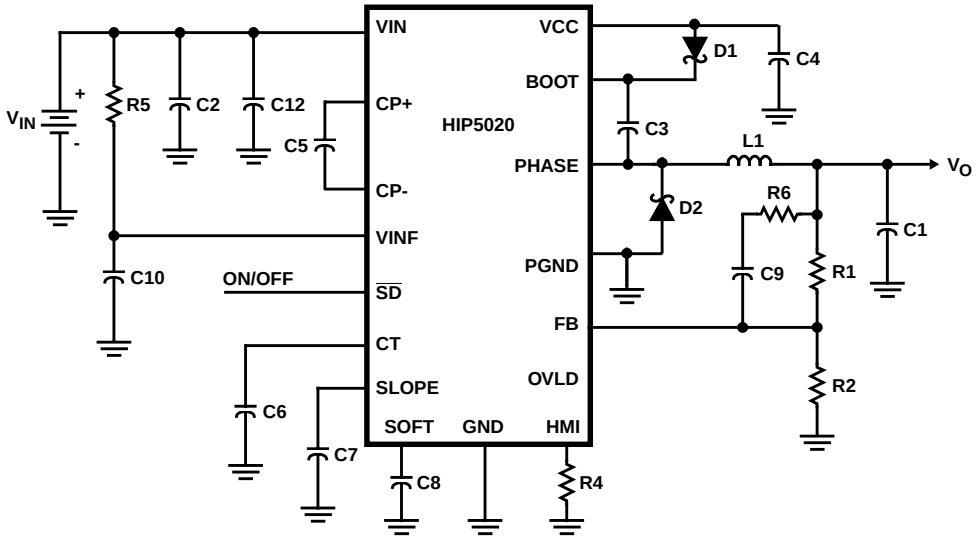



**FIGURE 1. EXAMPLE APPLICATION CIRCUIT**

**TABLE 1. EXAMPLE APPLICATION PERFORMANCE PARAMETERS**

These characteristics are for the circuit shown in Figure 1 with the components given in Tables 2 and 3.

| PARAMETER | CONDITIONS | CIRCUIT 1 HIGH EFFICIENCY | CIRCUIT 2 SMALL SIZE | CIRCUIT 3 LOW COST | UNITS |
|---|---|---|---|---|---|
| Input Voltage<br>- Typical<br>- Range | | 3 Li-Ion Cells:<br>11.1<br>8.1 to 16 | 2 Li-Ion Cells:<br>7.4<br>5.4 to 12 | 9 Nicd Cells:<br>10.8<br>8.1 to 16 | VDC |
| Switching Frequency | | 200 ±15% | 625 ±15% | 120 ±20% | kHz |
| Output Voltage Variation<br>Line Regulation<br>Load Regulation | Initial Setting<br>Input Voltage Range; $I_O$ = 1ADC<br>$I_O$ = 0.1 to 3ADC, $V_{IN}$ = Typical | 3.3 ±3.5%<br>±0.1<br>±0.3 | 3.3 ±2.2%<br>±0.1<br>±0.3 | 3.3 ±3.5%<br>±0.1<br>±0.4 | V<br>%<br>% |
| Output Voltage Ripple<br>- Full Load<br>- Light Load | Bandwidth < 20MHz<br>$I_O$ = 3ADC, $V_{IN}$ = Typical<br>$I_O$ = 50mADC, $V_{IN}$ = Typical | <br>18<br>50 | <br>30<br>80 | <br>20<br>70 | mV |
| Efficiency<br>- Full load<br>- Peak<br>- Light Load | <br>$I_O$ = 3ADC, $V_{IN}$ = Typical<br>0.5 < $I_O$ < 2ADC, $V_{IN}$ = Typical<br>$I_O$ = 50mADC, $V_{IN}$ = Typical | <br>86<br>92<br>88 | <br>86<br>89<br>84 | <br>86<br>90<br>72 | <br>%<br>%<br>% |
| Estimated Circuit Area<br>Tallest Component | | 3.5<br>0.45 | 2.1<br>0.24 | 3.6<br>0.68 | $in^2$<br>in |
| Normalized Circuit Cost | Ratio of total circuit cost to Circuit 2 | 1.1 | 1 | 0.75 | |

**TABLE 2. COMPONENT SUGGESTIONS FOR EXAMPLE APPLICATION CIRCUITS**

| COMPONENT | CIRCUIT 1 | CIRCUIT 2 | CIRCUIT 3 |
|---|---|---|---|
| D1 | MBR0540 | MBR0540 | 1N4148 |
| D2 | MBR0540 | Not Used | Not Used |
| L1 | 16µH, $R_{DC}$ < 15mΩ | 5µH, $R_{DC}$ < 22mΩ | 26µH, $R_{DC}$ < 25mΩ |
| C1 | 2x - 220µF, 10V OS-CON $ESR_{MAX}$ (100kHz) < 35mΩ | 3x - 220µF, 10V Tantalum $ESR_{MAX}$ (100kHz) < 100mΩ | 3x - 390µF, 25V, Aluminum $ESR_{MAX}$ (100kHz) < 65mΩ |
| C2 | 100µF, 20V OS-CON $ESR_{MAX}$ (100kHz) < 30mΩ | 2x - 100µF, 16V Tantalum $ESR_{MAX}$ (100kHz) < 100mΩ | 2x - 390µF, 25V Aluminum $ESR_{MAX}$ (100kHz) < 65mΩ |
| C3 | 0.1µF ±20% - Ceramic | 0.1µF ±10% - Ceramic | 0.1µF ±20% - Ceramic |
| C4 | 1µF ±20% - Ceramic | 0.22µF ±10% - Ceramic | 1µF ±20% - Ceramic |
| C5 | 1µF ±20% - Ceramic | 0.22µF ±10% - Ceramic | 1µF ±20% - Ceramic |
| C6 | 470pF ±5% - Ceramic | 150pF ±5% - Ceramic | 820pF ±10% - Ceramic |
| C7 | 680pF ±5% - Ceramic | 390pF ±5% - Ceramic | 1200pF ±5% - Ceramic |
| C8 | 0.1µF ±20% - Ceramic | 0.033µF ±10% - Ceramic | 0.01µF ±10% - Ceramic |
| C9 | 220pF ±5% - Ceramic | Not Used | Not Used |
| C10 | 0.1µF ±20% - Ceramic | 0.1µF ±20% - Ceramic | 0.1µF ±20% - Ceramic |
| C12 | 0.1µF ±20% - Ceramic | 0.1µF ±20% - Ceramic | 0.1µF ±20% - Ceramic |
| R1 | 562K ±1% | 20K (Note) | 100K ±1% |
| R2 | 348K ±1% | 12.4K (Note) | 61.9K ±1% |
| R4 | 33.2K | 37.4K | 49.9K |
| R5 | 200K | 2K | 2K |
| R6 | 49.9K | Not Used | Not Used |

NOTE: Both resistors available in one SOT-23 from California Micro Devices part # PAC27A01

**TABLE 3. SUGGESTED SUPPLIERS**

| COMPONENT | SUPPLIER | PHONE NUMBER | COMPONENT | SUPPLIER | PHONE NUMBER |
|---|---|---|---|---|---|
| Capacitors - Aluminum and Os Con | Sanyo | 501-633-5030 | Inductors - OCTA-PAC | Coiltronics | 407-241-7876 |
| Capacitors - Aluminum and Ceramic | Panasonic | 0774-32-1111 | Inductors - | Pulse Engineering | 619-674-8100 |
| Capacitors - Tantalum and Os Con | Sprague | 207-324-4140 | Inductors - | GB International | 607-785-1109 |
| Capacitors - Ceramic and Tantalum | AVX | 207-282-5111 | Magnetic Cores - Powdered Iron | Micrometals | 714-630-7420 |
| Capacitors - Aluminum | United Chemi-Con | 708-696-2000 | Magnetic Cores - Kool Mu | Magnetics | 412-282-8282 |
| | | | Magnetic Cores - Microlite | AlliedSignal Inc. | 201-581-7653 |

## Typical Performance Curves

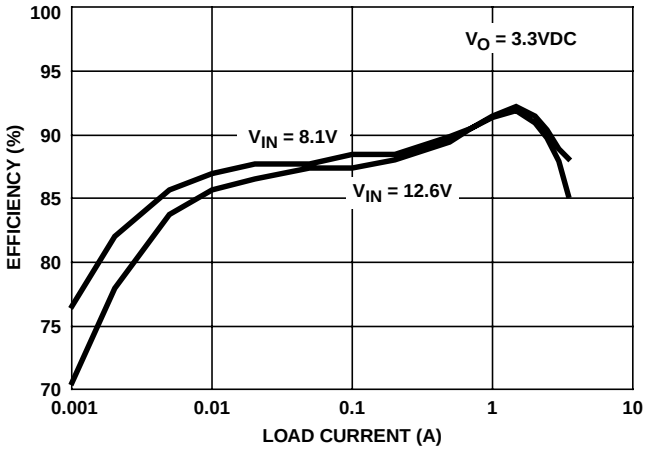



FIGURE 2A.

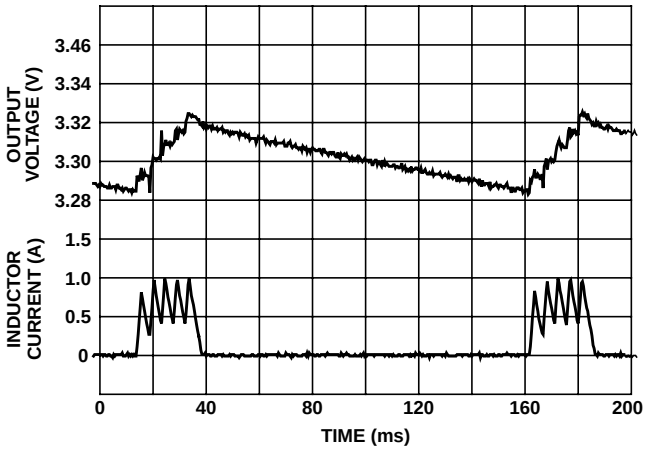



FIGURE 2B.

FIGURE 2. HIGH-EFFICIENCY CIRCUIT 1 MEASURED PERFORMANCE EFFICIENCY vs LOAD CURRENT AND HYSTERETIC MODE OPERATION ($V_{IN}$ = 11.1VDC, LO = 0.1ADC

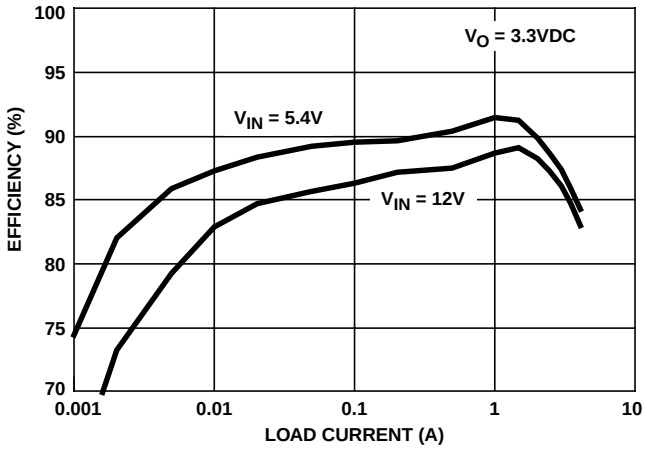



FIGURE 3A.

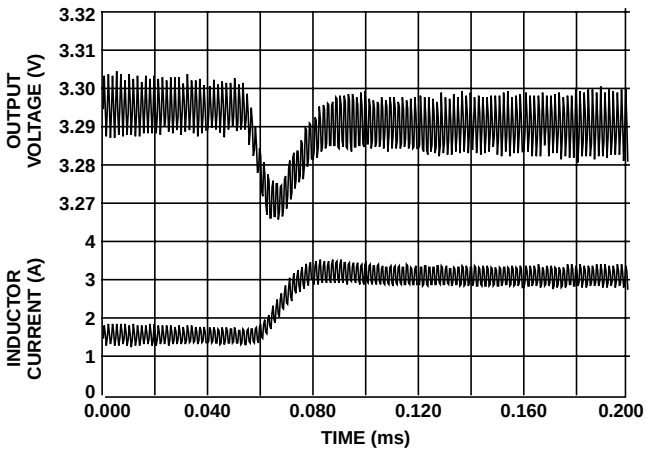



FIGURE 3B.

FIGURE 3. SMALL-SIZE CIRCUIT 2 MEASURED PERFORMANCE EFFICIENCY vs LOAD CURRENT AND 50% TO FULL LOAD TRANSIENT (1A/μs)

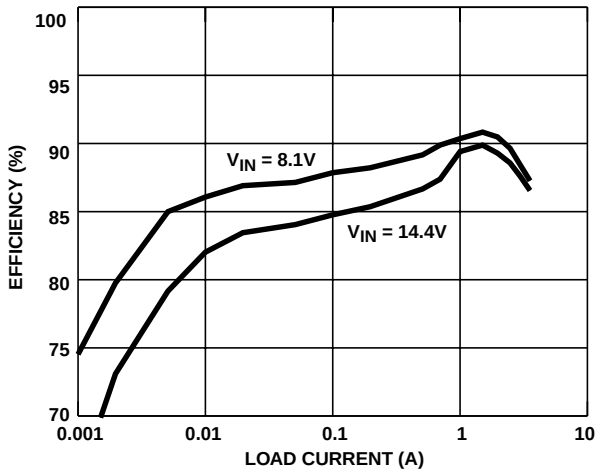



FIGURE 4A.

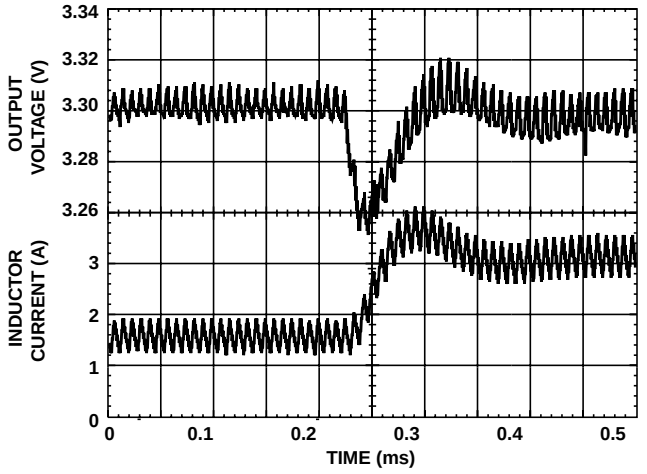



FIGURE 4B.

FIGURE 4. LOW-COST CIRCUIT 3 PERFORMANCE PREDICTIONS EFFICIENCY vs LOAD CURRENT AND 50% TO FULL LOAD TRANSIENT (100A/ms)

# Design Information

The HIP5020 is optimized for battery power systems with a 4.5V to 18V input. The integrated MOSFETs along with an LC output filter form a synchronous rectified, step-down (buck) converter. The output is regulated at high output current by peak-current-mode PWM control. At light loads, the control automatically transitions to hysteretic mode to regulate the output.

## Detailed Operating Description

The following description refers to symbols and components in the functioal Block Diagram and Figure 1. Figure 1 shows the HIP5020 in a DC/DC converter.

### Operating Modes

The HIP5020 has 4 modes of operation; Shutdown, Start-up, Run and Hysteretic modes. The controller draws only 2µA from the input supply in the Shutdown mode. This mode is activated when the $\overline{SD}$ pin is high. The controller enters the Start-up mode by releasing the $\overline{SD}$ pin, and the charge pump turns-on to increase $V_{CC}$ above the under-voltage lockout threshold. In the Start-up mode, the voltage on the SOFT pin increases at a rate set by the capacitor on the SOFT pin. The SOFT voltage limits the rate-of-rise of output voltage. The output voltage is regulated with peak current control in the Run mode at high output current. For low output currents, the controller automatically transitions to Hysteretic mode for output regulation. In this mode, the hysteretic comparator cycles the control on (RUN = High) and off (RUN = Low) as a function of the output voltage level. When off (RUN = Low), bias power is removed from most of the control's functions (only the reference and hysteretic comparator operate with RUN = Low). The converter replenishes the output capacitor charge with short duration power cycles (RUN = High) and the converter dissipates very little average power. A resistor (R4) programs the load current boundary (HMI) between the Run and Hysteretic modes.

### Run Mode

The HIP5020 operates in Run mode at high output currents. Each clock cycle of the oscillator sets the PWM Latch and turns-on the high side MOSFET (See the Functional Block Diagram). The current sensor supplies a voltage proportional to the current in the high side MOSFET. The PWM Comparator resets the PWM latch once the current signal exceeds the summation of the error amplifier and slope signals. The upper MOSFET turns off and the PWM latch enables the lower gate drive and logic. The current in the output inductor continues to flow, reducing the PHASE voltage (by displacing charge on the capacitances of the PHASE pin). The lower MOSFET turns-on after the voltage on the PHASE pin falls to ground as monitored by the phase comparator. The lower MOSFET remains 'on' for continuous output inductor current until the next cycle. For discontinuous inductor current operation, the phase comparator signals the lower gate drive to turn-off the lower MOSFET when the inductor current reaches zero by monitoring the phase voltage ($r_{DS(ON)}$ * I).

The HIP5020 regulates the output voltage with peak-current PWM control in Run mode. The peak-current-mode feedback, the MOSFETs and output inductor, L1 are all parts of the peak-current control loop. An outer voltage regulation loop then programs the peak current to the level required.

When averaged over many switching cycles, the entire peak-current control loop can be simplified and described as a voltage controlled current source. Figure 5 shows a simplified diagram of this operation. The current source supplies the output capacitor and load. The outer voltage regulation loop consists of an error amplifier and compensation components. The error amplifier programs the inductor current (as described above) to the value required to regulate the output voltage. Both the error amplifier and hysteretic comparator monitor the feedback (FB) pin. During the Run mode, the feedback node voltage ($V_{FB}$) is held to the reference voltage (REF) by the voltage feedback loop. $V_{FB}$ is related to $V_O$, R1 and R2.

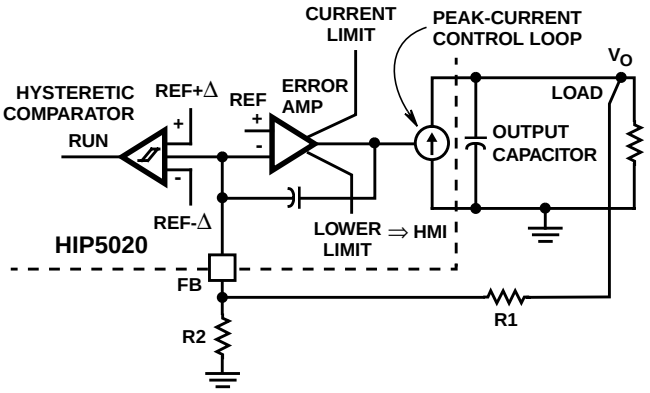



**FIGURE 5. SIMPLIFIED DIAGRAM OF OUTPUT VOLTAGE REGULATION AND MODE SWITCHING**

Limiting the error amplifier output voltage range provides both current-limit protection and a mechanism for setting the load current boundary between the Run and Hysteretic modes. Figure 6 shows the modes of operation as a function of the error amplifier output and load current. The error amplifier output voltage tracks the inductor current. The upper error amplifier clamp limits the peak inductor current which reduces the pulse-width (or duty factor). This reduces the output voltage with a constant current characteristic. The lower error amplifier limit sets the minimum inductor current. For load current demand below the minimum inductor current, the excess current adds charge to the output capacitor and the output voltage increases. The voltage on the feedback (FB) pin also increases and the converter operates in Hysteretic mode. The lower error amplifier limit is the voltage on the HMI (Hysteretic Mode Current) pin. The HMI level ($V_{HMI}$) sets the Run-to-Hysteretic mode load current boundary.

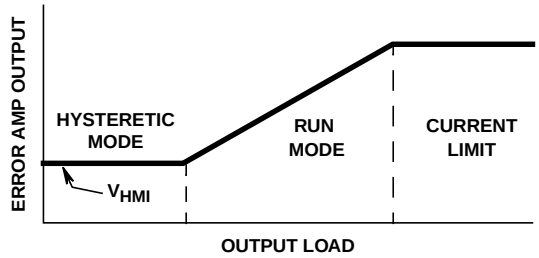



**FIGURE 6. OPERATING MODES WITH THE ERROR AMPLIFIER CLAMPS**

### Hysteretic Mode

The HIP5020 operates in the hysteretic mode with low output current. In this mode, the hysteretic comparator cycles the control on (RUN = High) and off (RUN = Low) as a function of the output voltage and the FB voltage level. Figure 7 illustrates the averaged Hysteretic Mode operation with reference to Figure 5. At light load, the error amplifier output voltage is held to the HMI voltage ($V_{HMI}$). This level commands an inductor current that exceeds the load current. The excess current flows into the output capacitor which increases the output voltage ($V_O$). The voltage feedback loop no longer holds $V_{FB}$ at the reference voltage. When $V_{FB}$ increases to the Upper Hysteretic Trip Level, the RUN signal transitions Low to power-down most of the control's functions, and the load is supplied by the output capacitor. After $V_{FB}$ (and the equivalent output voltage) drops below the Lower Hysteretic Trip Level, RUN transitions High, turning on the controller. The converter replenishes the charge on the output capacitor (C1). This cycle repeats to regulate the output voltage.

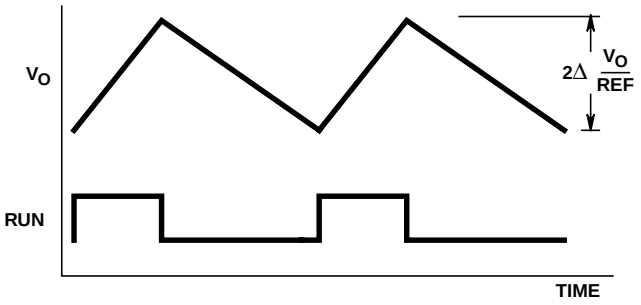



**FIGURE 7. TYPICAL HYSTERETIC MODE OPERATION**

The HIP5020 maintains peak-current control during Hysteretic mode. When the RUN signal transitions High, the control functions reenergize and the oscillator sets the PWM Latch which turns-on the high side MOSFET. The inductor current increases and resets the PWM latch to turn off the MOSFET. This cycle-by-cycle operation is identical to the Run mode operation. However, in hysteretic mode, the inductor current is regulated to a level proportional to $V_{HMI}$. With very light loads, the converter replenishes the output capacitor charge in a few switching cycles (RUN = High) and the converter dissipates very little average power. Operation automatically transitions to Run mode as the load increases above the Run-to-Hysteretic mode load current boundary; the RUN signal simply stays High.

The output voltage ripple during Hysteretic Mode is a function of the HMI (Hysteretic Mode Current) setting, output capacitor ESR, and the hysteretic voltage trip points. The approximate ripple voltage is:

$$V_{HMI} \bullet 1.7 \bullet ESR + 2 \bullet \Delta \bullet (R_1 / R_2 + 1)$$

Where $2\Delta$ is the hysteresis width (~20mV) and the 1.7 (A/V) factor is the error amplifier output voltage to peak current control gain (modulator gain).

### Protective Modes

The HIP5020 provides cycle-by-cycle current limiting and protects against over-current. The cycle-by-cycle current limit reduces the pulse width (duty factor) for peak inductor current levels exceeding the current limit (4A minimum). This results in a constant current output characteristic. The OVLD pin toggles high to indicate an overload condition. Should the current limit cause a small pulse width due to a saturating output inductor, over-current protection activates a soft-start cycle. The simultaneous occurrence of a minimum pulse width and a current limit signals an over-current condition. The converter enters the start-up mode by fully discharging the soft-start capacitor and inhibiting PWM operation. With a continuous overload, the over-current protection triggers the soft-start function which inhibits PWM operation until after the soft-start capacitor first fully charges to $V_{CC}$ and then fully discharges. This results in a very low average input current.

### Soft-Start

The soft-start function is programmed by a capacitor on the SOFT pin (C10). This capacitor is initially discharged. Releasing the SD pin, or increasing $V_{CC}$ above the undervoltage lockout threshold initiates a soft-start interval. As the internal 10µA source charges C10, the converter output follows the capacitor voltage, $V_{SOFT}$. The control establishes closed loop regulation when the output voltage approaches the level set by R1, R2 and the reference.

Initiating shutdown mode rapidly discharges capacitor C10. Releasing the SD pin initiates another start-up mode which charges up the capacitor C10 to $V_{CC}$.

Should the $V_{FB}$ exceed the upper hysteretic trip level, the internal 10µA source stops charging $C_{10}$. The soft-start interval will resume when $V_{FB}$ drops below the lower hysteretic trip level.

## Detailed Component Selection

The application circuits shown in Figure 1 and described by Tables 1 and 2 illustrate component trade-off to achieve size, cost and efficiency goals. A design and simulation software program is available that simplifies the small signal component selection (http://www.semi.harris.com). This section provides additional guidance for selecting alternate components.

### Output Capacitor

The output capacitor, C1 smooths the output voltage ripple of the DC-DC converter. The size and value depend upon the output ripple requirement, the dielectric characteristics, the value of output inductance and the switching frequency. Choose a capacitor with a low impedance at the switching frequency to meet the output voltage ripple requirement. Use only specialized low-ESR capacitors intended for switching-regulator applications.

Capacitor impedance above the switching frequency should also be minimized. During Hysteretic mode operation, the transition of RUN from low to high causes inductor current to ramp from zero to the HMI set level in a very short time. This rate of current change across the output capacitor's the equivalent series inductance (ESL) causes a voltage spike that appears (attenuated) on the FB pin. The ESL or the rate of current change must be limited to prevent the hysteretic comparator from toggling RUN between high and low. Unfortunately, ESL is not a specified parameter. Work with your capacitor supplier and measure the capacitor's impedance at the switching frequency (and the first few harmonics of the switching frequency) to select a suitable component. In most cases, multiple electrolytic capacitors of small case size perform better than a single large case capacitor.

### Output Inductor

The output inductor, L1 sets the ripple current and influences the converter efficiency. The ripple current, $\Delta I$ is related to the inductance and switching frequency ($F_S$), for continuous inductor current. Increasing the inductance or the switching frequency lowers the ripple current and the output ripple voltage. The inductance can be determined by:

$$L1 = \frac{V_{IN}-V_O}{\Delta I \bullet F_S} \bullet \frac{V_O}{V_{IN}}$$

Inductance is a function of the core permeability, core size, and the square of number of turns. The power dissipation of the inductor is also dependent upon the number of turns and the core. In general, most of the power dissipation is in the inductor's winding. Therefore, use high permeability core material to minimize the number of turns. Be sure the flux at full load current does not saturate the core. Recommended core materials include: Microlite™ from Allied Signal, ferrite, Kool-Mu™, molypermalloy (MMP), and powdered iron.

### Switching Frequency

The oscillator produces a sawtooth wave on the CT pin with an amplitude of 1.26V. The switching frequency is set by C6. Select the closest standard capacitance value according to the following formula:

$$C6 = \frac{10^{-4}}{F_S} - 10^{-11}$$

Higher switching frequency decreases the size of output filter L1 and C1 and enables a higher bandwidth converter for faster response to a load transient. However, higher frequencies dissipate more power for a less efficient converter.

### Control Loop Design

The HIP5020 realizes excellent transient response with proper control loop design. The device utilizes peak-current control with the entire current loop integrated within the HIP5020. Additionally, the HIP5020 includes a 12pF integration capacitor across the error amplifier. (See the Detailed Operating Description above.) Some applications need only add the resister R1 and capacitor C7 for a complete design.

The capacitor, C7 adds a compensation slope to the peak current control loop (see Slope Compensation below). C7 shows up in the closed loop transfer function as peaking around half of the switching frequency. For a stable design, make sure the closed loop gain at half of the switching frequency is below -10dB.

The error amplifier and compensation components regulate the output voltage by controlling the current loop (as shown in Figure 5). The compensation components shown in Figure 8 realize a lead-lag circuit. The resistor R1 adjusts the loop gain of the converter and resistor R6 and capacitor C9 set the pole and zero. The resistor R2 does not appear in the lead-lag transfer function. R2 sets the output voltage level. First stabilize control loop by selecting R1 and then determine R2 for the desired output voltage level.

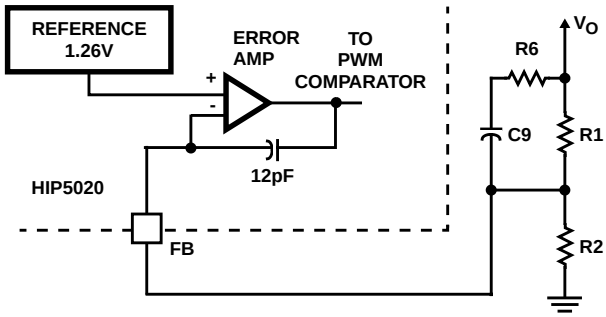



**FIGURE 8. LEAD-LAG COMPENSATION CIRCUIT**

Using the built-in 12pF integration capacitor across the error amplifier, the transfer function, G(s) for the lead-lag network is:

$$G(s) = \frac{K}{s} \bullet \frac{1 + s/\omega_z}{1 + s/\omega_p}$$

$$\text{where } K = \frac{1}{R1 \bullet 12 \bullet 10^{-12}}$$

$$\omega_z = \frac{1}{(R1 + R6) \bullet C9}$$

$$\text{and } \omega_p = \frac{1}{R6 \bullet C9}$$

The HIP5020 design and simulation software (available at the Harris WEB site) computes these values and greatly simplifies the following compensation design process. To design a DC-DC converter for stable operation:

1) Determine the output capacitor's ESR zero frequency, $f_{ESR}$ which is given by: $1/(2 \bullet \pi \bullet C1 \bullet ESR)$
2) Place the compensation pole ($\omega_p/2\pi$) at the ESR zero frequency, $f_{ESR}$.

Microlite™ is a trademark of Allied Signal

Kool-Mu™ is a trademark of Spang Company

3) Determine the desired converter bandwidth (or the frequency where the loop gain is unity). Bandwidth must be below 1/2 the switching frequency. A reasonable bandwidth is approximately 1/10 the switching frequency.
4) Select the compensation zero ($\omega_Z$) well below the desired bandwidth frequency and adjust as necessary to achieve the desired phase margin ($40^o$ Minimum).
5) Adjust the gain (via R1) and iterate the compensation zero and gain as needed to achieve the desired bandwidth and phase margin.
6) Measure the closed-loop transfer function at both minimum and maximum input voltage and at both full load and the Run-to-Hysteretic mode load current boundary.

Be sure to note the phase margin and the gain margin.

The single component R1 can compensate the control loop if the detailed characteristics of the output capacitor, bandwidth, and switching frequency meet strict requirements. The bandwidth (or unity gain frequency) must be much greater than the ESR zero frequency ($f_{ESR}$) and much less than twice the switching frequency. Additionally the break frequency of output capacitor's ESL must be much greater than the switching frequency. If these conditions exist, the ESR zero provides the necessary phase boost. However, note that the ESR is not a well controlled parameter and is variable with temperature and aging. Select R1 for the proper compensation gain and confirm the selection with closed-loop measurements. Additionally determine the worst case ESR variation and estimate this effect on converter stability.

### Output Voltage Setting

The resistor divider R1 and R2 sets the output voltage as a function of the reference voltage. Select R1 to achieve the desired bandwidth then determine R2 from:

$$R2 = R1 \bullet \frac{1.26}{V_O - 1.26}$$

The output voltage regulation improves with the use of integrated resistor network. By integrating the resistors, the variations of R1 track the variations of R2. The ratio of R1 to R2 remains constant and this minimizes the output voltage variation to improve regulation. Integrated resistor networks are available in small SOT-23 packages such as the one used in Circuit 2.

### Slope Compensation

Slope compensation is necessary to avoid current loop instability for duty ratios above 50%. Select C7 to set the amount of slope compensation according to the following:

$$C7_{MAX} = \frac{L1 \bullet 272 \bullet 10^{-6}}{V_O}$$

This value of capacitance provides a compensation ramp that is 1/2 of the reflected output inductor decreasing current slope.

### Charge Pump and Bootstrap Design

The charge pump and bootstrap circuit supply the internal bias power for the HIP5020. The majority of the bias power goes to gate drives. The charge pump operates at the switching frequency for input voltage below 9.8V. Select capacitors $C_4$ and $C_5$ according to the following:

$$C4, C5_{MIN} = \frac{0.088}{F_S} + 0.12 \bullet 10^{-6}$$

The gate of the upper N-channel MOSFET is driven above the input voltage by the internal gate drive with power supplied by the bootstrap circuit D1 and C3. A fast recovery, low leakage diode is recommended for D1. C3 should be a high quality ceramic capacitor.

### Hysteretic Mode Current Setting

The voltage on the HMI pin sets the load current boundary between Run mode and Hysteretic mode. This setting enables the designer to trade-off efficiency and output voltage ripple at low output current. The output voltage ripple is higher in Hysteretic mode as compared with Run mode. Many systems can tolerate higher power supply ripple at light loads because the reduced load induced ripple. The designer should select the load current boundary based upon converter efficiency characteristics and known load characteristics. For example, a HIP5020 converter powering a microprocessor load might select the HMI boundary between the sleep and active states of operation.

The ripple voltage is highest for load current just below the mode boundary. The ripple voltage is a function of the hysteresis width, the resistors R1 and R2, the hysteretic current setting (HMI) and the output capacitor ESR as described in the Hysteretic Mode section.

Figure 9 shows the efficiency versus load for two different $V_{HMI}$ settings. The efficiency at light load current is higher with a higher settings. The efficiency at light load current is higher $V_{HMI}$ setting. However, the more efficient design has a higher ripple voltage for load current between 0.2A and 0.6A. If the load is sensitive to power supply ripple during this load range, the lower efficiency HMI setting should be used.

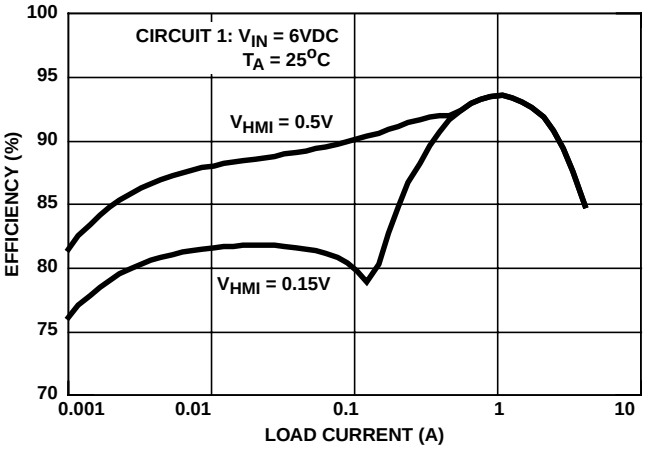



**FIGURE 9. EFFICIENCY vs LOAD CURRENT**

The voltage on the HMI pin is used to clamp the lower limit of error amplifier output voltage and the minimum peak inductor current. This voltage is set by a 20µA current source and the resistor, R4.

### Soft-Start

Set the Soft-Start capacitor, C8 so that the output voltage ramps to its final value with a current between the hysteretic mode current and the rated current. The minimum value for C8 can be determined from:

$$C8_{MIN} = T_{SOFT} \bullet \frac{10^{-5}}{V_{REF}}$$

$$\text{where } T_{SOFT} = \frac{C1 \bullet V_O}{3A}$$

Larger values for C8 will extend the soft-start interval, $T_{SOFT}$. Any loading during the Start-up mode lengthens $T_{SOFT}$.

### Bypass and Filter Capacitors

Capacitor C12 supplies the leading edge PWM current each switching cycle. A high quality (X7R dielectric ceramic) 0.1µF surface-mount capacitor is recommended. Locate C12 directly across the VIN and PGND pins.

Bypass the internal $V_{CC}$ supply with a high quality (X7R dielectric ceramic) surface-mount capacitor (C4). Locate C4 directly across the VCC and GND pins.

The value for capacitor C5 should be selected as described in the Charge Pump Regulator above. A single high quality (X7R dielectric ceramic) capacitor is usually adequate. Some applications may need a high capacitance, electrolytic for charge-pump operation. For these applications, a high quality capacitor in parallel with the electrolytic is recommended. Locate C5 directly across the CP+ and CP- pins.

R5 and C10 form a low-pass filter for the bias supply ($V_{INF}$) of the reference and hysteretic comparator functions. A 2kΩ resistor for R5 and a 0.1µF Capacitor for C10 is recommended. Locate C10 directly across the VINF and GND pins.

### Thermal Design

The power ground (PGND) pins of the SOIC package provide a thermal conduction path for removing heat from the HIP5020. Inside the package, the HIP5020 die is mounted on a copper structure with connections to PGND (pins 6, 7, 8, 9, 20, 21, 22, and 23). Solder the SOIC to a circuit board with a copper ground plane to remove heat from the package. With good component layout and 3 square inches of copper ground plane, the junction-to-ambient thermal resistance is 36$^{O}$C/W. Most of the converter's power dissipation will be in the HIP5020 and the output inductor, L1. The power dissipated in the HIP5020 can be estimated from the converter's full load efficiency and subtracting the inductor's power dissipation ($I_O^2 \bullet R_{DC}$). The junction temperature rise above ambient is this power multiplied by the thermal resistance. Use the HIP5020 design and simulation software for more accurate thermal simulations. Be sure to keep the junction temperature below 125$^{O}$C for reliable operation. Careful component layout and good thermal design maximized the efficiency and reliability of the converter.

## Detailed Characteristics

### Charge Pump Regulator

The charge pump regulator supplies control power ($V_{CC}$) to the internal functions of the HIP5020. The charge pump operates for input voltage levels below 9.8V and is disabled for input voltages above 9.8V. Figure 10 shows the charge pump output voltage ($V_{CC}$) as a function of the input voltage ($V_{IN}$). For input voltages below 9.8V nominally, the charge pump operates in two regions - as a voltage doubler and as a voltage regulator. The charge pump operates as a normal voltage doubler when $V_{CC}$ is below approximately 14.8V. The charge pump limits $V_{CC}$ to approximately 14.8V in the regulation region. For input voltages above 9.8V, the charge pump is disabled and $V_{CC}$ follows the input voltage less a diode drop.

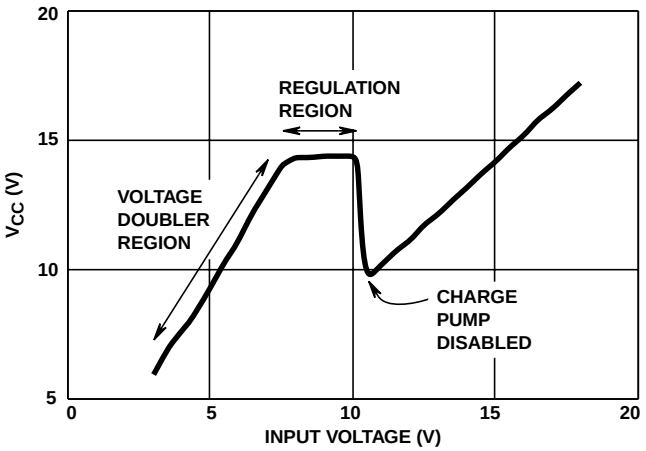



**FIGURE 10. CHARGE PUMP REGULATOR INPUT VOLTAGE CHARACTERISTICS**

The charge pump can be used to supply current for external loads on the VCC pin. Figure 11 shows the regulation characteristics of the charge pump in the various operating regions. These characteristics are for a DC-DC converter (Circuit 3) operating at 100kHz and with 1µF capacitors for C4 and C5.

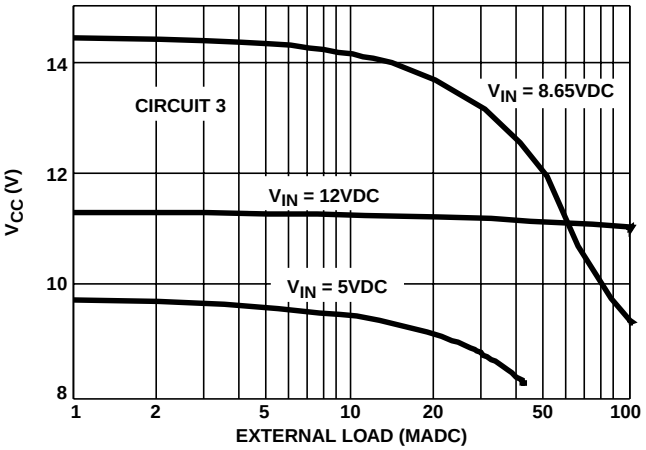



**FIGURE 11. BIAS VOLTAGE ($V_{CC}$) vs EXTERNAL LOAD CURRENT**

The charge pump may not be suitable for some applications and external loads. Be sure that the load can tolerate the $V_{CC}$ voltage variation with input voltage. During Hysteretic Mode, the external load should be removed when the converter turns off. Note that the charge pump and oscillator are disabled with RUN low (see Operating Modes). The external load could cause an under-voltage lockout trip and subsequent soft-start cycle.

### Light Load Power Dissipation

The converter efficiency and power dissipation at light load is mainly a function of the bias supplied to the HIP5020. Figure 12 shows the input current as a function of the input voltage for the two states of the RUN signal. $I_{IN}$ is summation of both the current into the VIN and VINF pins. The curve for $I_{IN}$ with the RUN signal High does not include the gate drive power.

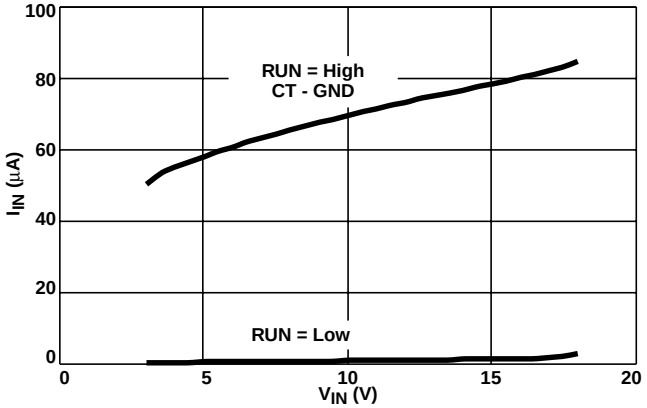



**FIGURE 12. BIAS POWER CHARACTERISTICS**

The gate drive power is a function of the MOSFETs gate charge, voltage and switching frequency. Figure 13 shows the combined gate energy required by the internal MOSFETs with the charge pump characteristics. To determine the total bias power:

1) Multiply the value in Figure 13 by the switching frequency.
2) Add the product of the voltage and current from the RUN = High curve in Figure 12.
3) Multiply by the ratio of RUN time to the Hysteretic period.
4) Add the product of the voltage and current from the RUN = Low curve in Figure 12.

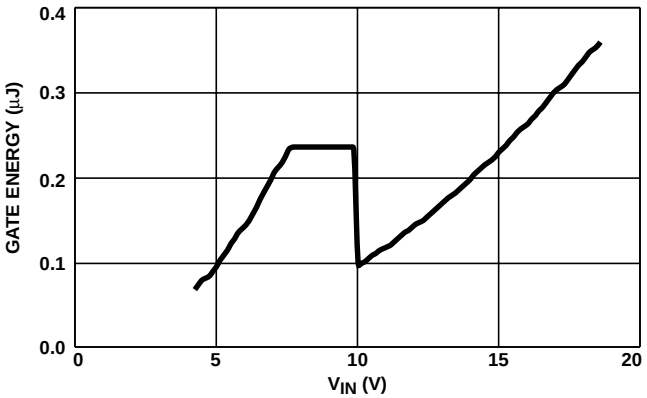



**FIGURE 13. MOSFET GATE ENERGY CHARACTERISTICS vs INPUT VOLTAGE**

### MOSFET On-Resistance

Conduction losses are a significant portion of the power dissipation in a DC-DC converter. The HIP5020 conduction losses are the product of the square of the average output current and the MOSFET on-resistance - $r_{DS(ON)}$. The $r_{DS(ON)}$ of the MOSFETs is a function of $V_{CC}$ and junction temperature. $V_{CC}$ changes with the input voltage as shown in Figure 10 above. Figure 14 shows the maximum $r_{DS(ON)}$ of both MOSFETs as a function of input voltage for a junction temperature of $25^oC$. The junction temperature of the HIP5020 also effects $r_{DS(ON)}$. Figure 15 shows the $r_{DS(ON)}$ as a function of temperature for three gate voltage levels. The $r_{DS(ON)}$ can be estimated at a given input voltage and junction temperature as follows:

1) Assume that the gate voltage is equal to $V_{CC}$. Find the gate voltage at $25^oC$ from Figure 10.
2) Multiply this number by the $r_{DS(ON)}$ shown in Figure 15. Interpolate as necessary.

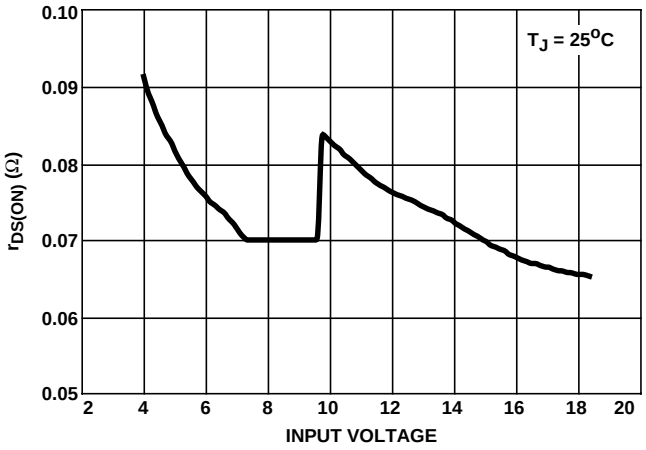



**FIGURE 14. $r_{DS(ON)}$ vs INPUT VOLTAGE**

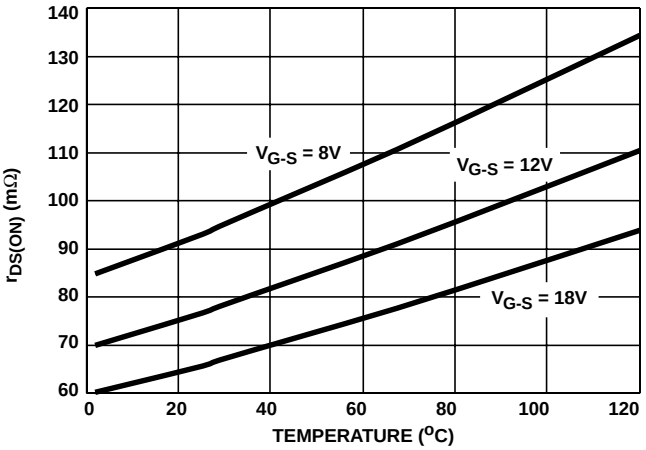



**FIGURE 15. $r_{DS(ON)}$ vs JUNCTION TEMPERATURE**

## Application Hints

### Short Duration RUN Interval

Some converter designs may observe a series of short run interval pulses (RUN = High) in hysteretic mode that can reduce the light-load efficiency. The run interval is interrupted by the voltage on the FB pin crossing over the Upper Hysteretic Trip Level before the output capacitor gains sufficient charge. This operation can be caused by a number of factors:

1) Poor physical layout. Use wide traces to connect the power components.
2) Poor component choice. Use only power supply specific electrolytic capacitors. Additionally use ceramic capacitors in parallel with the bulk electrolytic capacitors.
3) Sudden voltage excursions across the output capacitor and the error amplifier output.

Be sure to clear up any layout problems first. Poor layout not only causes efficiency problems, but can be a source of noise for surrounding circuits. If the short run interval is still observed, a capacitor can be added across each R2 and R4.

During the transition of RUN from low to high, the voltage on the FB pin starts at the Lower Hysteretic Trip Level. The error amplifier activates and its output slews to $V_{HMI}$. This causes an increase in $V_{FB}$ due to current in the compensation capacitor. Adding a capacitor across R4 slows the rate of HMI voltage increase during the transition of RUN from low to high and decreases error amplifier slew rate.

Voltage excursions across the output capacitor and circuit board traces after the transition of RUN from low to high results in an increase in $V_{FB}$. As the inductor current ramps to the HMI level, the output voltage increases due to the output capacitor's ESR and ESL. This voltage spike is attenuated by the resistor divider, R1 and R2 but still appears on the FB pin. A small capacitor across R2 further attenuates any output voltage spikes. The small capacitor eliminates the short duration RUN interval, but will not reduce the output voltage spikes. A better solution may be a better, higher quality output capacitor with low ESR and ESL.

### Bootstrap and Phase Diodes

The bootstrap function requires a diode D1 to supply gate drive power for the upper N-channel MOSFET. A Schottky is recommended for most applications due to its fast switching speed and low forward voltage. A fast-recovery diode can be used in low switching frequency, cost sensitive applications.

Many applications will not need a Schottky diode from phase to ground. The internal body diode of the integrated MOSFET is sufficiently fast. A small Schottky diode can be added to improve the light load efficiency. This diode only conducts during the short intervals (< 50ns) before and after the lower MOSFET conducts. In most cases, a Schottky ratted for 0.5A is sufficient.