MPQ7221

16-Channel, 80mA/Ch, LED Driver with Separated PWM Analog Dimming and I²C Interface, AEC-Q100 Qualified

DESCRIPTION

The MPQ7221 is a 16-channel LED driver that operates across a wide 4.5V to 16V input voltage (V_{IN}) range. The MPQ7221 applies 16 internal current sources in each LED string terminal. The LED current (I_{LED}) of each channel is set by an external current-setting resistor, with a maximum current up to 80mA.

The MPQ7221 integrates an I²C interface, where 10 different I²C addresses are configurable via an external resistor. This allows the MPQ7221 to support up to 10 cascaded devices to drive the LED array. Each channel can be enabled or disabled via the I²C.

The MPQ7221 employs separated pulse-width modulation (PWM) dimming and analog dimming for each LED channel. Each channel uses 12-bit resolution PWM dimming and 6-bit analog dimming. The I_{LED} ramp rate and phase shift can be configured to optimize the EMI and EMC performance.

The MPQ7221 can output a refresh signal from the RFSH/FLT pin, with the refresh signal frequency set via a register. Full protections include open-load protection, short-load protection, and over-temperature protection (OTP). If any of the protections is triggered, then the fault indicator is pulled low and the corresponding fault register is set.

The MPQ7221 is available in a QFN-24 (4mmx4mm) package, and is AECQ-100 qualified.

FEATURES

- Easy Scalability:
  - 16 Channels, 80mA/Channel Max
  - 10 Addresses Configurable via an External Resistor
- I²C Control:
  - I²C Interface
  - 6-Bit Analog Dimming for Each Channel
  - 12-Bit Pulse-Width Modulation (PWM) Dimming for Each Channel
- Optimized for EMI and EMC:
  - Selectable PWM Dimming Frequency (f_{PWM}): 220Hz, 250Hz, 280Hz, and 330Hz
  - Configurable LED Current (I_{LED}) Slew Rate
  - 40μs Phase Shift
- Full Protection Features:
  - Fault Indicator
  - LED Open Protection
  - LED Short Protection with Configurable Threshold
  - Under-Voltage Lockout (UVLO)
  - Over-Temperature Protection (OTP)
- Additional Features:
  - 4.5V to 16V Wide Input Voltage (V_{IN}) Range
  - Refresh Signal Output
  - I_{LED} Configured by an External Resistor
  - Available in a QFN-24 (4mmx4mm) Package with Wettable Flanks
  - Available in AEC-Q100 Grade 1

APPLICATIONS

- Automotive Taillights
- Automotive Turning Lights

TYPICAL APPLICATION

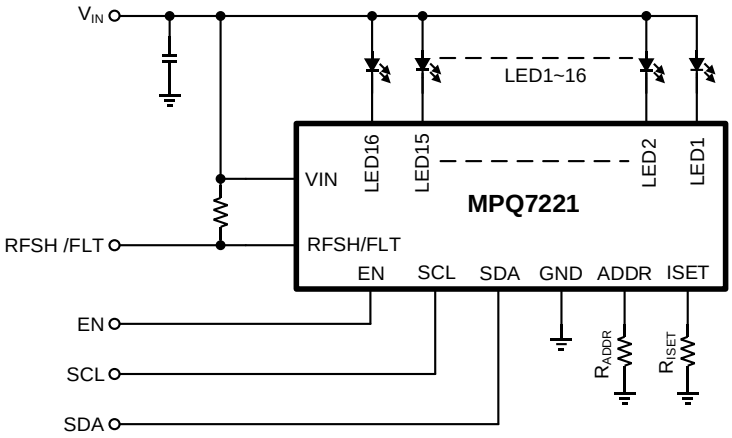


Figure 1: Typical Application Circuit

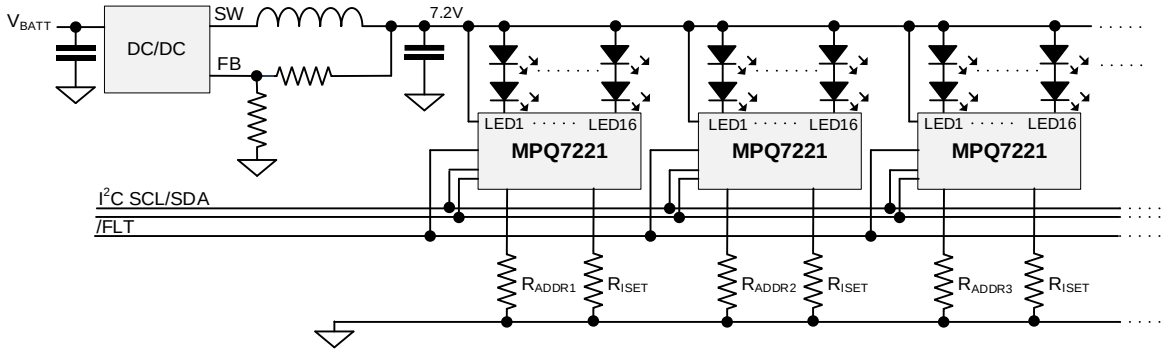


Figure 2: System Application Circuit with 2 LEDs in Series

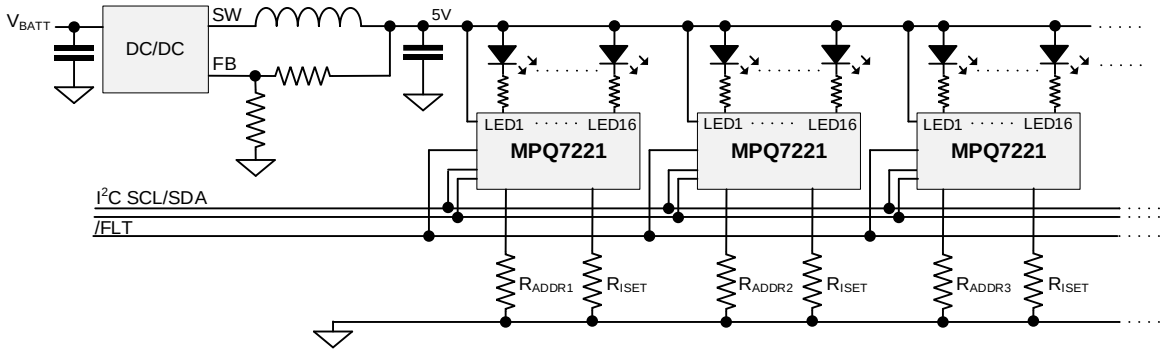


Figure 3: System Application Circuit with 1 LED and Resistor in Series

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Level**
MPQ7221GRE-AEC1***	QFN-24 (4mmx4mm)	*See Below*	1

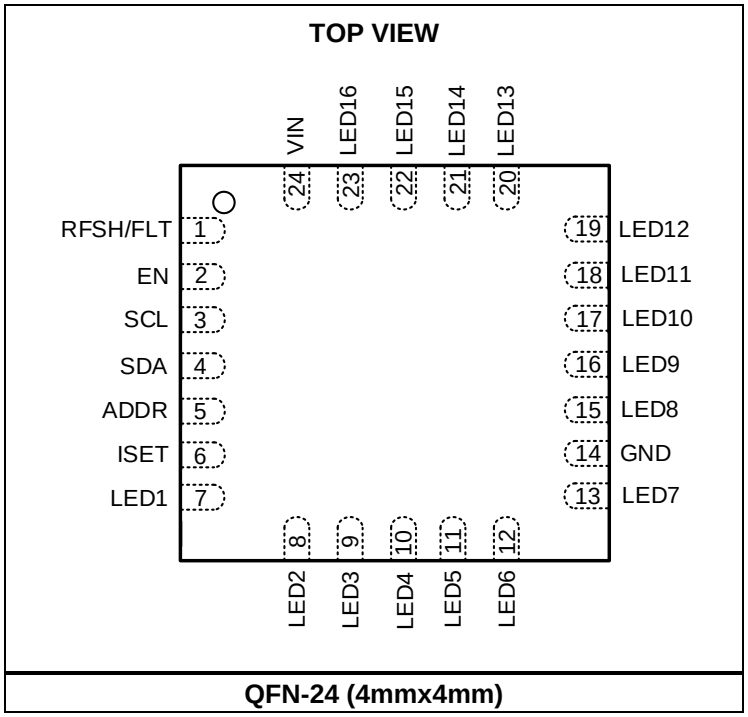
* For Tape & Reel, add suffix -Z (e.g. MPQ7221GRE-AEC1-Z).
** Moisture Sensitivity Level Rating
*** Wettable Flank

TOP MARKING

MPSYWW
MP7221
LLLLLL
E

MPS: MPS prefix
Y: Year code
WW: Week code
MP7221: Part number
LLLLLL: Lot number
E: Wettable flank

PACKAGE REFERENCE



QFN-24 (4mmx4mm)

PIN FUNCTIONS

Pin #	Name	Description
1	RFSH/FLT	**Refresh signal output or fault flag.** If FLTEN = 0, the REFSH/FLT pin outputs a synchronized signal set via the FRFSH register. If FLTEN = 1, REFSH/FLT is an indicator for fault conditions. If a fault is triggered, pull REFSH/FLT low.
2	EN	**Enable control.** Pull the EN pin low to disable the IC; pull EN high to enable the IC.
3	SCL	**I²C interface clock input.**
4	SDA	**I²C interface data input.**
5	ADDR	**I²C address setting.** Configure the I²C address via a separate ADDR resistor (R_{ADDR}) to GND. Use the four least significant bits (LSB) of the I²C addresses. A total of 10 different addresses are configurable.
6	ISET	**LED current setting.** Connect a current-setting resistor from ISET to ground to configure the current in each LED string.
7	LED1	**LED channel 1 current input.** Connect the LED channel 1 cathode to this pin.
8	LED2	**LED channel 2 current input.** Connect the LED channel 2 cathode to this pin.
9	LED3	**LED channel 3 current input.** Connect the LED channel 3 cathode to this pin.
10	LED4	**LED channel 4 current input.** Connect the LED channel 4 cathode to this pin.
11	LED5	**LED channel 5 current input.** Connect the LED channel 5 cathode to this pin.
12	LED6	**LED channel 6 current input.** Connect the LED channel 6 cathode to this pin.
13	LED7	**LED channel 7 current input.** Connect the LED channel 7 cathode to this pin.
14	GND	**Ground.**
15	LED8	**LED channel 8 current input.** Connect the LED channel 8 cathode to this pin.
16	LED9	**LED channel 9 current input.** Connect the LED channel 9 cathode to this pin.
17	LED10	**LED channel 10 current input.** Connect the LED channel 10 cathode to this pin.
18	LED11	**LED channel 11 current input.** Connect the LED channel 11 cathode to this pin.
19	LED12	**LED channel 12 current input.** Connect the LED channel 12 cathode to this pin.
20	LED13	**LED channel 13 current input.** Connect the LED channel 13 cathode to this pin.
21	LED14	**LED channel 14 current input.** Connect the LED channel 14 cathode to this pin.
22	LED15	**LED channel 15 current input.** Connect the LED channel 15 cathode to this pin.
23	LED16	**LED channel 16 current input.** Connect the LED channel 16 cathode to this pin.
24	VIN	**Power supply input.** This pin supplies power to the IC, and must be locally bypassed.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} ..... -0.3V to +22V
V_{LED1} to V_{LED16} ..... -0.5V to +22V
All other pins ..... -0.3V to +5V
Continuous power dissipation (T_A = 25°C) (2) (7)
QFN-24 (4mmx4mm) 1.79W
Junction temperature ..... 150°C
Lead temperature ..... 260°C

ESD Ratings

Human body model (HBM) ..... Class 1C (3)
Charged device model (CDM) ..... Class C2b (4)

Recommended Operating Conditions

Supply voltage (V_{IN}) ..... 4.5V to 16V
Operating junction temp (T_J) (5) ..... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-24 (4mmx4mm)			
JESD51-7	42	9	°C/W (6)
EVQ7221-R-00A	70	15	°C/W (7)

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Per AEC-Q100-002.
4) Per AEC-Q100-011.
5) Operating devices at a junction temperature up to 150°C is possible. Contact MPS for more details.
6) Measured on JESD51-7, a 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application. The θ_{JC} value shows the thermal resistance from the junction-to-case bottom.
7) Measured on a standard EVB: a 2-layer, 1oz copper thickness PCB (6.35cmx6.35cm). The θ_{JC} value shows the thermal resistance from the junction-to-case top.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, V_{EN} = 5V, T_J = -40°C to +125°C, typical value is at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Supply Voltage						
Input voltage range	V_{IN}		4.5		16	V
Quiescent supply current	I_Q				5	mA
Shutdown supply current	I_{SD}	V_{EN} = 0V, V_{IN} = 16V			2	μA
Input under-voltage lockout (UVLO) threshold	V_{IN_UVLO}	Rising edge	3.6	3.8	4.2	V
		Falling edge	3.3	3.5	3.7	V
Enable (EN)						
EN rising threshold	V_{EN_ON}	EN rising	2.1			V
EN falling threshold	V_{EN_OFF}	EN falling			0.8	V
EN pull-down resistor	R_{EN}			1		MΩ
RFSH/FLT						
RFSH/FLT output frequency	$f_{RFSH/FLT}$	FRFSH[9:0] = 0x1A9, FPWM[2:0] = 01	285	300	315	Hz
RFSH/FLT pull-down resistor		FLTEN = 1, fault triggered			100	Ω
LED Regulator						
ISET voltage	V_{ISET}	T_J = 25°C	1.176	1.2	1.224	V
LED current	I_{LED}	R_{ISET} = 24kΩ, ICHx[5:0] = 0x3F	-5%	50	+5%	mA
		R_{ISET} = 24kΩ, ICHx[5:0] = 0x3F, T_J = 25°C	-3%	50	+3%	mA
		R_{ISET} = 15kΩ, ICHx[5:0] = 0x3F	-5%	80	+5%	mA
		R_{ISET} = 15kΩ, ICHx[5:0] = 0x3F, T_J = 25°C	-3%	80	+3%	mA
Current sink headroom	V_{LEDx}	I_{LED} = 50mA		200	300	mV
		I_{LED} = 80mA		350	450	mV
Dimming						
Pulse-width modulation (PWM) frequency	f_{PWM}		240	250	260	Hz
PWM duty step	t_{PWM}	12-bit resolution, f_{PWM} = 250Hz		1		μs
Phase shift	t_{DELAY}	PS_EN = 1		40		μs
I_{LED} step		I_{LED} = 80mA, analog dimming step		1.25		mA
I_{LED} slew rate in PWM dimming		SLEW[2:0] = 01, rising edge		5		μs
		SLEW[1:0] = 11, rising edge		20		μs
Protections						
LED short-string protection threshold	V_{SLP}	STH[1:0] = 01	2.85	3	3.15	V
LED short-string protection time	t_{SLP}	V_{LEDx} > STH		4		ms
LED short-string protection hiccup time	t_{SLP_HICCUP}			1		ms

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{EN} = 5V, T_J = -40°C to +125°C, typical value is at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
LED short-string protection hiccup detection time	V_{SLP_DET}			32		µs
LED open-string protection threshold	V_{LED_UV}			100	150	mV
LED open-string protection time	t_{LEDO}	V_{LEDx} < 100mV		4		ms
LED open-string protection hiccup time	t_{SLP_HICCUP}			1		ms
LED open-string protection hiccup detection time	V_{SLP_DET}			32		µs
Thermal shutdown threshold (8)	T_{ST}			170		°C
Thermal shutdown hysteresis (8)	T_{ST_HYS}			20		°C
I²C Interface						
Input logic low	V_{IL}		0		0.4	V
Input logic high	V_{IH}		1.3V			V
Output logic low	V_{OL}	I_{LOAD} = 3mA			0.4	V
SCL clock frequency	f_{SCL}				1200	kHz
SCL high time	t_{HIGH}		0.32			µs
SCL low time	t_{LOW}		0.12			µs
Data set-up time	t_{SU_DAT}		10			ns
Data hold time	t_{HD_DAT}		0		0.15	µs
Set-up time for a repeated start condition	t_{SU_STA}		0.16			µs
Hold time for a start condition	t_{HD_STA}		0.16			µs
Set-up time for a stop condition	t_{SU_STO}		0.16			µs
SCL rising time after a repeated start condition and an acknowledge bit	t_{R_CL1}		20		160	ns
SCL rising time	t_{R_CL}		20		80	ns
SCL falling time	t_{F_CL}		20		80	ns
SDA rising time	t_{R_DA}		20		160	ns
SDA falling time	t_{F_DA}		20		160	ns
Pulse width of suppressed spike	t_{SP}		0		10	ns
Capacitance bus for each bus line	C_B				400	pF

Note:

8) Derived from bench characterization. Not tested in production.

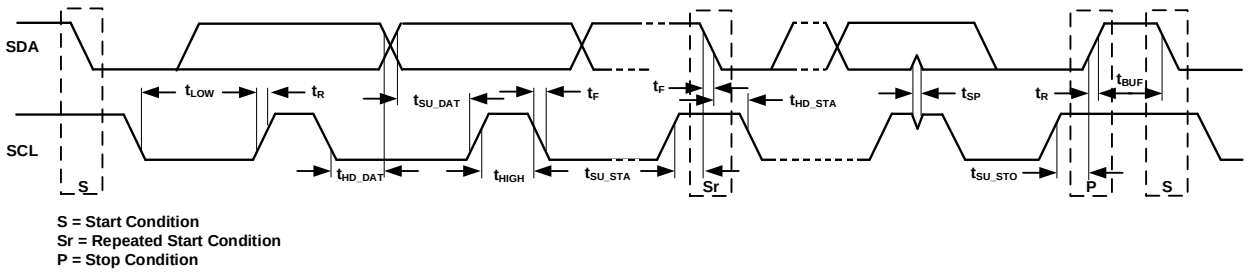
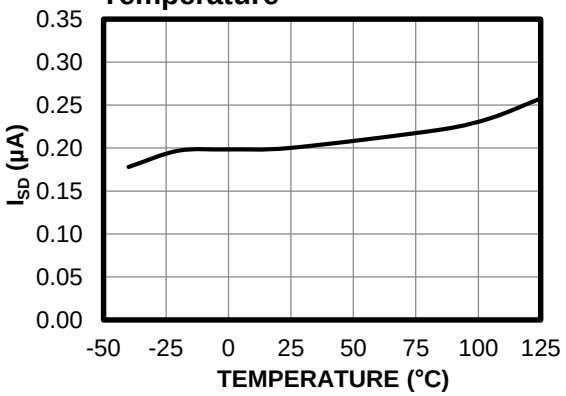


Figure 4: I²C-Compatible Interface Timing Diagram

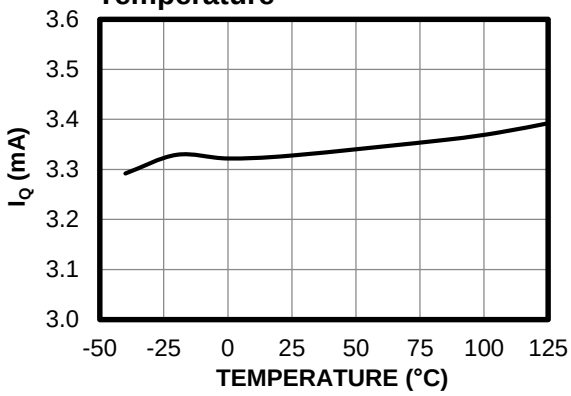
TYPICAL CHARACTERISTICS

V_{IN} = 5V, T_J = -40°C to +125°C, unless otherwise noted.

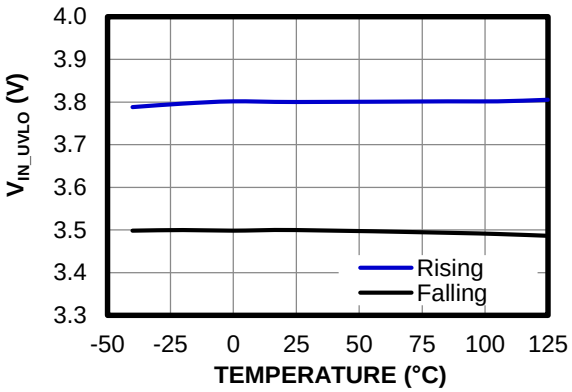
Shutdown Current vs. Temperature



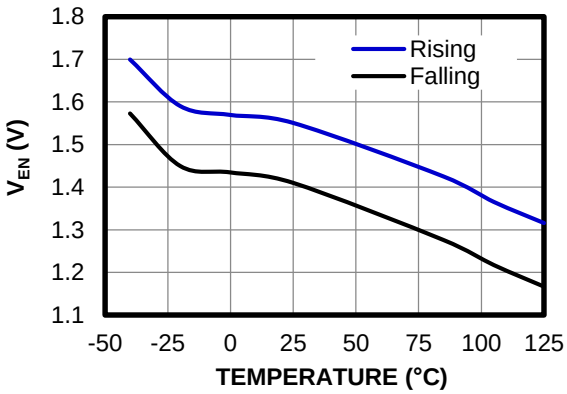
Quiescent Current vs. Temperature



V_{IN} UVLO Threshold vs. Temperature

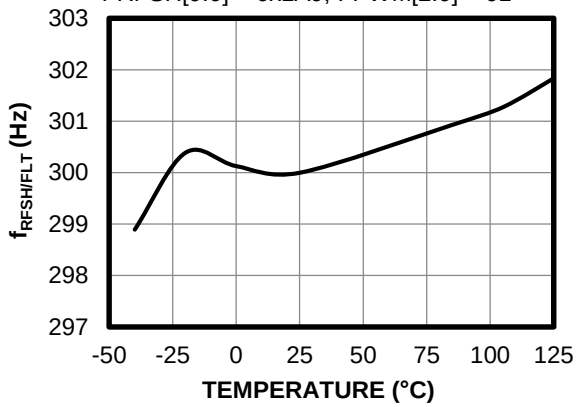


EN Threshold vs. Temperature

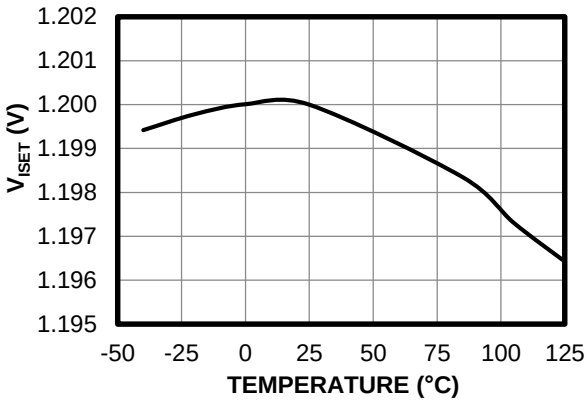


RFSH/FLT Output Frequency vs. Temperature

FRFSH[9:0] = 0x1A9, FPWM[2:0] = 01



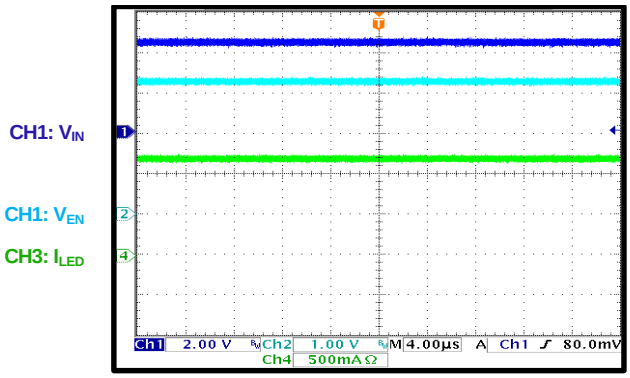
ISET Voltage vs. Temperature



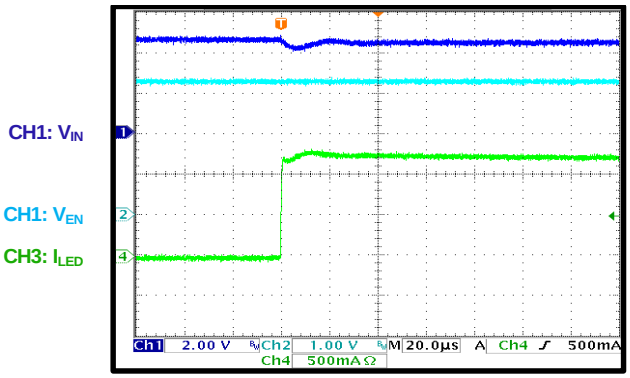
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 4.5V, I_{LED} = 80mA per string, LED = 16P1S, T_A = 25°C, unless otherwise noted.

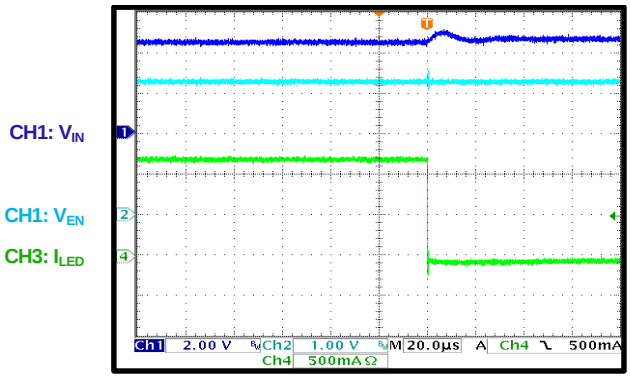
Steady State



Start-Up via the EN Bit

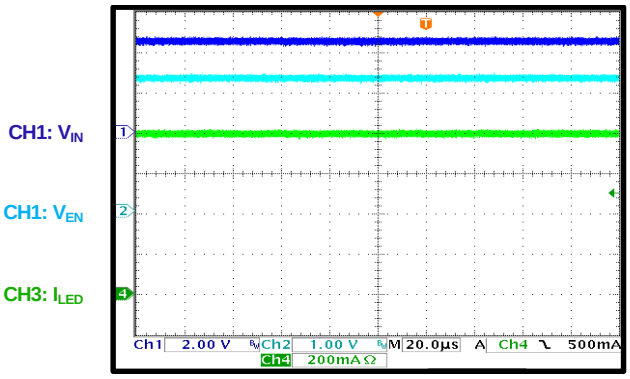


Shutdown via the EN Bit



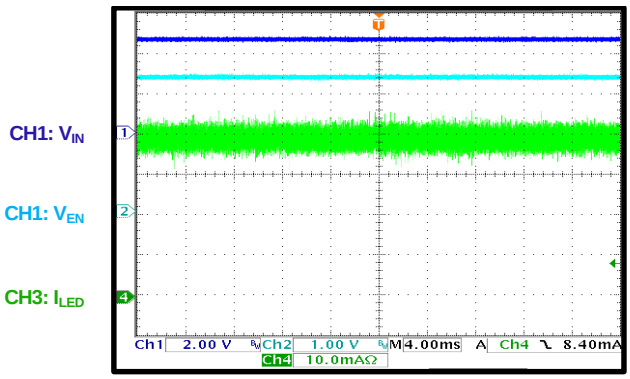
Analog Dimming

50mA/string



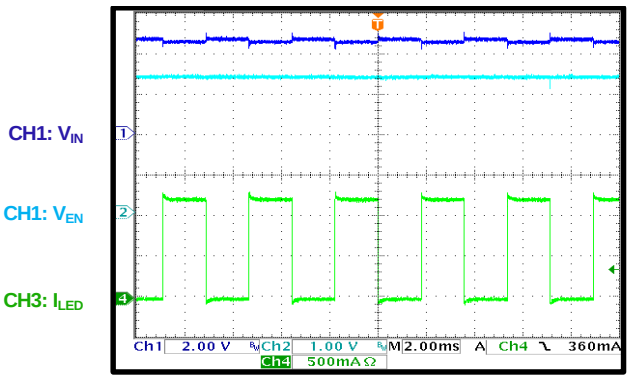
Analog Dimming

2.5mA/string



PWM Dimming

PWM duty = 50%

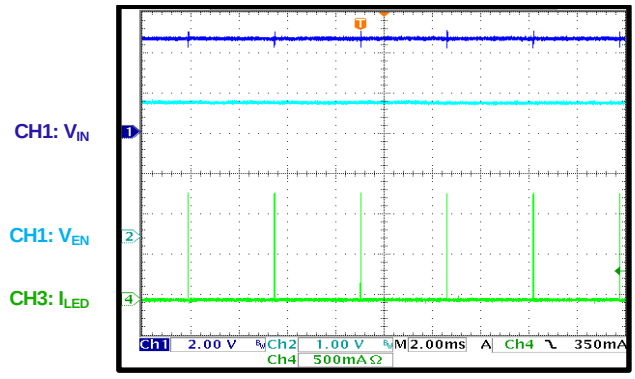


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 4.5V, I_{LED} = 80mA per string, LED = 16P1S, T_A = 25°C, unless otherwise noted.

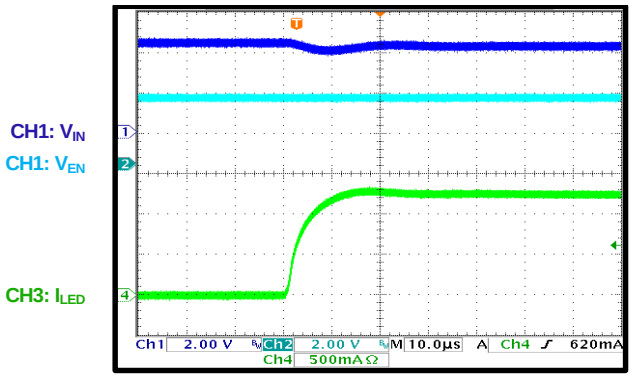
PWM Dimming

PWM duty = 0.5%



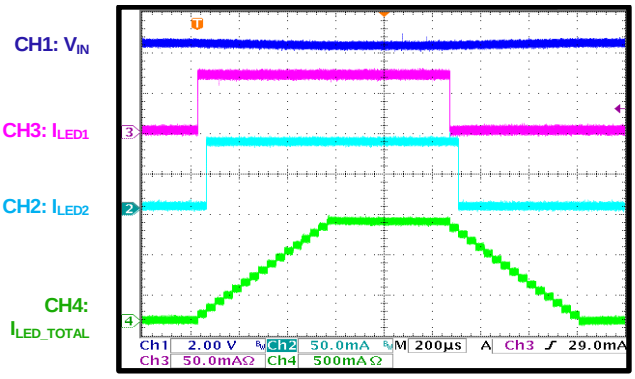
Slew Rate

PWM dimming slew rate = 5μs



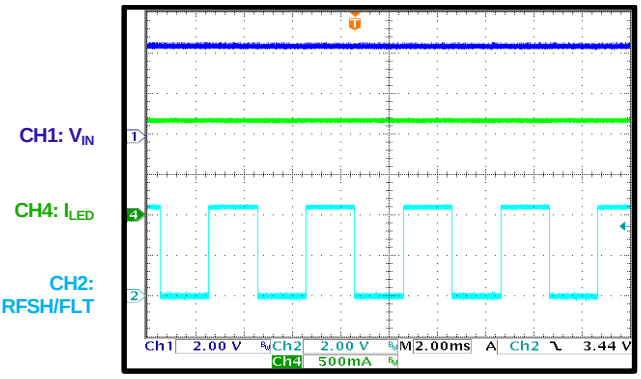
Phase Shift

PWM dimming duty = 20%



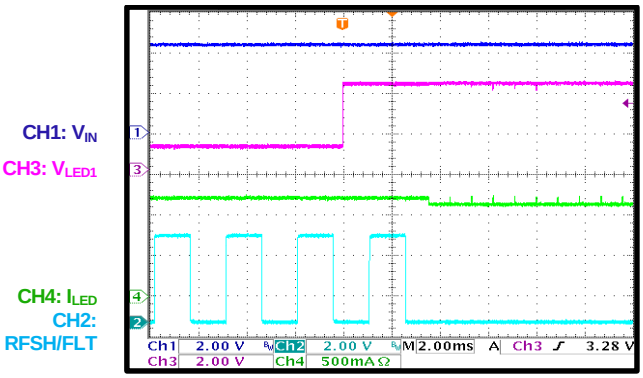
Refresh Function

f_{PWM} = 250Hz, FRFSH = 0x1FF



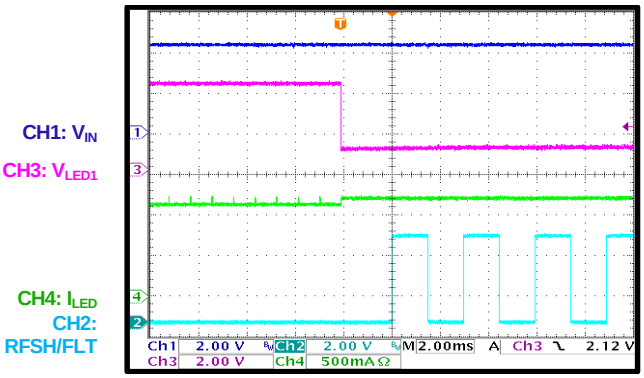
LEDx Short Entry

RFSH/FLT fault enabled, f_{PWM} = 330Hz, FRFSH = 0x1FF



LEDx Short Recovery

RFSH/FLT fault enabled, f_{PWM} = 330Hz, FRFSH = 0x1FF

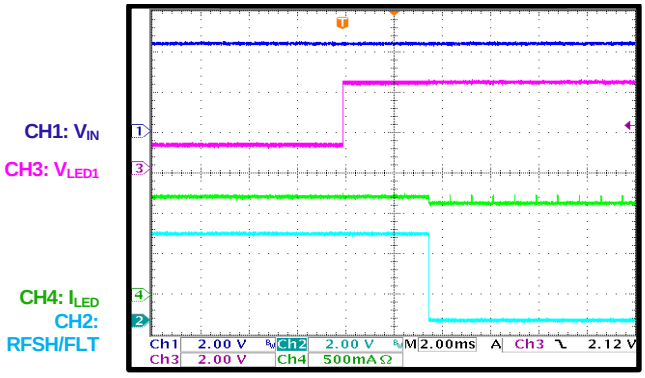


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 4.5V, I_{LED} = 80mA per string, LED = 16P1S, T_A = 25°C, unless otherwise noted.

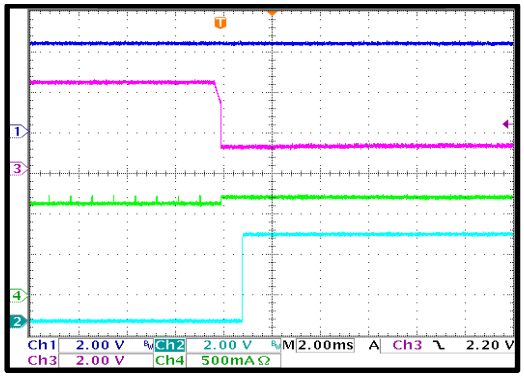
LEDx Short Entry

RFSH/FLT fault enabled, f_{PWM} = 250Hz, FRFSH = 0x000



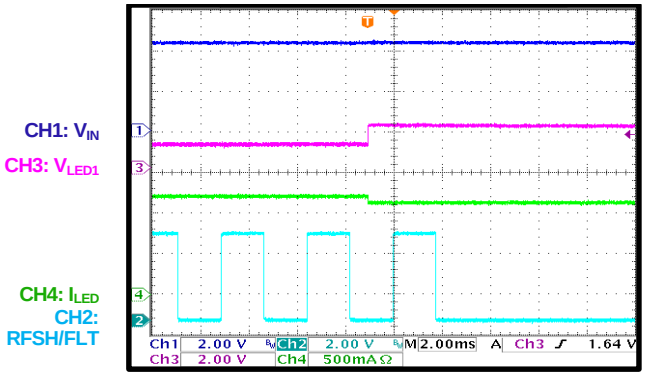
LEDx Short Recovery

RFSH/FLT fault enabled, f_{PWM} = 250Hz, FRFSH = 0x000



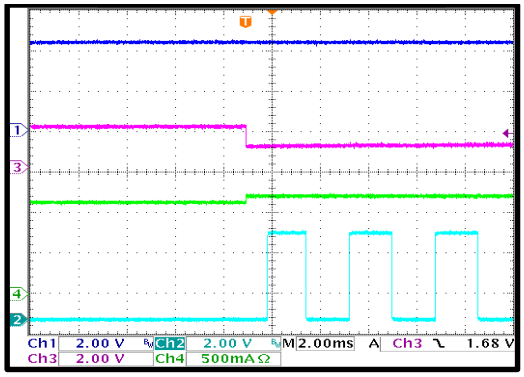
LEDx Open Entry

RFSH/FLT fault enabled, f_{PWM} = 280Hz, FRFSH = 0x1FF



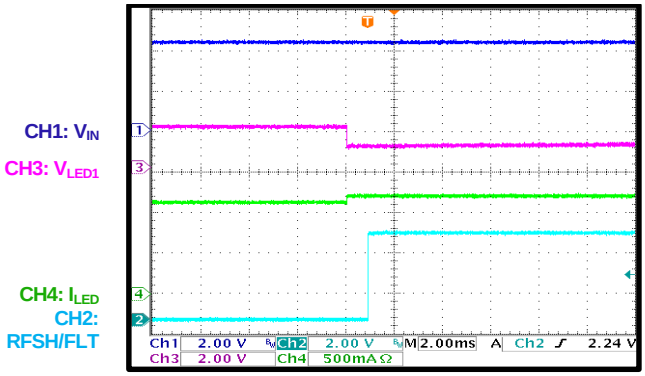
LEDx Open Recovery

RFSH/FLT fault enabled, f_{PWM} = 280Hz, FRFSH = 0x1FF



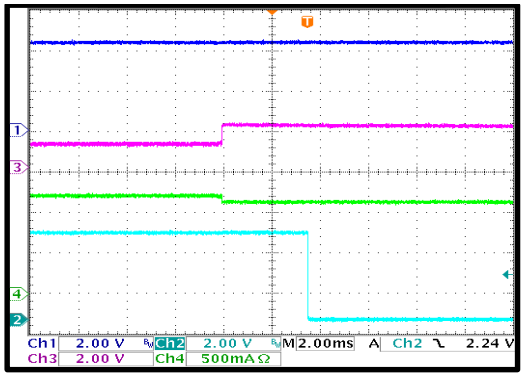
LEDx Open Entry

RFSH/FLT fault enabled, f_{PWM} = 250Hz, FRFSH = 0x000



LEDx Open Recovery

RFSH/FLT fault enabled, f_{PWM} = 250Hz, FRFSH = 0x000



FUNCTIONAL BLOCK DIAGRAM

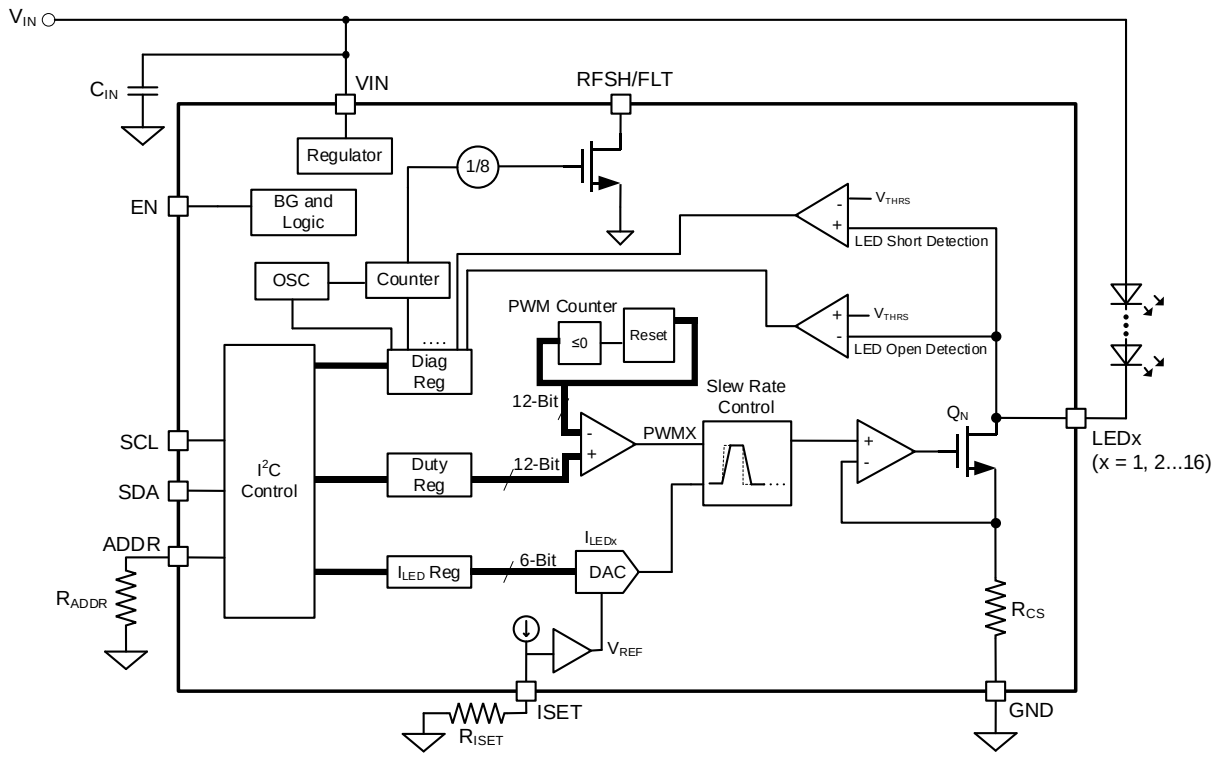


Figure 5: Functional Block Diagram

OPERATION

The MPQ7221 applies 16 internal current sources in each LED string terminal. The LED current (I_{LED}) of all the channels is set via an external current-setting resistor, with a maximum current up to 80mA.

Enable (EN) and Start-Up

Once the input voltage (V_{IN}) exceeds the under-voltage lockout (UVLO) threshold (V_{IN_UVLO}) and the EN pin exceeds the rising threshold (V_{EN_ON}), the MPQ7221 enters standby mode and the I²C interface is active. After setting the I²C register, set the EN bit high to start up the system. The start-up sequence is as follows:

1. VIN
2. EN
3. I²C setting
4. Set the EN bit via the I²C

Channel Selection

The channel can be disabled by pulling the corresponding CHxEN bit (where x = 1, 2...16) low or connecting the channel to GND.

LED Current Setting

Connect a resistor from the ISET pin to GND to set the 16-channel I_{LED}. The ISET current (I_{SET}) can be calculated using Equation (1):

$$I_{SET}(mA) = \frac{1200}{R_{ISET}}(k\Omega) \quad (1)$$

Dimming

Each channel includes a separate 6-bit analog dimming register and 12-bit pulse-width modulation (PWM) dimming register. The MPQ7221 can support analog dimming and PWM dimming for each channel.

In analog dimming, the I_{LED} amplitude changes when the analog dimming register changes. Change the code in ICHx (x = 1, 2...16) to apply analog dimming for the corresponding channel. The change in the I_{LED} amplitude (I_{LED}) can be calculated using Equation (2):

$$I_{LED}(mA) = \frac{ICHx}{63} \times ISET \quad (2)$$

Where ICHx is the analog dimming code for channel x (x = 1, 2...16).

If ICHx is set to 0, then I_{LED} is 0.

In PWM dimming, the LED current is chopped, the high value of I_{LED} remains the same, and the I_{LED} duty varies with the PWM dimming register.

The PWM dimming duty (D_{PWM}) is set by the register PWMx (x = 1, 2...16), and can be calculated using Equation (3):

$$D_{PWM} = \frac{PWMx}{4095} \quad (3)$$

Where PWMx is the D_{PWM} code for channel x (x = 1, 2...16).

The duty changes only when the PWM duty register's 8 most significant bits (MSB) are written. If PWMx is set to 0, then the corresponding channel I_{LED} is 0mA.

The PWM dimming frequency (f_{PWM}) can be selected by the register FPWM[1:0], where:

- FPWM[1:0] = 00, 220Hz
- FPWM[1:0] = 01, 250Hz (default)
- FPWM[1:0] = 10, 280Hz
- FPWM[1:0] = 11, 330Hz

To avoid glitches during operation, two steps are required:

1. Change the FPWM value only when the EN bit is set to 0.
2. Write the FPWM register, there is a10μs delay before other registers can be written.

Phase Shift

The channel-by-channel phase-shift function is enabled by setting the PS_EN bit high via the I²C interface.

When the phase shift function is enabled, the channel x + 1 (x = 1, 2...15) I_{LED} rising edge occurs 40μs after the channel x I_{LED} rising edge.

SYNC Output

The fault indicator function can be enabled via the FLTEN bit.

If FLTEN = 0, then the fault indicator function is disabled and the RFSH/FLT pin keeps the output refresh signal, even when protection is triggered.

If FLTEN = 1, then the fault indicator function is enabled and the SYNC/FLT pin is pulled low when protection is triggered.

Table 1 shows the RFSH/FLT output status, which depends on the fault condition.

Table 1: RFSH/FLT Output Status

FLTEN	FRFSH = 0x000		FRFSH = 0x001 - 0x12B	
	No fault	Fault	No fault	Fault
1	Pull high externally	Low	Rectangle signal	Low
0	Pull high externally		Rectangle signal	

The refresh signal frequency ($f_{REFRESH}$) is set via the FRFSH[9:0] register. If FRFSH[9:0] = 0x000, then RFSH/FLT outputs high. If FRFSH[9:0] = 0x001 to 0x3FF, then RFSH/FLT outputs a rectangle signal (FPWM[1:0] = 01, 250Hz f_{PWM}). $f_{REFRESH}$ can be estimated using Equation (4):

$$f_{REFRESH} = \frac{127500}{FRFSH[9:0]} \quad (4)$$

The relationship between $f_{REFRESH}$ and f_{PWM} when FRFSH[9:0] > 0 can be estimated using Equation (5):

$$f_{REFRESH} = \frac{127500}{FRFSH} \times \frac{f_{PWM}}{250} (Hz) \quad (5)$$

Where FRFSH is the register FRFSH[9:0] value, and f_{PWM} is set by register FPWM[1:0], meaning f_{PWM} is selectable as 220Hz, 250Hz, 280Hz, and 330Hz.

It should be noted that all the values in Equation (5) are decimal-based. In addition, $f_{REFRESH}$ does not change until the 8MSB are written. The FRFSH register value is reset when FRFSH[9:0] = 0x000 is written.

The clock for $f_{REFRESH}$ generation divides the internal oscillator by 8. The FRFSH register sets the counter number.

Figure 6 shows the $f_{REFRESH}$ generation.

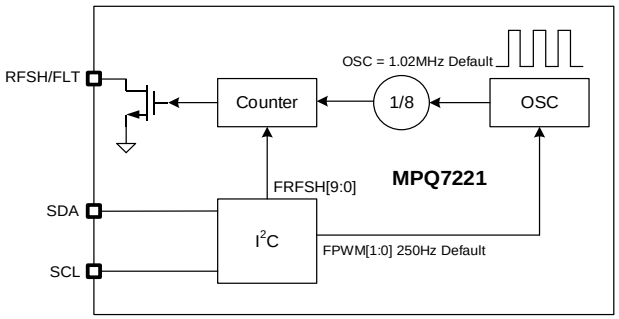


Figure 6: Refresh Frequency Generation

LED Current Slew Rate Control

To sufficiently optimize the EMI performance, change the I_{LED} rising and falling slew rate in PWM dimming. The I_{LED} rising and falling slew rate is controlled by the SLEW[1:0] register, where:

- SLEW[1:0] = 00, no slew rate
- SLEW[1:0] = 01, 5μs
- SLEW[1:0] = 10, 10μs
- SLEW[1:0] = 11, 20μs

Protections

The MPQ7221 employs V_{IN} UVLO, LED short protection, LED open protection, and thermal shutdown.

The /FLT pin is an active low, open-drain output that is pulled high to an external voltage source. If a protection is triggered, the corresponding fault bit is set and /FLT is pulled low.

In hiccup mode, /FLT is pulled high once all fault conditions are removed. In latch-off mode, /FLT is released once all fault bits are read.

For LED open and short protection, hiccup mode or latch-off mode can be selected via the LATCH bit in the I²C.

If LATCH = 1, the MPQ7221 enters latch-off mode. Once a fault is triggered, the fault channel remains off until the power is cycled on VIN or EN turns off, which resets the fault channel.

If LATCH = 0, the MPQ7221 enters hiccup mode, during which the fault channel tries to conduct for 20μs every 1ms to detect whether the fault has been cleared. Once the fault condition is removed, /FLT is released.

V_{IN} Under-Voltage Lockout (UVLO)

When V_{IN} drops below V_{IN_UVLO}, the IC stops working and all the I²C registers are reset.

LED Open Protection

When LED is open, the LEDx (x = 1, 2...16) voltage (V_{LEDx}) drops. If V_{LEDx} drops below the 100mV protection threshold for 4ms, then LED open protection is triggered, the fault channel turns off, the corresponding open fault bit (CHxO, where x = 1, 2...16) is set, and /FLT is pulled low. The fault bit is reset when it is read, and then /FLT is released high.

LED Short Protection

In an LED short condition, V_{IN} - V_{LEDx} drops low and LED short protection is triggered once V_{LEDx} (x = 1, 2...16) exceeds the voltage set by STH for 4ms. Then the short channel turns off, the corresponding fault bit CHxS (x = 1, 2...16) is set, and /FLT is pulled low.

The LED short protection threshold is configured via the STH[1:0] register, where:

- STH[1:0] = 00, 2V short protection threshold
- STH[1:0] = 01, 3V short protection threshold
- STH[1:0] = 10, 4V short protection threshold
- STH[1:0] = 11, 5V short protection threshold

The fault bit is reset when it is read, and then /FLT is released high.

Over-Temperature Protection (OTP)

If the IC temperature exceeds 170°C, then over-temperature protection (OTP) is triggered, all channels turn off, /FLT is pulled low, and FT_OTP is set. Once the temperature drops by 20°C, all the channels turn on and the IC resumes normal operation.

I²C INTERFACE

I²C Chip Address

The device address is 0x30~0x39, and is configured via the ADDR resistor (R_{ADDR}). The internal current source flows to R_{ADDR}, and the ADDR voltage determines the I²C address. Ten different addresses can be configured via R_{ADDR}.

Table 2 shows the I2C address setting details.

Table 2: I²C Address Setting

R_{ADDR} / R_{ISET}	I²C Address (A3A2A1A0)
<0.05	0000
>0.05, <0.15	0001
>0.15, <0.25	0010
>0.25, <0.35	0011
>0.35, <0.45	0100
>0.45, <0.55	0101
>0.55, <0.65	0110
>0.65, <0.75	0111
>0.75, <0.85	1000
>0.85, <0.95	1001

At start-up, the IC checks the I²C address first. The address remains the same during operation until the IC's power is reset.

After a start (S) command, the I²C-compatible master sends a 7-bit address, followed by an 8th data direction bit (where 1 = read and 0 = write, respectively).

Figure 7 shows the register address to/from which the data is written and read.

0	1	1	A3	A2	A1	A0	R/W

Figure 7: I²C Compatible Device Address

To avoid glitches during operation, two steps are required:

1. Change the FPWM value only when the EN bit is set to 0.
2. Write the FPWM register, then resume writing the other registers after a 10μs delay.

REGISTER MAP

Add	Default	D7	D6	D5	D4	D3	D2	D1	D0
00h	01	RESERVED						FPWM[1:0]	
01h	00	FLTEN	LATCH	STH[1:0]		SLEW[1:0]		PS_EN	EN
02h	01	RESERVED					FT_OTP	FRFSH[1:0]	
03h	6A	FRFSH[9:2]							
04h	FF	CH16EN	CH15EN	CH14EN	CH13EN	CH12EN	CH11EN	CH10EN	CH9EN
05h	FF	CH8EN	CH7EN	CH6EN	CH5EN	CH4EN	CH3EN	CH2EN	CH1EN
06h	00	CH16O	CH15O	CH14O	CH13O	CH12O	CH11O	CH10O	CH9O
07h	00	CH8O	CH7O	CH6O	CH5O	CH4O	CH3O	CH2O	CH1O
08h	00	CH16S	CH15S	CH14S	CH13S	CH12S	CH11S	CH10S	CH9S
09h	00	CH8S	CH7S	CH6S	CH5S	CH4S	CH3S	CH2S	CH1S
0Ah	3F	RESERVED		ICH1[5:0]					
0Bh	0F	RESERVED				PWM1[3:0]			
0Ch	FF	PWM1[11:4]							
0Dh	3F	RESERVED		ICH2[5:0]					
0Eh	0F	RESERVED				PWM2[3:0]			
0Fh	FF	PWM2[11:4]							
10h	3F	RESERVED		ICH3[5:0]					
11h	0F	RESERVED				PWM3[3:0]			
12h	FF	PWM3[11:4]							
13h	3F	RESERVED		ICH4[5:0]					
14h	0F	RESERVED				PWM4[3:0]			
15h	FF	PWM4[11:4]							
16h	3F	RESERVED		ICH5[5:0]					
17h	0F	RESERVED				PWM5[3:0]			
18h	FF	PWM5[11:4]							
19h	3F	RESERVED		ICH6[5:0]					
1Ah	0F	RESERVED					PWM6[3:0]		
1Bh	FF	PWM6[11:4]							
1Ch	3F	RESERVED		ICH7[5:0]					
1Dh	0F	RESERVED				PWM7[3:0]			
1Eh	FF	PWM7[11:4]							
1Fh	3F	RESERVED		ICH8[5:0]					
20h	0F	RESERVED				PWM8[3:0]			
21h	FF	PWM8 11:4							
22h	3F	RESERVED		ICH9[5:0]					
23h	0F	RESERVED					PWM9[3:0]		
24h	FF	PWM9[11:4]							
25h	3F	RESERVED		ICH10[5:0]					
26h	0F	RESERVED					PWM10[3:0]		
27h	FF	PWM10[11:4]							
28h	3F	RESERVED		ICH11[5:0]					
29h	0F	RESERVED					PWM11[3:0]		

REGISTER MAP *(continued)*

Add	Default	D7	D6	D5	D4	D3	D2	D1	D0
2Ah	FF	PWM11[11:4]							
2Bh	3F	RESERVED		ICH12[5:0]					
2Ch	0F	RESERVED					PWM12[3:0]		
2Dh	FF	PWM12[11:4]							
2Eh	3F	RESERVED		ICH13[5:0]					
2Fh	0F	RESERVED					PWM13[3:0]		
30h	FF	PWM13[11:4]							
31h	3F	RESERVED		ICH14[5:0]					
32h	0F	RESERVED					PWM14[3:0]		
33h	FF	PWM14[11:4]							
34h	3F	RESERVED		ICH15[5:0]					
35h	0F	RESERVED					PWM15[3:0]		
36h	FF	PWM15[11:4]							
37h	3F	RESERVED		ICH16[5:0]					
38h	0F	RESERVED					PWM16[3:0]		
39h	FF	PWM16[11:4]							

REG00h

Addr: 0x00				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:2	N/A	R	000000	Reserved.
1:0	FPWM	RW	01	Sets the pulse-width modulation (PWM) dimming frequency (D_{PWM}). Change the FPWM value only when the EN bit is set to 0. Write the FPWM register, then allow for a 10μs delay before writing to other registers. 00: 220Hz 01: 250Hz 10: 280Hz 11: 330Hz

REG01h

Addr: 0x01				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7	FLTEN	RW	0	Enables the RFSH/FLT fault indicator. 0: Disabled, where the fault indicator function is disabled and RFSH/FLT is the refresh signal output 1: Enabled, where the fault indicator function is enabled
6	LATCH	RW	0	Enables latching off if a fault occurs. 0: Disabled, hiccup mode used if a fault occurs 1: Enabled, fault latches if a fault occurs
5:4	S_TH[1:0]	RW	00	Sets the LED short protection threshold. 00: 2V 01: 3V 10: 4V 11: 5V
3:2	SLEW[1:0]	RW	00	Sets the LED current (I_{LED}) slew rate. 00: No slew rate 01: 5μs 10: 10μs 11: 20μs
1	PS_EN	RW	0	Enables the phase shift. 0: Disabled 1: Enabled, where channel x + 1's rising edge occurs 40μs after channel x (x = 1, 2...15)
0	EN	RW	0	Enables the IC. 0: Disabled 1: Enabled

REG02h

Addr: 0x02				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:3	N/A	R	0	Reserved.
2	FT_OTP	R	0	Sets the over-temperature (OT) fault. 0: No over-temperature protection (OTP) fault 1: OTP fault
1:0	FRFSH[1:0]	RW	01	Sets the refresh frequency ($f_{REFRESH}$), 2 least significant bits (LSB). FRFSH[9:0] = 0x000, high FRFSH[9:0] > 0 $f_{REFRESH} = \frac{127500}{FRFSH} x \frac{f_{PWM}}{250} (Hz)$ Where all values in the equation are decimal-based, and $f_{REFRESH}$ does not change until the 8 most significant bits (MSB) are written. The default $f_{REFRESH}$ is 300Hz.

REG03h

Addr: 0x03				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	FRFSH[9:2]	RW	6A	Sets $f_{REFRESH}$, 8MSB. FRFSH[9:0] = 0x000, high FRFSH[9:0] > 0 $f_{REFRESH} = \frac{127500}{FRFSH} x \frac{f_{PWM}}{250} (Hz)$ Where all values in the equation are decimal-based and $f_{REFRESH}$ does not change until the 8MSB are written. The default $f_{REFRESH}$ is 300Hz.

REG04h

Addr: 0x04				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7	CH16EN	RW	1	Enables channel 16. 0: Disabled 1: Enabled
6	CH15EN	RW	1	Enables channel 15. 0: Disabled 1: Enabled
5	CH14EN	RW	1	Enables channel 14. 0: Disabled 1: Enabled
4	CH13EN	RW	1	Enables channel 13. 0: Disabled 1: Enabled
3	CH12EN	RW	1	Enables channel 12. 0: Disabled 1: Enabled
2	CH11EN	RW	1	Enables channel 11. 0: Disabled 1: Enabled
1	CH10EN	RW	1	Enables channel 10. 0: Disabled 1: Enabled
0	CH9EN	RW	1	Enables channel 9. 0: Disabled 1: Enabled

REG05h

Addr: 0x05				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7	CH8EN	RW	1	Enables channel 8. 0: Disabled 1: Enabled
6	CH7EN	RW	1	Enables channel 7. 0: Disabled 1: Enabled
5	CH6EN	RW	1	Enables channel 6. 0: Disabled 1: Enabled
4	CH5EN	RW	1	Enables channel 5. 0: Disabled 1: Enabled
3	CH4EN	RW	1	Enables channel 4. 0: Disabled 1: Enabled
2	CH3EN	RW	1	Enables channel 3. 0: Disabled 1: Enabled
1	CH2EN	RW	1	Enables channel 2. 0: Disabled 1: Enabled
0	CH1EN	RW	1	Enables channel 1. 0: Disabled 1: Enabled

REG06h

Addr: 0x06				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7	CH16O	R	0	Channel 16 open protection fault flag. 0: No fault 1: Fault
6	CH15O	R	0	Channel 15 open protection fault flag. 0: No fault 1: Fault
5	CH14O	R	0	Channel 14 open protection fault flag. 0: No fault 1: Fault
4	CH13O	R	0	Channel 13 open protection fault flag. 0: No fault 1: Fault
3	CH12O	R	0	Channel 12 open protection fault flag. 0: No fault 1: Fault
2	CH11O	R	0	Channel 11 open protection fault flag. 0: No fault 1: Fault
1	CH10O	R	0	Channel 10 open protection fault flag. 0: No fault 1: Fault
0	CH9O	R	0	Channel 9 open protection fault flag. 0: No fault 1: Fault

REG07h

Addr: 0x07				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7	CH8O	R	0	Channel 8 open protection fault flag. 0: No fault 1: Fault
6	CH7O	R	0	Channel 7 open protection fault flag. 0: No fault 1: Fault
5	CH6O	R	0	Channel 6 open protection fault flag. 0: No fault 1: Fault
4	CH5O	R	0	Channel 5 open protection fault flag. 0: No fault 1: Fault
3	CH4O	R	0	Channel 4 open protection fault flag. 0: No fault 1: Fault
2	CH3O	R	0	Channel 3 open protection fault flag. 0: No fault 1: Fault
1	CH2O	R	0	Channel 2 open protection fault flag. 0: No fault 1: Fault
0	CH1O	R	0	Channel 1 open protection fault flag. 0: No fault 1: Fault

REG08h

Addr: 0x08				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7	CH16S	R	0	Channel 16 short protection fault flag. 0: No fault 1: Fault
6	CH15S	R	0	Channel 15 short protection fault flag. 0: No fault 1: Fault
5	CH14S	R	0	Channel 14 short protection fault flag. 0: No fault 1: Fault
4	CH13S	R	0	Channel 13 short protection fault flag. 0: No fault 1: Fault
3	CH12S	R	0	Channel 12 short protection fault flag. 0: No fault 1: Fault
2	CH11S	R	0	Channel 11 short protection fault flag. 0: No fault 1: Fault
1	CH10S	R	0	Channel 10 short protection fault flag. 0: No fault 1: Fault
0	CH9S	R	0	Channel 9 short protection fault flag. 0: No fault 1: Fault

REG09h

Addr: 0x09				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7	CH8S	R	0	Channel 8 short protection fault flag. 0: No fault 1: Fault
6	CH7S	R	0	Channel 7 short protection fault flag. 0: No fault 1: Fault
5	CH6S	R	0	Channel 6 short protection fault flag. 0: No fault 1: Fault
4	CH5S	R	0	Channel 5 short protection fault flag. 0: No fault 1: Fault
3	CH4S	R	0	Channel 4 short protection fault flag. 0: No fault 1: Fault
2	CH3S	R	0	Channel 3 short protection fault flag. 0: No fault 1: Fault
1	CH2S	R	0	Channel 2 short protection fault flag. 0: No fault 1: Fault
0	CH1S	R	0	Channel 1 short protection fault flag. 0: No fault 1: Fault

REG0Ah

Addr: 0x0A				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	N/A	R	00	Reserved.
5:0	ICH1[5:0]	RW	111111	Channel 1 I_{LED} analog dimming register. $I_{LED} = \frac{Code}{63} \times I_{SET}$ Where Code is the register value.

REG0Bh

Addr: 0x0B				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:4	N/A	R	0000	Reserved.
3:0	PWM1[3:0]	RW	1111	Sets the channel 1 I_{LED} D_{PWM}, 4LSB. D_{PWM} only changes when the 8MSB are written.

REG0Ch

Addr: 0x0C				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM1[11:4]	RW	11111111	Sets the channel 1 I_{LED} D_{PWM}, 8MSB. D_{PWM} only changes when the 8MSB are written.

REG0Dh

Addr: 0x0D				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	N/A	R	00	Reserved.
5:0	ICH2[5:0]	RW	111111	Channel 2 I_{LED} analog dimming register. $$I_{LED} = \frac{Code}{63} \times I_{SET}$$ Where Code is the register value.

REG0Eh

Addr: 0x0E				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7:4	N/A	R	0000	Reserved.
3:0	PWM2[3:0]	RW	1111	Sets the channel 2 I_{LED} D_{PWM}, 4LSB. D_{PWM} only changes when the 8MSB are written.

REG0Fh

Addr: 0x0F				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM2[11:4]	RW	11111111	Sets the channel 2 I_{LED} D_{PWM}, 8MSB. D_{PWM} only changes when the 8MSB are written.

REG10h

Addr: 0x10				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	N/A	R	00	Reserved.
5:0	ICH3[5:0]	RW	111111	Channel 3 I_{LED} analog dimming register. $$I_{LED} = \frac{Code}{63} \times I_{SET}$$ Where Code is the register value.

REG11h

Addr: 0x11				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7:4	N/A	R	0000	Reserved.
3:0	PWM3[3:0]	RW	1111	Sets the channel 3 I_{LED} D_{PWM}, 4LSB. D_{PWM} only changes when the 8MSB are written.

REG12h

Addr: 0x12				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM3[11:4]	RW	11111111	Sets the channel 3 I_{LED} D_{PWM}, 8MSB. D_{PWM} only changes when the 8MSB are written.

REG13h

Addr: 0x13				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	N/A	R	00	Reserved.
5:0	ICH4[5:0]	RW	111111	Channel 4 I_{LED} analog dimming register. $$I_{LED} = \frac{Code}{63} \times I_{SET}$$ Where Code is the register value.

REG14h

Addr: 0x14				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:4	N/A	R	0000	Reserved.
3:0	PWM4[3:0]	RW	1111	Sets the channel 4 I_{LED} D_{PWM}, 4LSB. D_{PWM} only changes when the 8MSB are written.

REG15h

Addr: 0x15				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM4[11:4]	RW	11111111	Sets the channel 4 I_{LED} D_{PWM}, 8MSB. D_{PWM} only changes when the 8MSB are written.

REG16h

Addr: 0x16				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	N/A	R	00	Reserved.
5:0	ICH5[5:0]	RW	111111	Channel 5 I_{LED} analog dimming register. $$I_{LED} = \frac{Code}{63} \times I_{SET}$$ Where Code is the register value.

REG17h

Addr: 0x17				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:4	N/A	R	0000	Reserved.
3:0	PWM5[3:0]	RW	1111	Sets the channel 5 I_{LED} D_{PWM}, 4LSB. D_{PWM} only changes when the 8MSB are written.

REG18h

Addr: 0x18				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM5[11:4]	RW	11111111	Sets the channel 5 I_{LED} D_{PWM}, 8MSB. D_{PWM} only changes when the 8MSB are written.

REG19h

Addr: 0x19				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	N/A	R	00	Reserved.
5:0	ICH6[5:0]	RW	111111	Channel 6 I_{LED} analog dimming register. $$I_{LED} = \frac{Code}{63} \times I_{SET}$$ Where Code is the register value.

REG1Ah

Addr: 0x1A				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:4	N/A	R	0000	Reserved.
3:0	PWM6[3:0]	RW	1111	Sets the channel 6 I_{LED} D_{PWM}, 4LSB. D_{PWM} only changes when 8MSB is written.

REG1Bh

Addr: 0x1B				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM6[11:4]	RW	11111111	Sets the channel 6 I_{LED} D_{PWM}, 8MSB. D_{PWM} only changes when the 8MSB are written.

REG1Ch

Addr: 0x1C				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	N/A	R	00	Reserved.
5:0	ICH7[5:0]	RW	111111	Channel 7 I_{LED} analog dimming register. $$I_{LED} = \frac{Code}{63} \times I_{SET}$$ Where Code is the register value.

REG1Dh

Addr: 0x1D				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:4	N/A	R	0000	Reserved.
3:0	PWM7[3:0]	RW	1111	Sets the channel 7 I_{LED} D_{PWM}, 4LSB. D_{PWM} only changes when the 8MSB are written.

REG1Eh

Addr: 0x1E				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM7[11:4]	RW	11111111	Sets the channel 7 I_{LED} D_{PWM}, 8MSB. D_{PWM} only changes when the 8MSB are written.

REG1Fh

Addr: 0x1F				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	N/A	R	00	Reserved.
5:0	ICH8[5:0]	RW	111111	Channel 8 I_{LED} analog dimming register. $$I_{LED} = \frac{Code}{63} \times I_{SET}$$ Where Code is the register value.

REG20h

Addr: 0x20				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:4	N/A	R	0000	Reserved.
3:0	PWM8[3:0]	RW	1111	Sets the channel 8 I_{LED} D_{PWM}, 4LSB. D_{PWM} only changes when the 8MSB are written.

REG21h

Addr: 0x21				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM8[11:4]	RW	11111111	Sets the channel 8 I_{LED} D_{PWM}, 8MSB. D_{PWM} only changes when the 8MSB are written.

REG22h

Addr: 0x22				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	N/A	R	00	Reserved.
5:0	ICH9[5:0]	RW	111111	Channel 9 I_{LED} analog dimming register. $$I_{LED} = \frac{Code}{63} \times I_{SET}$$ Where Code is the register value.

REG23h

Addr: 0x23				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:4	N/A	R	0000	Reserved.
3:0	PWM9[3:0]	RW	1111	Sets the channel 9 I_{LED} D_{PWM}, 4LSB. D_{PWM} only changes when the 8MSB are written.

REG24h

Addr: 0x24				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM9[11:4]	RW	11111111	Sets the channel 9 I_{LED} D_{PWM}, 8MSB. D_{PWM} only changes when the 8MSB are written.

REG25h

Addr: 0x25				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	N/A	R	00	Reserved.
5:0	ICH10[5:0]	RW	111111	Channel 10 I_{LED} analog dimming register. $$I_{LED} = \frac{Code}{63} \times I_{SET}$$ Where Code is the register value.

REG26h

Addr: 0x26				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:4	N/A	R	0000	Reserved.
3:0	PWM10[3:0]	RW	1111	Sets the channel 10 I_{LED} D_{PWM}, 4LSB. D_{PWM} only changes when the 8MSB are written.

REG27h

Addr: 0x27				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM10[11:4]	RW	11111111	Sets the channel 10 I_{LED} D_{PWM}, 8MSB. D_{PWM} only changes when the 8MSB are written.

REG28h

Addr: 0x28				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	NA	R	00	Reserved.
5:0	ICH11[5:0]	RW	111111	Channel 11 I_{LED} analog dimming register. $$I_{LED} = \frac{Code}{63} \times I_{SET}$$ Where Code is the register value.

REG29h

Addr: 0x29				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:4	N/A	R	0000	Reserved.
3:0	PWM11[3:0]	RW	1111	Sets the channel 11 I_{LED} D_{PWM}, 4LSB. D_{PWM} only changes when the 8MSB are written.

REG2Ah

Addr: 0x2A				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM11[11:4]	RW	11111111	Sets the channel 11 I_{LED} D_{PWM}, 8MSB. D_{PWM} only changes when the 8MSB are written.

REG2Bh

Addr: 0x2B				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	N/A	R	00	Reserved.
5:0	ICH12[5:0]	RW	111111	Channel 12 I_{LED} analog dimming register. $$I_{LED} = \frac{Code}{63} \times I_{SET}$$ Where Code is the register value.

REG2Ch

Addr: 0x2C				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:4	N/A	R	0000	Reserved.
3:0	PWM12[3:0]	RW	1111	Sets the channel 12 I_{LED} D_{PWM}, 4LSB. D_{PWM} only changes when the 8MSB are written.

REG2Dh

Addr: 0x2D				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM12[11:4]	RW	11111111	Sets the channel 12 I_{LED} D_{PWM}, 8MSB. D_{PWM} only changes when the 8MSB are written.

REG2Eh

Addr: 0x2E				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	N/A	R	00	Reserved.
5:0	ICH13[5:0]	RW	111111	Channel 13 I_{LED} analog dimming register. $$I_{LED} = \frac{Code}{63} \times I_{SET}$$ Where Code is the register value.

REG2Fh

Addr: 0x2F				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:4	N/A	R	0000	Reserved.
3:0	PWM13[3:0]	RW	1111	Sets the channel 13 I_{LED} D_{PWM}, 4LSB. D_{PWM} only changes when the 8MSB are written.

REG30h

Addr: 0x30				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM13[11:4]	RW	11111111	Sets the channel 13 I_{LED} D_{PWM}, 8MSB. D_{PWM} only changes when the 8MSB are written.

REG31h

Addr: 0x31				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	N/A	R	00	Reserved.
5:0	ICH14[5:0]	RW	111111	Channel 14 I_{LED} analog dimming register. $$I_{LED} = \frac{Code}{63} \times I_{SET}$$ Where Code is the register value.

REG32h

Addr: 0x32				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:4	N/A	R	0000	Reserved.
3:0	PWM14[3:0]	RW	1111	Sets the channel 14 I_{LED} D_{PWM}, 4LSB. D_{PWM} only changes when the 8MSB are written.

REG33h

Addr: 0x33				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM14[11:4]	RW	11111111	Sets the channel 14 I_{LED} D_{PWM}, 8MSB. D_{PWM} only changes when the 8MSB are written.

REG34h

Addr: 0x34				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	N/A	R	00	Reserved.
5:0	ICH15[5:0]	RW	111111	Channel 15 I_{LED} analog dimming register. $$I_{LED} = \frac{Code}{63} \times I_{SET}$$ Where Code is the register value.

REG35h

Addr: 0x35				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:4	N/A	R	0000	Reserved.
3:0	PWM15[3:0]	RW	1111	Sets the channel 15 I_{LED} D_{PWM}, 4LSB. D_{PWM} only changes when the 8MSB are written.

REG36h

Addr: 0x36				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM15[11:4]	RW	11111111	Sets the channel 15 I_{LED} D_{PWM}, 8MSB. D_{PWM} only changes when the 8MSB are written.

REG37h

Addr: 0x37				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	N/A	R	00	Reserved.
5:0	ICH16[5:0]	RW	111111	Channel 16 I_{LED} analog dimming register. $I_{LED} = \frac{Code}{63} \times I_{SET}$ Where Code is the register value.

REG38h

Addr: 0x38				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:4	N/A	R	0000	Reserved.
3:0	PWM16[3:0]	RW	1111	Channel 16 I_{LED} D_{PWM}, 4LSB. D_{PWM} only changes when the 8MSB are written.

REG39h

Addr: 0x39				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM16[11:4]	RW	11111111	Sets the channel 16 I_{LED} D_{PWM}, 8MSB. D_{PWM} only changes when the 8MSB are written.

APPLICATION INFORMATION

LED Current Setting

Connect a resistor from the ISET pin to GND to set I_{LED} for all 16 channels. I_{LED} can be calculated using Equation (6):

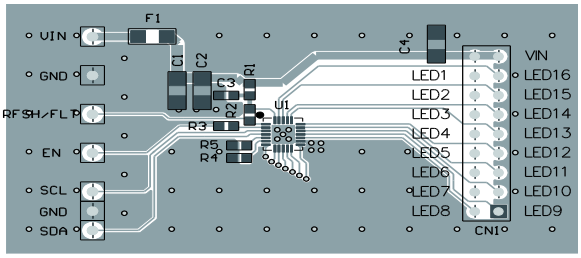
$$I_{LED}(mA) = \frac{1200}{R_{ISET}(k\Omega)} \quad (6)$$

For a maximum 80mA I_{LED}, ensure that V_{IN} ≥ 4.5V to power the IC.

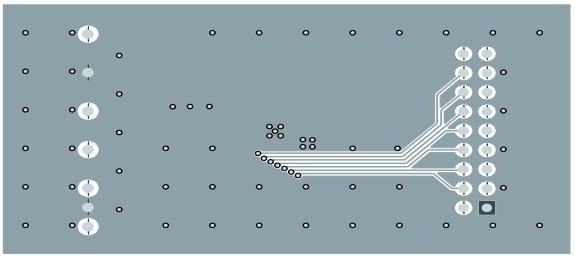
PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 8 and follow the guidelines below:

1. Ensure that the traces from the LED anode to the LEDx pins are wide enough to support the set current (up to 80mA).



Top Layer



Bottom Layer

Figure 8: Recommended PCB Layout (9)

Note:

9) The recommended layout is based on Figure 9 on page 35.

TYPICAL APPLICATION CIRCUITS

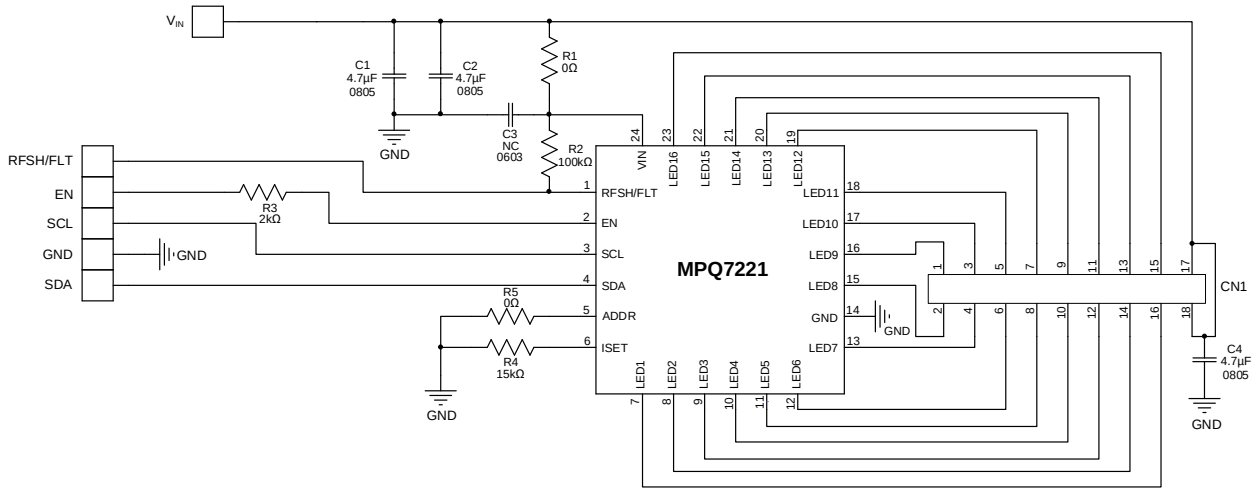


Figure 9: Typical Application Circuit (I_{LED} = 80mA/Channel)

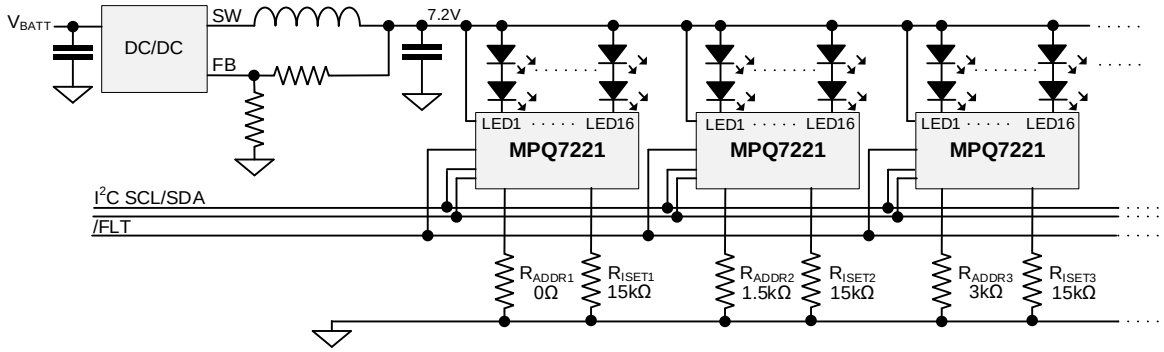
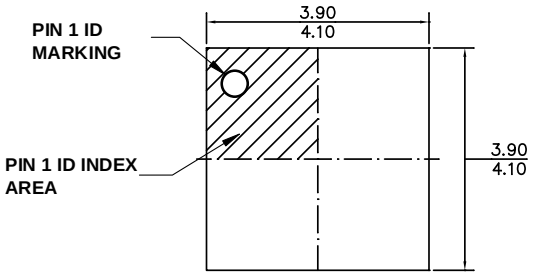


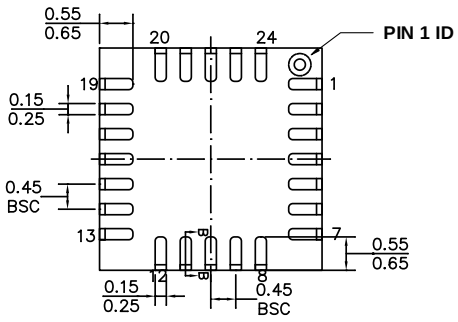
Figure 10: Typical System Application Circuit (2 LEDs in Series, I_{LED} = 80mA/Channel)

PACKAGE INFORMATION

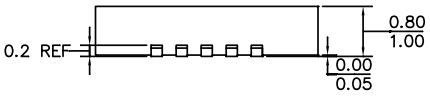
QFN-24 (4mmx4mm)
Wettable Flank



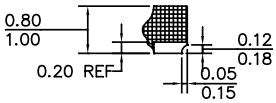
TOP VIEW



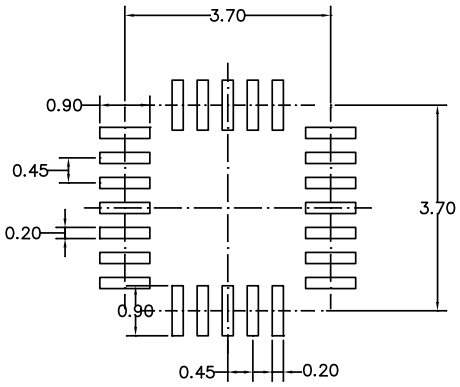
BOTTOM VIEW



SIDE VIEW



SECTION B-B

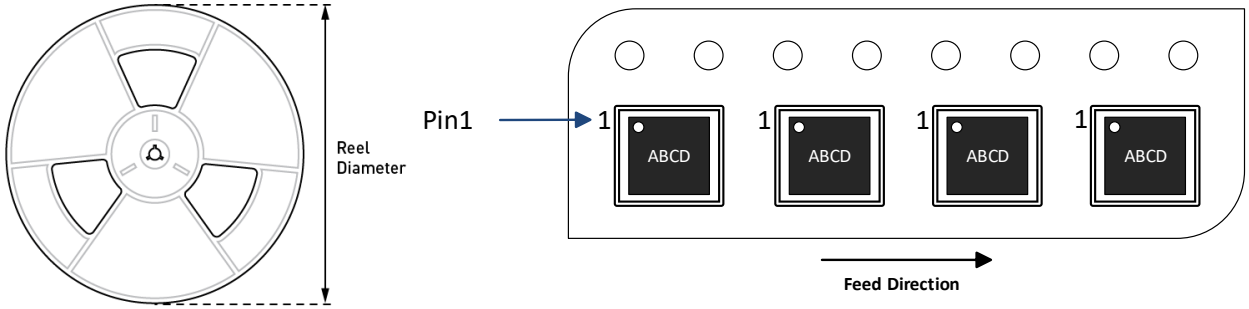


RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ7221GRE-AEC1-Z	QFN-24 (4mmx4mm)	5000	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	6/22/2022	Initial Release	-