89C024XE
HIGH PERFORMANCE 2400 BPS INTELLIGENT MODEM CHIP SET

- Support for Error Correction
- Optional MNP Class 4/5
- CHMOS
- For Public Switched Telephone Network and Unconditioned Leased Lines Applications
- V.22 bis, V.22 A/B, V.21, Bell 212A, and Bell 103 Compatible
- Serial Command Set Compatible with Hayes Smartmodem 2400
- Automatically Adapts to Remote Modem Type with Recognition of Data Rates
- DTMF and Pulse Dialing, with Automatic Selection of Dial Signaling
- On-Chip Hybrid and Billing Delay Timer
- On-Chip Serial Port and Handshake Signals for RS-232/V.24 Interface
- Telephone Line Audio Monitor Output
- Analog/Digital Loopback Diagnostics with Mark/Space Pattern Generation and Error Detection
- Simple Serial Interface to External NVRAM
- Easily Customized Command Set and Features
- Two Chip Intelligent Modem Solution with Minimal External Components
- No External μC Required
- Output Programmable over 16 dB Range
- Dial and Re-dial Capability
- Full Set of Control Signals for DAA Interface
- Local, External, or Slave Timing Options in Synchronous Mode
- Adaptive Equalization
- Capable of Detecting Dial, Busy, Ringback and Modem Answer Tones of Most International Networks
- Auxiliary Relay Control Output

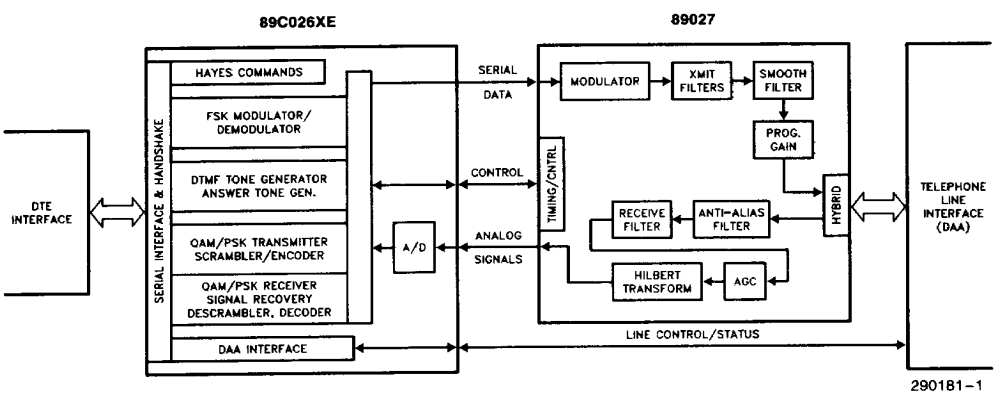

Figure 1. 89C024XE System Block Diagram

October 1988
Order Number: 290181-001

GENERAL DESCRIPTION

Intel 89C024XE is a highly integrated, low power, high performance, intelligent modem chip set. This two chip solution is composed of the 89027 Analog Front End and 89C026XE microcontroller. At 12.96 MHz the microcontroller is capable of executing error correction and data compression routines. The system conforms to the following CCITT and BELL standards.

- CCITT V.22 bis
  2400 bps sync and async
  1200 bps sync and async (fall-back)
- CCITT V.22 A & B
  1200 bps sync and async
  600 bps sync and async (fall-back)
- CCITT V.21
  0 to 300 bps anisochronous
- BELL 212A
  1200 bps sync and async
  300 bps fall-back mode
- BELL 103
  0 to 300 bps anisochronous

The 89C024XE system consists of a 16 bit application specific processor (89C026XE) and an analog front end device (89027). The 89C026XE processor performs all "Digital Signal Processing" algorithm execution for processing the modem signals, as well as providing all modem control functions typically performed by an external processor. The analog front end provides for 2 wire and 4 wire telephone line interface, D/A conversion, and most of the complex filtering functions required in QAM/DPSK/FSK modems. Refer to Figure 1 for a simplified block diagram of the system.

In stand-alone modem applications, the 89C024XE chip set along with a Data Access Arrangement (DAA), a serial NVRAM, and RS-232 driver/receivers and EPROM represent the circuitry required for implementing an auto-dial, auto-answer, 300 to 2400 bps, full duplex Hayes compatible intelligent modem.

A complete set of Industry Standard AT commands is provided for modem configuration and user interface. Virtually all PC software written for the Hayes Smartmodem 2400 can also be used with this chip set. Alternatively, in applications where user proprietary modem control commands and features are desired, the user can replace the 89C024XE internal command module with custom proprietary software.

The 89C024XE has a set of default features. Upon power up, the modem configuration will be in accordance with these default options, unless a different configuration has been saved in the external NVRAM with the &W command.

The 89C024XE modem has built in auto-dialing and auto-answering capabilities. It can be configured to the proper line signaling mode (Tone or Pulse), and to to the type (CCITT or Bell) and speed of the calling or answering modem. It can also detect and identify call set-up signals of telephone networks, allowing unattended data call operation.

A full set compatible with CCITT V.54 diagnostic loop-test features is supported. The chip set also provides a line signal for audio monitoring of call progress, a comprehensive set of DAA control lines for a simple interface to the telephone network, and a full complement of TTL level RS-232/ V.24 handshake signals.

PACKAGING

89027 is available in PLCC and standard plastic DIP packages. The 89C026XE is available in PLCC package.

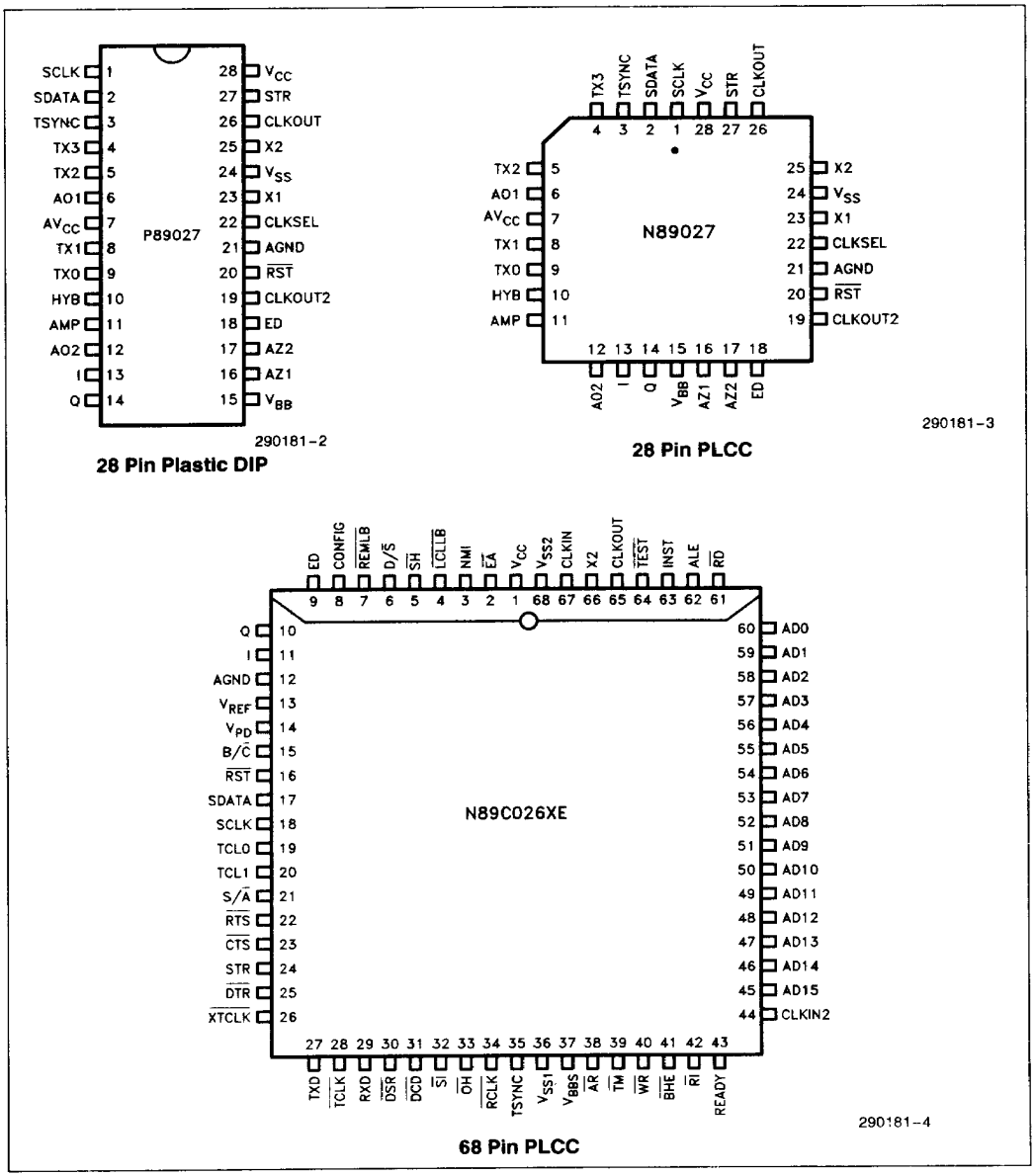

Figure 2. Device Packages

CALL ESTABLISHMENT, TERMINATION AND RETRAIN

The 89C024XE modem system incorporates all protocols and functions required for automatic (or manual) establishment, progress and termination of a data call.

The modem chip-set has a built in auto-dialer, both DTMF and Pulse type, and is capable of automatically adapting to the telephone dial type. The dialing sequence on the telephone link conforms to the CCITT V.25 recommendations. An exception to the V.25 is that the interrupted calling tone will not be transmitted by the calling modem, as is suggested in V.22 bis.

The modem can detect the dial, busy and ringback signals at remote end, and will provide call progress messages to the user. The modem is capable of redialing the last number dialed, by one command.

The modem when configured for auto-answer, will answer an incoming call, remain silent for the two second billing delay interval, before transmitting the answer tones. Afterwards modem to modem identification and handshaking will proceed at a speed and operating mode acceptable to both ends of the link.

The data call can also be setup by manual dialing with the modems set to data mode, or by voice to data transfer by means of mechanical switch (exclusion key), using the $\overline{SH}$ pin. Once set to data mode, the modem handshaking will proceed before the modems will be ready to accept and exchange data.

During data transmission, if one of the modems finds that the received data is likely to have a high bit error rate (indicated by a large mean square error in the adaptive equalizer), it initiates a retrain sequence. This automatic retrain feature is only available at 2400 bps, and conforms to CCITT V.22 bis recommendations.

Disconnection of the data call can be initiated by the DTE at the local end, or by the remote DTE, (if the modem is configured to accept it). Whether $\overline{DTR}$ will initiate a disconnect, depends on the last &D command. Receiving a long space from a remote modem will initiate a disconnect only after a Y1 command. The optional disconnect requests originated by the remote modem, are of two types, (1) disconnect when receiving long-space, and (2) disconnect when received carrier is dropped. The modem chip-set can also be configured to transmit 'long-space' just before disconnection, in each of the aforementioned cases.

Because the CCITT and Bell modem connection protocols are quite different from each other and do not provide recognition of remote modem type (i.e. V.22 bis to 212A), the Intel chip-set provides the additional capability of identifying the remote modem type. This feature is beneficial during the migration phase of the technology from the 1200 bps to 2400 bps. In North America, where the installed base of 1200 bps modems is mostly made-up of 212A type, this feature allows a "Data Base Service Provider" to easily upgrade the existing 212A modems to 2400 bps V.22 bis standard, transparently, to 212A users. Similarly, a user with a 89C024XE based modem system can automatically call data bases with either 212A or V.22 bis modems, without concern over the difference. This feature's benefits are realized in smooth upgrading of data links, with minimum cost and reduced disruption in services. Refer to Table 1 for a detailed description of remote modem compatibility.

SOFTWARE CONFIGURATION COMMANDS

This section lists the 89C024XE commands and registers that may be used while configuring the modem. Commands instruct the modem to perform an action, the value in the associated registers determine how the commands are performed, and the result codes returned by the modem tell the user about the execution of the commands.

The commands may be entered in a string, with or without spaces in between. Any spaces within or between commands will be ignored by the modem. During the entry of any command, the 'backspace' key (CNTRL H) can be used to correct any error. Upper case or lower case characters can be used in the commands. Commands described in the following paragraphs refer to asynchronous terminals using ASCII codes.

Table 1. Remote Modem Compatibility

Originating 89C024XE Modem		Answer Modem: Bell 300	Bell 1200	CCITT 300	CCITT 600	CCITT 1200	CCITT 2400
Bell	300	300	300	—	—	300*	300*
	1200	1200*	1200	—	—	1200	1200
CCITT	300	—	—	300	—	—	—
	600	—	—	—	600	—	—
	1200	1200*	1200	—	—	1200	1200
	2400	1200*	1200		—	1200	2400

Answering 89C024XE Modem		Originating Modem: Bell 300	Bell 1200	CCITT 300	CCITT 600	CCITT 1200	CCITT 2400
Bell	300	300	1200	—	—	1200	1200
	1200	300	1200	—	—	1200	1200
CCITT	300	—	—	300	—	—	—
	600	—	—	—	600	—	—
	1200	300*	1200	—	—	1200	1200
	2400	300*	1200	—	—	1200	2400

* These connection data rates are obtained when connecting 89C024XE based modems end to end. The same results may not be obtained when a 89C024XE based modem is connected to other modems.

Command Set

AT	Attention code.
A	Go off-hook in answer mode
A/	Repeat previous command string
Bn	BELL/CCITT Protocol Compatibility at 1200 bps
Ds	The dialing commands (0-9 A B C D * # P R T S W , ; @)
En	Echo command (En)
Hn	Switch-Hook Control
	If &J1 option is selected, H1 will also switch the auxiliary relay
In	Request Product Code and Checksum
Ln	Speaker Volume
Mn	Monitor On/Off
O	On-Line
Qn	Result Codes
Sn=x	Write S Register
Sn	Read S Register
Vn	Enable Short-Form Result Codes
Xn	Enable Extended Result Code
Yn	Enable Long Space Disconnect
Z	Fetch Configuration Profile
+ + +	The Default Escape Code

& Command Set (Continued)

&C	DCD Options
&D	DTR Options
&F	Fetch Factory Configuration Profile
&G	Guard Tone
&J	Telephone Jack Selection
&L	Leased/Dial-up Line Selection
&M	Async/Sync Mode Selection
&P	Make/Break Pulse Ratio
&R	RTS/CTS Options
&S	DSR Options
&T	Test Commands
&W	Write Configuration to Non Volatile Memory
&X	Sync Clock Source
&Z	Store Telephone Number

CONFIGURATION REGISTERS

The modem stores all the configuration information in a set of registers. Some registers are dedicated to special command and function, and others are bit-mapped, with different commands sharing the register space to store the command status.

S *	Ring to Answer
S1	Ring Count. (Read Only)
S2	Escape Code Character
S3	Carriage Return Character
S4	Line Feed Character
S5	Back Space Character
S6	Wait for Dial Tone
S7	Wait for Data Carrier
S8	Pause Time for the Comma Dial Modifier
S9	Carrier Detect Response Time
S10	Lost Carrier to Hang Up Delay
S11	Not Used
S12	Escape Code Guard Time
S13	Not Used
S14 *	Bit Mapped Option Register
S15	Not Used
S16	Modem Test Options
S17	Not Used
S18 *	Test Timer
S19	Not Used
S20	Not Used
S21 *	Bit Mapped Options Register
S22 *	Bit Mapped Options Register
S23 *	Bit Mapped Options Register
S24	Not Used
S25 *	Delay to DTR (Sync Only)
S26 *	RTS to CTS Delay (Half Dup.)
S27 *	Bit Mapped Options Register

NOTE:
* These S registers can be stored in the NVRAM.

Dial Modifiers

P	Pulse Dial
R	Originate call in Answer Mode
T	Tone Dial
S	Dial a stored number
W	Wait for dial tone
,	Delay a dial sequence
;	Return to command state
	Initiate a flash
@	Wait for quit
	If neither P or T is specified in the command string, the modem automatically selects the proper dial mode.

Example:

Terminal: AT &Z T 1 (602) 555-1212
Modem: OK

Result: Modem stores T16025551212 in the external NVRAM.

The number can be dialed from asynchronous mode by issuing the following command:

Terminal: AT DS
Modem: T16025551212

or by turning on $\overline{DTR}$ when in Synchronous Mode 2. Up to 33 symbols (dial digits and dial modifiers) may be stored. Spaces and other delimiters are ignored and do not need to be included in the count. If more than 33 symbols are supplied, the dial string will be truncated to 33.

APPLICATIONS OVERVIEW

The block diagram of a stand-alone 300 to 2400 bps Hayes compatible modem is depicted in Figure 3. The DAA section shown in this diagram may be obtained with FCC registration, or implemented using the suggested diagram in Figure 4.

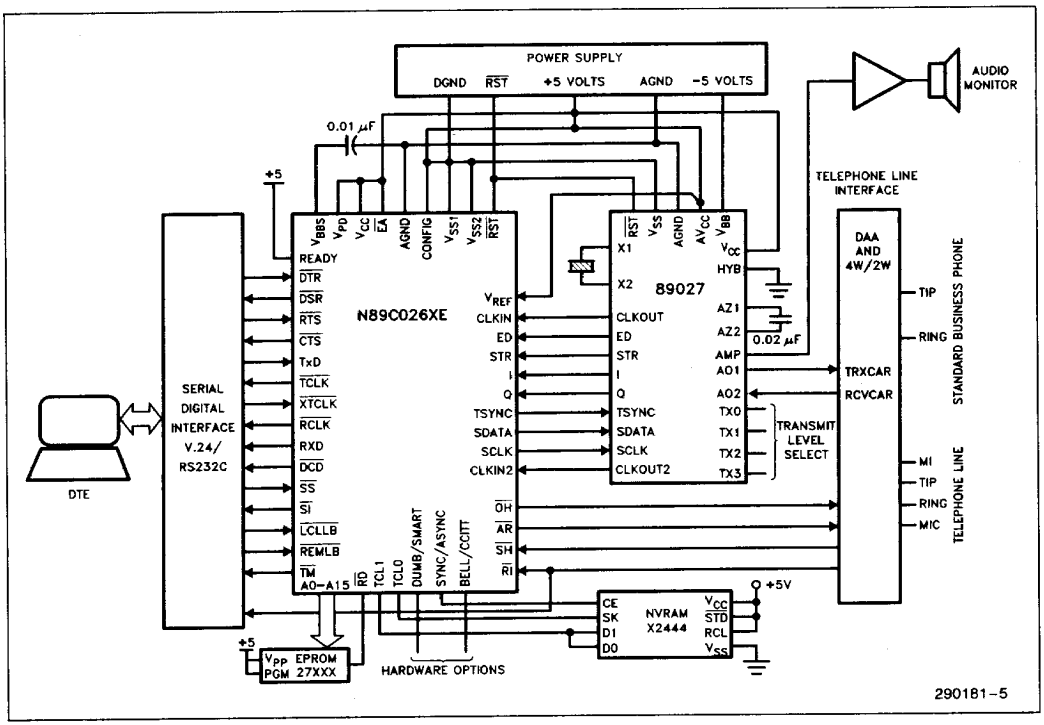

Figure 3. Typical Modem Configuration

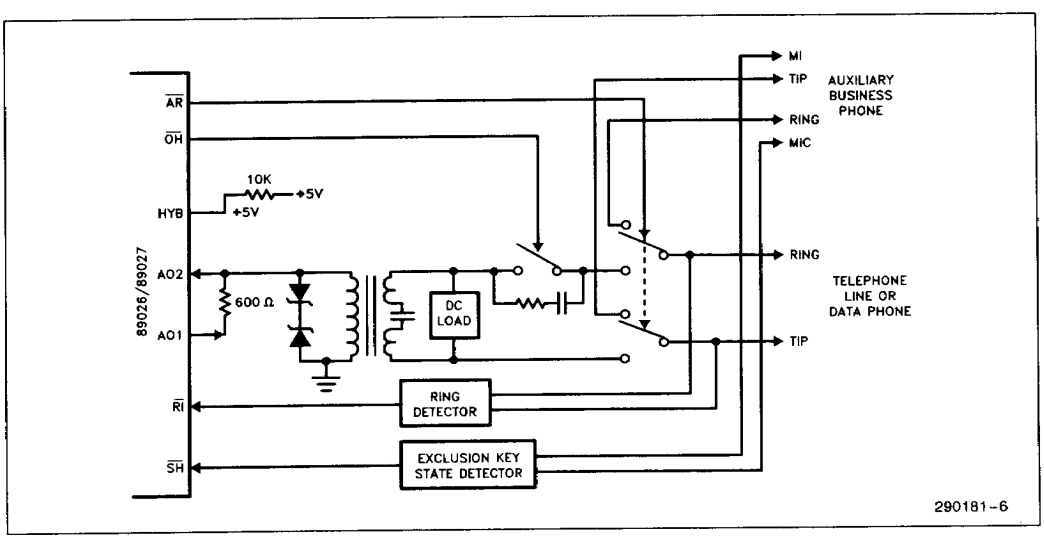

Figure 4. Typical Telephone Line Interface with Built In Hybrid

SYSTEM COMPATIBILITY SPECIFICATIONS

Parameter	Specification
Synchronous	2400 bps ±0.01% V.22 bis 1200 bps ±0.01% V.22 and BELL 212A 600 bps ±0.01% V.22 A,B
Asynchronous	2400, 1200, 600 bps, character asynchronous. 0 - 300 bps anisochronous.
Asynchronous Speed Range	+1% −2.5% default. Extended +2.3% −2.5% range of CCITT standards optional via software customization.
Asynchronous Format	8,9,10,11 bits, including start, stop, parity. Bits 8, 9, 11 optional via S/W customization.
Synchronous Timing Source	Internal, derived from the local oscillator. External, provided by DTE through $\overline{\text{XTCLK}}$. Slave, derived from the received clock.
Telephone Line Interface	Two wire full duplex over public switched network or 4 wire leased lines. On-chip hybrid and billing delay timers. Output level −1 to −16 dBm
Modulation	V.22 bis, 16 point QAM at 600 baud. V.22 and 212A, 4 point DPSK at 600 baud. V.21 and 103, binary phase coherent FSK
Output Spectral Shaping	Square root of 75% raised cosine, QAM/PSK.
Transmit Carrier Frequencies V.22 bis, V.22, 212A V.21 Bell 103 mode	 Originate 1200 Hz ± .01% Answer 2400 Hz ± .01% Originate 'space' 1180 Hz ± .01% Originate 'mark' 980 Hz ± .01% Answer 'space' 1850 Hz ± .01% Answer 'mark' 1650 Hz ± .01% Originate 'space' 1070 Hz ± .01% Originate 'mark' 1270 Hz ± .01% Answer 'space' 2020 Hz ± .01% Answer 'mark' 2225 Hz ± .01%
Receive Carrier Frequency Limits V.22 bis, V.22, 212A V.21 Bell 103	 Originate 2400 Hz ± 7 Hz Answer 1200 Hz ± 7 Hz Originate 'space' 1850 Hz ± 12 Hz Originate 'mark' 1650 Hz ± 12 Hz Answer 'space' 1180 Hz ± 12 Hz Answer 'mark' 980 Hz ± 12 Hz Originate 'space' 2020 Hz ± 12 Hz Originate 'mark' 2225 Hz ± 12 Hz Answer 'space' 1070 Hz ± 12 Hz Answer 'mark' 1270 Hz ± 12 Hz
Energy Detect Sensitivity	Greater than −43 dBm ED is ON. Less than −48 dBm ED is OFF. Signal in dBm measured at AO2.
Line Equalization	Fixed compromise equalization, transmit. Adaptive equalizer for DPSK/QAM, receive.
Diagnostics Available	Local analog loopback. Local digital loopback. Remote digital loopback. Local interface loopback.
Self Test Pattern Generator	Alternate 'ones' and 'zeros' and error detector, to be used along with most loopbacks. A number indicating the bit errors detected is sent to DTE.

RECEIVER PERFORMANCE SPECIFICATIONS

Parameter	Specification
Test condition: Unconditioned 3002 line, across the full dynamic range. The noise bandwidth is 3 KHz flat.	
Random Noise	Typical Bit Error rate of 1 in 100000 or better at 12 dB SNR at 300 bps, 5 dB SNR at 600 bps, 8 dB SNR at 1200 bps and 16 dB SNR at 2400 bps.
Frequency Offsets(1)	± 7 Hz.
Phase Jitter(1)	2400 bps - 15° peak to peak, at up to 300 Hz. 600, 1200 bps - 45° peak to peak, at up to 300 Hz.

NOTE:
1. There are no observable data errors for the received signals, for the above limits of line impairments. These impairments are applied one at a time in absence of noise.

PERFORMANCE SPECIFICATIONS

Parameter	Min	Typ	Max	Units	Comments
DTMF Level		5.0		dBm	at AO1
DTMF Second Harmonic			−35	dB	HYB enabled into 600Ω
DTMF Twist (Balance)		3		dB	
Default DTMF Duration		100		ms	Software Controlled
Pulse Dialing Rate		10		pps	
Pulse Dialing Make/Break		39/61 33/67		% %	US UK, Hong Kong
Pulse Interdigit Interval		785		ms	
Billing Delay Interval			2.1	sec	
Guard Tone Frequency Amplitude Frequency Amplitude		540 −3 1800 −6		Hz dB Hz dB	referenced to High channel transmit. QAM/DPSK Modes Only
Dial Tone Detect Duration		3.0		sec	
Ringback Tone Detect Duration Cadence		 0.75 1.5		 sec 	 Off/On Ratio
Busy Tone Detect Duration Cadence	 0.67	 0.2 	 1.5	 sec 	 Off/On Ratio

89C026XE OVERVIEW

The 89C026XE processor performs data manipulation, signal processing and user interface functions. It supports external ROM and RAM to perform asynchronous, synchronous, and/or custom code with or without high level protocol functions. These options will allow proprietary modem control, functions, call progress management applications to be implemented. A block diagram of the 89C026XE is provided in Figure 5.

89C026XE contains a TTL compatible serial link to DTE equipment, along with a full complement of V.24/RS-232-C control signals. Alternatively, a UART or USART may be used directly to transfer data to and from a microcomputer bus. The industry standard AT command set is supported by the 89C026XE, facilitating compatability between 89C024XE and most PC software written for the AT command set.

During transmit operation, the 89C026XE synthesizes DTMF tones and the 300 BPS FSK modem signal and transmits them to the 89027 as digitized amplitude samples. During 1200 and 2400 BPS operation, DPSK and QAM is used to send 2 to 4 bits of information respectively at 600 baud to the AFE. Because the QAM coding technique is an inherently synchronous transmission mechanism, in the case of asynchronous QAM transmission, the asynchronous data is synchronized by adding or deleting stop bits. Following the synchronization process, the 89C026XE transmits digitized phase and amplitude samples to 89027 over the high speed serial link.

In the receive operation, the information is received by the 89C026XE from the 89027 as two signals which are 90 degrees phase shifted from each other. These analog signals are then digitized by the A/D converter resident on the 89C026XE. By using DSP algorithms, the received signals are processed using adaptive equalization for telephone line delay, amplitude distortion and gain adjustment is executed and the signal demodulated. Following demodulation, the data is unscrambled, and if necessary, returned to asynchronous format.

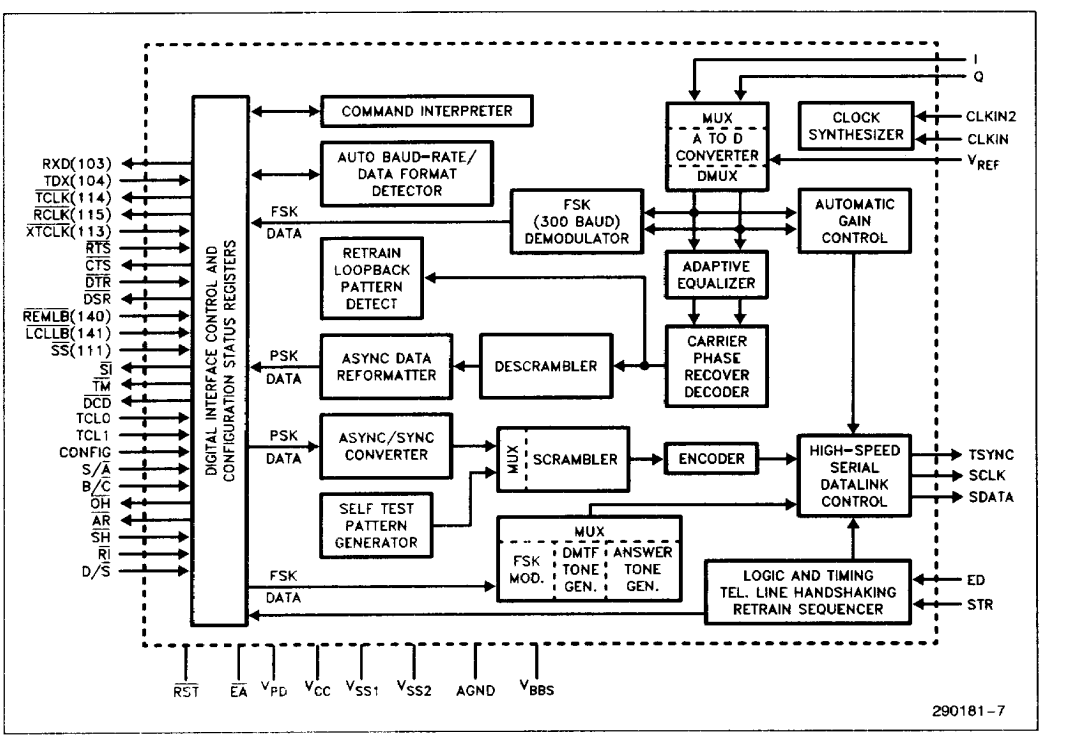

Figure 5. 89C026XE Block Diagram

89C026XE PINOUT

Symbol	Function (89026)	Direction	Pin No.
CLKIN	12.96 MHz master clock from 89027	In	67
CLKIN2	270 KHz from 89027	In	44
$\overline{RST}$	Chip reset (active low)	In	16
I	In-phase received signal	In	11
Q	Quadrature-phase received signal	In	10
STR	Symbol Timing from 89027	In	24
ED	Energy Detect input	In	9
TSYNC	Transmitter sync pulse to 89027	Out	35
SDATA	Serial Data to 89027	Out	17
SCLK	Serial Clock to 89027	Out	18
$\overline{OH}$	Off-Hook control to DAA	Out	33
$\overline{SH}$	Switch-Hook from dataphone	In	5
$\overline{RI}$	Ring Indicator from DAA	In	42
$\overline{AR}$	Aux Relay control to DAA	Out	38
TCL1	NVRAM Data I/O	I/O	20
TCL0	NVRAM CLK	Out	19
B/$\overline{C}$	103/V.21 default option	In	15
S/$\overline{A}$	NVRAM CE	Out	21
D/$\overline{S}$	Dumb/$\overline{Smart}$ mode select	In	6
CONFIG	Custom Firmware Disable	In	8
$\overline{TM}$	Test Mode Indicator	Out	39
$\overline{TXD}$	Transmitted data from DTE	In	27
$\overline{RXD}$	Received data to DTE	Out	29
$\overline{RTS}$	Request to send from DTE	In	22
$\overline{CTS}$	Clear to Send to DTE	Out	23
$\overline{DSR}$	Data Set Ready to DTE	Out	30
$\overline{DCD}$	Data Carrier Detect to DTE	Out	31
$\overline{DTR}$	Data Terminal Ready from DTE	In	25
$\overline{RCLK}$	Received clock to DTE	Out	34
$\overline{TCLK}$	Transmit clock to DTE	Out	28
$\overline{XTCLK}$	External timing clock from DTE	In	26
$\overline{SI}$	Speed Indicator to DTE	Out	32
$\overline{REMLB}$	Remote Loopback Command from DTE	In	7
$\overline{LCLLB}$	Local Loopback Command from DTE	In	4
V_{CC}	Positive power supply (+5V)	+5V	1
V_{PD}	Ram back-up power	+5V	14
V_{REF}	A/D converter reference	+5V	13
V_{SS1}	Digital ground	GND	36
V_{SS2}	Digital ground	GND	68
AGND	Analog ground	AGND	12
V_{BBS}	Back-bias generator output	Out	37
$\overline{EA}$	External Memory enable	In	2
AD0-AD15	External memory access address/data(5)	I/O	60-45
$\overline{AA}$	Auto Answer	Out	60
$\overline{JS}$	Jack Select	Out	59

89C026XE PINOUT (Continued)

Symbol	Function (89026)	Direction	Pin No.
NMI	No-maskable Interrupt(V_{SS})(1)	In	3
X2	Crystal output(NC)(2)	Out	66
CLKOUT	Clk output	Out	65
$\overline{TEST}$	Factory test(V_{CC})(3)	In	64
INST	External memory instruction fetch	Out	63
ALE	Address latch enable	Out	62
$\overline{RD}$	External memory read	Out	61
READY	External memory ready(V_{CC})(3)	In	43
$\overline{BHE}$	External memory bus high enable	Out	41
$\overline{WR}$	External memory write	Out	40

NOTES:
1. Pins marked with (V_{SS}) must be connected to V_{SS}.
2. Pins marked with (NC) are to be left unconnected.
3. Pins marked with (V_{CC}) must be connected to V_{CC}.
4. With internal ROM enabled, AD0-AD1 are used as $\overline{AA}$ and $\overline{JS}$.

89C026XE PIN DESCRIPTION

$\overline{XTCLK}$

Transmitter timing from DTE, when external clock option is selected.

TXD

The serial data from DTE to be transmitted on the line. A logic 'high' is mark. In synchronous mode, 89026 samples this data on the rising edges of $\overline{TCLK}$.

$\overline{TCLK}$

Clock output from 89026 as timing source for data exchange from DTE to modem. Serial data is read on the rising edges of the $\overline{TCLK}$. This output is High in asynchronous mode.

RXD

The serial data to DTE. 'Mark' is a logic High. In synchronous mode, the rising edge of $\overline{RCLK}$ occurs in the middle of RXD.

$\overline{RCLK}$

Synchronous clock output. Rising edge of $\overline{RCLK}$ occurs in the middle of each RXD bit. This pin remains High in asynchronous mode.

V_{BBS}

This pin to be connected to AGND through a 0.01 μF capacitor.

$\overline{TM}$

A Low indicates maintenance condition in the modem.

$\overline{DCD}$

In async operation, $\overline{DCD}$ remains Low regardless of data carrier (default), or it can be programmed to indicate received carrier signal is within the required timing and amplitude limits. In sync operation Low indicates the received carrier signal is within the required timing and amplitude limits.

$\overline{DSR}$

Low indicates modem is off-hook, and it is in data transmission mode, and the answer tone is being exchanged. $\overline{CTS}$ Low indicates modem is prepared to accept data.

$\overline{RTS}$

In async mode $\overline{RTS}$ is ignored. Under command control, in sync mode $\overline{RTS}$ can be ignored, or the modem can respond with a Low on $\overline{CTS}$.

$\overline{DTR}$

&D0 command will cause the modem to ignore $\overline{DTR}$. For &D1 the modem assumes the asynchronous command state on a Low to High transition of the $\overline{DTR}$ circuit. The &D2 command does the same as &D1 except the state of $\overline{DTR}$ will enable/disable auto answer. A Low to High transition of $\overline{DTR}$ after the &D3 command will cause the modem to assume the initialization state.

B/$\overline{C}$

Low configures the modem to CCITT V.21. High will configure the modem to Bell 103, when at 300 bps speed. This pin only affects the modem in 300 bps operation.

TCL1, TCL0

These pins are used as the serial clock and data for interface to an NVRAM. Refer to Figure 3. TCL0 is used to output a clock and serial data is read in on TCL1.

$\overline{AR}$

This Auxiliary relay control is for switching a relay for voice or data calls. High is voice, Low is data.

$\overline{RI}$

A Low signal from DAA indicates line ringing. This input is ignored when the modem is configured for leased line. This signal should follow the ring cadence.

$\overline{OH}$

Low controls off hook. High indicates on hook. When dialing, this control is used to pulse dial the line.

$\overline{SH}$

Used as a telephone voice to data switch or vice versa. Any logic level transition will toggle the modem state. This input is ignored, if a software command attempts to switch the modem between voice and data.

$\overline{AA}$

Used as an indicator for Auto Answer status and Ring indicator. Active low.

$\overline{LCLLB}$

A Low will set the modem in the local analog loopback test mode. Logic Low levels applied simultaneously to $\overline{REMLB}$ and $\overline{LCLLB}$ pins, sets the modem to the local digital loopback.

$\overline{REMLB}$

A logic Low on this pin initiates a remote loopback condition.

$\overline{SI}$

Selects one of the two data rates or ranges of rates in the DTE to correspond to the rate in modem. Low selects the higher rate (2400 CCITT/1200 BELL) or range of rates. High selects the Low rate or range of rates.

D/$\overline{S}$

A Low on this pin will indicate the smart mode which will respond to all commands. A High will ignore all commands.

V_{REF}

Voltage reference for the analog to digital converter should be connected to the 89027 AVcc.

V_{PD}

The internal RAM power down supply voltage to be connected to 5 Volts during normal operation.

S/$\overline{A}$

The function of this pin is re-defined as external NVRAM CE.

CONFIG

Low indicates availability of custom software modules in off-chip memory.

$\overline{EA}$

When high, memory access from address 2000H to 4000H are directed to on-chip ROM. When low, all Memory access is directed to off-chip memory.

$\overline{JS}$

Low is used to pulse A and A1 leads to control a 1A2 Key System jack.

89C026XE ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	−10 to +80° C
Storage Temperature	−40 to +125° C
Voltage from Any Pin to V_{SS} or AGND	−0.3V to +7.0V
Average Output Current from Any Pin	10 mA
Power Dissipation	1.5 Watts

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

NOTICE: Specifications contained within the following tables are subject to change.

OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
TA	Ambient Temperature Under Bias	0	+70	C
V_{CC}	Digital Supply Voltage	4.75	5.25	V
FREQ	CLKIN Frequency 12.96 Mhz	−0.01%	+0.01%	
CLKIN2	Frequency 270 KHz	−0.01%	+0.01%	
V_{PD}	Power-Down Supply Voltage	4.75	5.25	V

NOTE:
V_{BBS} should be connected to AGND through a 0.01 μF capacitor. AGND, V_{ss} and the 89027 V_{ss}, AGND must be nominally at the same potential.

DC CHARACTERISTICS

Symbol	Parameter	Min	Max	Units	Comments
V_{IL}	Input Low Voltage	−0.3	+0.8	V	Except $\overline{RST}$
V_{IL1}	Input Low Voltage,$\overline{RST}$	−0.3	+0.7	V	
V_{IH}	Input High Voltage	2.0	V_{cc}+.5	V	Except $\overline{RST}$, NMI, CLKIN
V_{IH1}	Input High Voltage, $\overline{RST}$ Rising	2.4	V_{cc}+.5	V	
V_{IH2}	Input High Voltage, $\overline{RST}$ Falling	2.1	V_{cc}+.5	V	
V_{IH3}	Input High Voltage, NMI, CLKIN	2.4	V_{cc}+.5	V	
V_{OL}	Output Low Voltage		0.45	V	See Note 1.
V_{OH}	Output High Voltage	2.4		V	See Note 2.
I_{CC}	V_{cc} Supply Current		55	mA	All outputs disconnected
I_{PD}	V_{PD} Supply Current		1	mA	Normal operation and Power-Down
I_{REF}	V_{REF} Supply Current		15	mA	
I_{LI}	Input Leakage Current		±10	μA	V_{in}=0 to V_{cc} See Note 3
I_{IH}	Input High Current to $\overline{EA}$		100	μA	V_{IH}=2.4V
I_{IL}	Input Low Current		−100	μA	V_{IL}=0.45V See Note 4
I_{IL1}	Input Low Current to $\overline{RST}$		−2	mA	V_{IL}=0.45V
I_{IL2}	Input Low Current S/$\overline{A}$, $\overline{SH}$, $\overline{RI}$, READY		−50	μA	V_{IL}=0.45V
C_s	Pin Capacitance (Any Pin to V_{ss})		10	pF	1 MHz

NOTES:
1. I_{OL} = 0.36 mA for pins TCL0, TCL1, B/$\overline{C}$, $\overline{RTS}$, $\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$, $\overline{SI}$, $\overline{AR}$, and $\overline{OH}$. Also if AD0 - AD15 are configured as I/O ports.
I_{OL} = 2.0 mA for $\overline{TM}$, CLKOUT, ALE, $\overline{BHE}$, $\overline{RD}$, $\overline{WR}$, RXD, $\overline{TCLK}$, and AD0 - AD15 when used as external memory bus.
2. I_{OH} = −20 μA for pins TCL0, TCL1, B/$\overline{C}$, $\overline{RTS}$, $\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$, $\overline{SI}$, $\overline{AR}$, and $\overline{OH}$.
I_{OH} = −200 μA for $\overline{TM}$, CLKOUT, ALE, $\overline{BHE}$, $\overline{RD}$, $\overline{WR}$, RXD, $\overline{TCLK}$, and AD0 - AD15 when used as external memory bus. AD0 - AD15 when used as I/O ports, have open-drain outputs.
3. For pins $\overline{DTR}$, $\overline{XTCLK}$, TXD, D/$\overline{S}$, $\overline{REMLB}$, $\overline{LCLLB}$, CONFIG, AD0-AD15.
4. TCL0, TCL1, B/$\overline{C}$, $\overline{RTS}$.
5. Power must be applied to the device in the following sequence: V_{ss} first, then V_{cc}.

A.C. CHARACTERISTICS V_{CC}, V_{PD} = 4.75V to 5.25V; T_A = 0°C to 70°C; CLKIN = 12.96 MHz

Test Conditions: Load capacitance on output pins = 80 pF
T_{OSC} = 1/12.96 MHz

The memory system must meet these specifications to work with 89C026XE

Symbol	Parameter	Min	Max	Units	Notes
T_{AVYV}	Address Valid to READY Setup		$2T_{OSC}-75$	ns	
T_{LLYV}	ALE Low to READY Setup		$T_{OSC}-72$	ns	
T_{YLYH}	Non READY Time	No upper limit		ns	
T_{CLYX}	READY Hold after CLKOUT Low	0	$T_{OSC}-30$	ns	(Note 1)
T_{LLYX}	READY Hold after ALE Low	$T_{OSC}-15$	$2T_{OSC}-40$	ns	(Note 1)
T_{AVGV}	Address Valid to Buswidth Setup		$2T_{OSC}-70$	ns	
T_{LLGV}	ALE Low to Buswidth Setup		$T_{OSC}-70$	ns	
T_{CLGX}	Buswidth Hold after CLKOUT Low	0		ns	
T_{AVDV}	Address Valid to Input Data Valid		$3T_{OSC}-60$	ns	
T_{RLDV}	$\overline{RS}$ Active to Input Data Valid		$T_{OSC}-23$	ns	
T_{CLDV}	CLKOUT Low to Input Data Valid		$T_{OSC}-50$	ns	
T_{RHDZ}	End of $\overline{RD}$ to Input Data Float		$T_{OSC}-20$	ns	
T_{RXDX}	Data Hold after $\overline{RD}$ Inactive	0		ns	

NOTES:
1. If max is exceeded, additional wait states will occur.

The 89C026XE will meet these specifications:

Symbol	Parameter	Min	Max	Units	Notes
F_{CLKIN}	CLKIN Frequency	12.95870	12.96129	MHz	12.96 ±0.01%
F_{CLKIN2}	CLKIN2 Frequency	269.973	270.027	KHz	270 ±0.01%
T_{XHCH}	XTAL1 High to CLKOUT High or Low	40	110	ns	(Note 1)
T_{CLCL}	CLKOUT Cycle Time	$2T_{OSC}$		ns	
T_{CHCL}	CLKOUT High Period	$T_{OSC}-10$	$T_{OSC}+10$	ns	
T_{CLLH}	CLKOUT Falling Edge to ALE Rising	−5	15	ns	
T_{LLCH}	ALE Falling Edge to CLKOUT Rising	−15	15	ns	
T_{LHLH}	ALE Cycle Time	$4T_{OSC}$		ns	
T_{LHLL}	ALE High Period	$T_{OSC}-10$	$T_{OSC}+10$	ns	
T_{AVLL}	Address Setup to ALE Falling Edge	$T_{OSC}-15$		ns	
T_{LLAX}	Address Hold after ALE Falling Edge	$T_{OSC}-35$		ns	
T_{LLRL}	ALE Falling Edge to $\overline{RD}$ Falling Edge	$T_{OSC}-40$		ns	
T_{RLCL}	$\overline{RD}$ Low to CLKOUT Falling Edge	10	30	ns	
T_{RLRH}	$\overline{RD}$ Low Period	$T_{OSC}-5$		ns	
T_{RHLH}	$\overline{RD}$ Rising Edge to ALE Rising Edge	T_{OSC}	$T_{OSC}+25$	ns	(Note 2)
T_{RLAX}	$\overline{RD}$ Low to Address Float	10		ns	
T_{LLWL}	ALE Falling Edge to $\overline{WR}$ Falling Edge	$T_{OSC}-10$		ns	
T_{CLWL}	CLKOUT Low to $\overline{WR}$ Rising Edge	0	25	ns	
T_{QVWH}	Data Stable to $\overline{WR}$ Rising Edge	$T_{OSC}-20$		ns	
T_{CHWH}	CLKOUT High to $\overline{WR}$ Rising Edge	−10	10	ns	
T_{WLWH}	$\overline{WR}$ Low Period	$T_{OSC}-30$		ns	
T_{WHQX}	Data Hold after $\overline{WR}$ Rising Edge	$T_{OSC}-10$		ns	
T_{WHLH}	$\overline{WR}$ Rising Edge to ALE Rising Edge	$T_{OSC}-10$	$T_{OSC}+15$	ns	(Note 2)
T_{WHBX}	$\overline{BHE}$, INST HOLD after $\overline{WR}$ Rising Edge	$T_{OSC}-10$		ns	

NOTES:
1. This specification is not tested, but is verified by design analysis and/or derived from other tested parameters.
2. Assuming back-to-back bus cycles.

WAVEFORM

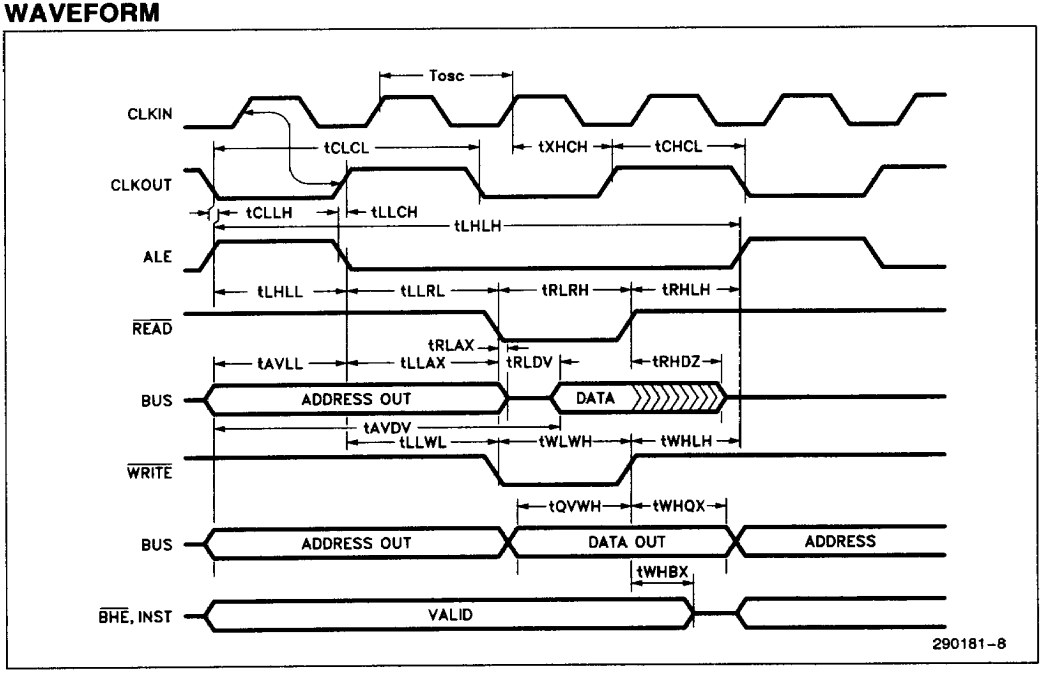

Figure 6. Bus Signal Timings

89027 OVERVIEW

The 89027 is a 28 pin CMOS analog front end device, which performs most of the complex filtering functions required in modem transmitters and receivers. A general block diagram of this chip is provided in Figure 7. Most of the analog signal processing functions in this chip are implemented with CMOS switched capacitor technology. The 89027 functions are controlled by 89C026XE, through a high speed serial data link.

During FSK transmit operation, the 89027 receives digitally synthesized mark and space sinusoid amplitude information from the 89C026XE. The 89027 converts the signal to its analog equivalent, filters it, and transmits it to the telephone line. For QAM transmission, the signal constellation points are transferred to the 89027. This information is modulated into an analog signal, passed through spectral shaping filters, combined with the necessary guard tone, smoothed by a low pass filter, and transmitted to the line. Prior to transmitting either FSK or QAM signals to the telephone line, the 89027 adjusts the signal gain through an on-board programmable gain amplifier.

During the receive operation, the received FSK and QAM signals are passed through anti-alias filters, bandsplit filters, automatic gain control and carrier detect circuits, a Hilbert transform filter, and the output sent to the 89C026XE processor as analog signals.

Other functions provided by the 89027 are: an on-board two wire to four wire circuit with disable capability, an audio monitor output with software configurable gain, and a programmable gain transmit signal.

The 89027 is available in 28 pin plastic DIP and PLCC packages.

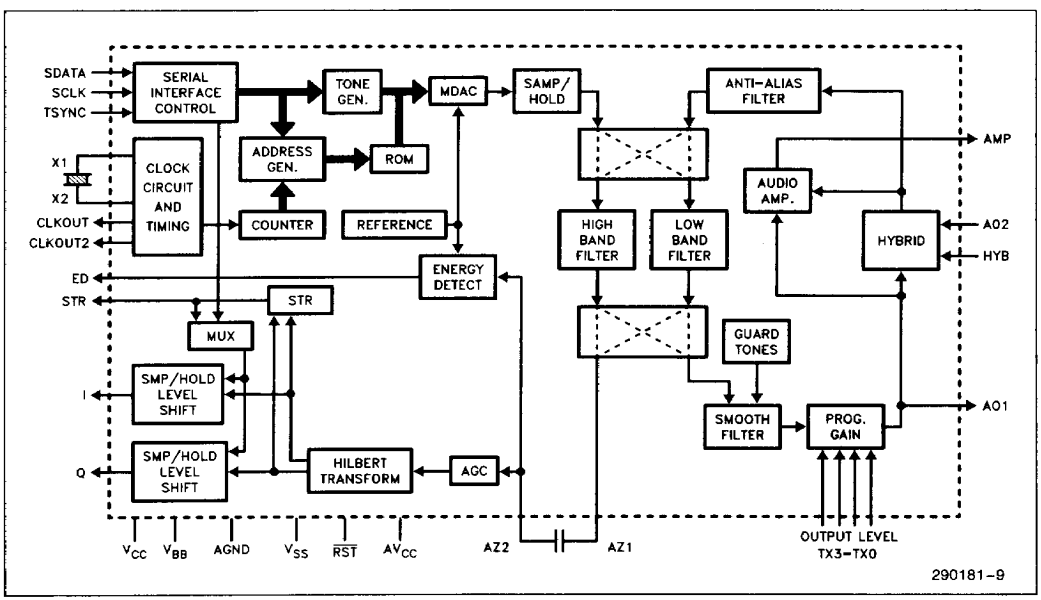

Figure 7. 89027 Block Diagram

89027 PINOUT

Symbol	Function (89027)	Direction	Pin No.
V_{CC}	Positive Power Supply (Digital)	+5V	28
V_{BB}	Negative Power Supply	−5V	15
V_{SS}	Digital Ground	DGND	24
AGND	Analog Ground	AGND	21
AV_{CC}	Positive Power Supply (Analog)	+5	7
X1	Xtal Oscillator	In	23
X2	Xtal Oscillator	Out	25
CLKOUT	12.96 MHz Clock Output to 89C026XE	Out	26
CLKOUT2	270 KHz Clock Output to 89C026XE	Out	19
$\overline{RST}$	Chip reset (active low)	In	20
HYB	Enable on-chip hybrid (1)	In	10
AZ1	Auto-zero capacitor	Out	16
AZ2	Auto-zero capacitor	In	17
SDATA	Serial data from 89C026XE	In	2
SCLK	Serial clock from 89C026XE	In	1
TSYNC	Transmitter sync from 89C026XE	In	3
STR	Symbol timing to 89C026XE	Out	27
ED	Receiver energy detect to 89C026XE	Out	18
I	In phase received signal to 89C026XE	Out	13
Q	Quadrature-phase received signal to 89C026XE	Out	14
AO1	Transmitter output	Out	6
AO2	Receiver input	In	12
AMP	Output to monitor speaker	Out	11
TX0	Transmitter level control (LSB) (1)	In	9
TX1	Transmitter level control(1)	In	8
TX2	Transmitter level control (1)	In	5
TX3	Transmitter level control (MSB)(1)	In	4

NOTE:
1. When held high, these pins should be connected through 10K resistors to A_{VCL}

89027 Pinout Description

TX0-3

These four pins control the transmitted signal level. The output level can be adjusted from −1 dBm to −16 dBm in 1 dB steps.

HYB

This pin enables the on-chip hybrid. A line impedance matching network must be connected between AO1 and AO2 when HYB is enabled. If HYB is disabled and an external 4W/2W hybrid is used, the hybrid receive path must be amplified by 6 dB.

AO1

Transmitter output.

AO2

Receiver input.

AMP

This output can be used to monitor the call progress tones and operation of the line.

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... −10 to +80° C
Storage Temperature ..... −40 to +125° C
All Input and Output Voltages with Respect to V_{BB} ..... −0.3V to +13.0V
All Input and Output Voltages with Respect to V_{CC} & AV_{CC} ..... −13.0V to 0.3V
Power Dissipation 1.35W
Voltage with Respect to V_{SS}(1) ..... −0.3V to 6.5V

NOTE:
1. Applies to pins SCLK, SDATA, TSYNC, $\overline{RST}$, HYB, TX0–TX3 only.

POWER DISSIPATION

Ambient Temp = 0° to 70° C, V_{CC} = AV_{CC} = 5 ± 5%, V_{SS} = AGND = 0.

Symbol	Parameter	Min	Typ	Max	Units
$Aicc_1$	AV_{CC} Operating Current		19	25	mA
Icc_1	V_{CC} Operating Current		7	10	mA
Ibb_1	V_{BB} Operating Current		−19	−25	mA
$Aicc_s$	AV_{CC} Standby Current		0.2	1	mA
Icc_s	V_{CC} Standby Current		7	10	mA
Ibb_s	V_{BB} Standby Current		−0.6	−2	mA
Pdo	Operating Power Dissipation		225	300	mW
Pds	Standby Power Dissipation		40	70	mW

DC CHARACTERISTICS

(Ta = 0°C to 70°C, AV_{CC} = V_{CC} = 5V ±5%, V_{BB} = 5V ±5%, AGND = V_{SS} = 0V), supply voltage must be at the same potential as the 89C026XE power supply. Typical Values are for Ta = 25°C and nominal power supply values. Power must be applied in the following sequence: V_{SS}, AGND, V_{BB}, V_{CC}, and AV_{CC}. V_{CC}, AV_{CC} and 89C026XE V_{REF} must be nominally at the same potential.

Inputs: TX0, TX1, TX2, TX3, HYB, $\overline{RST}$
Outputs: CLKOUT

Symbol	Parameter	Min	Max	Units	Test Condition
Iil	Input Leakage Current	−10	+10	μA	$V_{SS} \le Vin \le V_{CC}$
Vil	Input Low Voltage	V_{SS}	0.8	V	
Vih	Input High Voltage	2.0	V_{CC}	V	
Vol	Output Low Voltage		0.4	V	$Iol \ge -1.6mA$,1 TTL load
Voh	Output High Voltage	2.4		V	$Ich \le 50\mu a$, 1 TTL load
V_{co1}	CLKOUT Low Voltage		0.4	V	C_1 = 60 pF
Vcoh	CLKOUT High Voltage	2.4		V	C_1 = 60 pF

AC CHARACTERISTICS (T_a = 25°C, V_{CC} = AV_{CC} = 5 V, V_{SS} = AGND = 0, V_{BB} = −5 V)

ANALOG INPUTS: AO2

Parameter	Min	Typ	Max	Units	Test Condition
AO2 Input Voltage Range			−9	dBm	
AO2 Input Resistance		10		Mohms	−3.5V < Vin < +3.5V
AO2 Allowed DC offset	−30		+30	mV	Relative to AGND

AUTO ZERO CAPACITANCE

Capacitance = 0.015 μF
Tolerance = ±10 %
Voltage Rating = 10V
Type = Non-Electrolytic, low leakage.

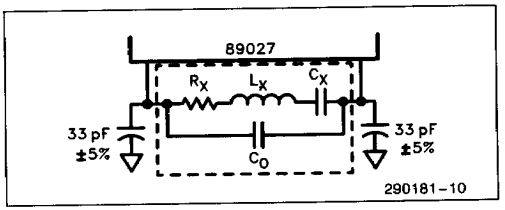

Figure 8. Crystal Equivalent Circuit

CRYSTAL REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Comments
Frequency Accuracy (0°C–70°C)	−0.0035%		+0.0035%	12.960 Mhz	Refer to Figure 8
Rx		10	16	ohms	
Cx		0.024		pF	
Co	5.1	5.6	6.1	pF	
C_L	−5%		+5%	33 pF	2 Load Capacitors

Crystal Type: Series Resonant

ANALOG OUTPUTS: A01, AMP

Parameter	Min	Typ	Max	Units	Comments
Load Resistance AO1 AMP	 600 10			 ohms Kohms	
Load Capacitance AMP			 100	 pF	
Audio Amp Gain AO1 to Amp		−9 −18 −24 −75		dB dB dB dB	Software Selectable
Audio Amp Gain(1) AO2 to Amp		+12 +3 −4 −65		dB dB dB dB	Software Selectable

NOTE:
1. Assumes on-chip hybrid is enabled. When on-chip hybrid is disabled, gain with respect to AO2 is reduced by 6 dB.

TRANSMIT LEVEL

OUTPUT TRANSMIT LEVEL (1)	TX 3,2,1,0	Typ	Units
	0 0 0 0	+5	dBm
	0 0 0 1	+4	dBm
	•	•	•
	•	•	•
	•	•	•
	1 1 1 0	−9	dBm
	1 1 1 1	−10	dBm

NOTE:
1. For FSK, PSK, QAM xmit signal measured at AO1.

REFERENCE MANUAL

Overview

For reference purposes please refer to the 89024 Reference Manual which also contains a full description of the AT commands and S-registers supported by the 89C024XE Modem chip set.

ORDERING INFORMATION

Intel literature number: 296235-001