82307
DMA/Micro Channel ARBITRATION CONTROLLER

- **8 Channel DMA Controller (8/16-Bit)**
- **Integrated Central Arbitration Control Point**
- **Refresh Address Generation/Cycling**
- **Numerics Co-processor Interface**
- **Address Decoding**
  - **— Numeric Coprocessor**
  - **— Interrupt Controller**
  - **— POS Address Space for Expansion Slots**
- **Low Power CHMOS Technology**
- **132-Pin Plastic Quad Flat Pack Packaging**
  (See Packaging Spec., Order # 231369)

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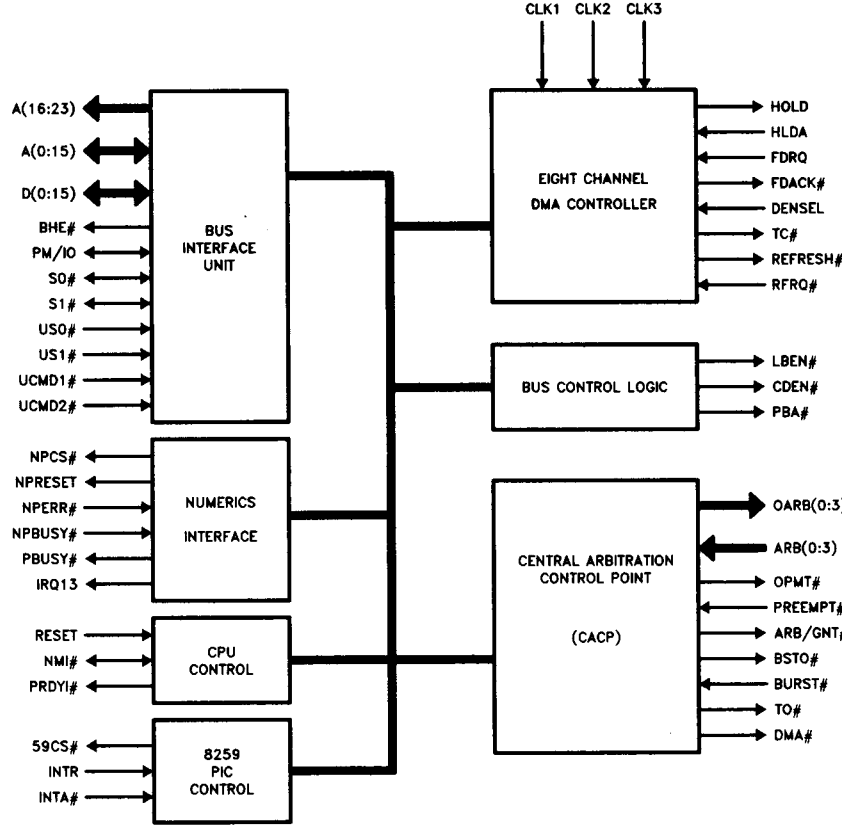
The 82307 DMA/Micro Channel Arbitration Controller is a register level implementation of the equivalent VLSI device in IBM Micro Channel systems. The Central Arbitration Control Point (CACP) as defined in the Micro Channel Architecture for bus arbitration is integrated in this VLSI device.

The 82307 also integrates the Address decoder logic for generating decodes for numeric coprocessor, Interrupt controllers and POS address space.



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DMA FUNCTION

The 82307 features eight 8/16-bit channels, 24-bit addressing capability, and operates in two-cycle transfer mode as defined in the Micro Channel architecture. The DMA controller owns the bus for both halves of the transfer cycle.

The DMA function in the 82307 also supports the motherboard Floppy Disk Controller. Upon receiving the DMA request from the FDC, the DMA controller arbitrates for the Micro Channel bus on behalf of the FDC. The FDC is acknowledged once the bus is granted to initiate the data transfer.

Micro Channel ARBITRATION

The other major function of the 82307 DMA controller is to provide Micro Channel Arbitration. It provides full Micro Channel bus arbitration capability according to the 18-level priority scheme. During normal operation priority 0–15 are assigned with 15 being the lowest priority for the CPU. Priority level −1 which has the higher priority than 0 is also assigned to CPU (switched from 15 to −1) during NMI error recovery. The highest priority −2 is used for refresh.

The bus arbitration priority is asserted via the ARB0–ARB3 signals by the requesting masters to gain control. Bus granting is assigned by the priority level. During an arbitration cycle no Micro Channel master is allowed to drive the bus.

The bus can be preempted by the 82307 when arbitrating on behalf of DMA, or when it is requested to run a refresh cycle, or to respond to NMI error recovery. The preempting of the bus can also be initiated by Micro Channel masters.

The CACP Control Port 090H is integrated on chip.

Micro Channel REFRESH ADDRESS GENERATION/CYCLING

The actual refresh request is generated by the 82309 Address Bus Controller. Upon receiving this request the 82307 DMA Controller gains bus control and executes the refresh cycle. Address generation for the Micro Channel refresh cycle is generated by the 82307 DMA controller.

NUMERICS COPROCESSOR INTERFACE

The 82307 DMA controller supports the numerics coprocessor interface. It provides software transparency required to interface an 80387 to 80386 processor. Ports F0H and F1H are integrated on the 82307.

The numerics coprocessor interface support includes the chip select decode for coprocessor internal register accesses of addresses F8H, FAH and FCH. The 82307 also alerts the CPU of any coprocessor error output generated by asserting the interrupt request IRQ13.

ADDRESS DECODER

The Address Decoder logic decodes the chip select for the 8259 Interrupt Controllers and generates POS Address Space output for addresses 100H through 107H to support the Card set-up signals for the expansion slots.

The chip select output is for both 8259s in the system, so it must be externally gated with local channel address bit A7 to select each actual device.

For programming and register level details, please refer to IBM PS/2 Technical Reference Manual.

82307 DMA/Micro Channel Arbitration Controller Pin Definitions

Signal Name	Pin Number	I/O	Description
A<0:23>	13-2, 130-124, 122-118	A0-A15 B A16-A23 O	Processor local address bus. A16-A23 are output only and are driven when the DMA controller is bus master. A0-A15 are bi-directional. They are inputs when the CPU is master, allowing the CPU access to the chip's internal ports. They are outputs when the DMA is master.
D<0:15>	18-21, 23-31, 35-37	B	Processor local data bus. When the DMA is master, it drives this bus in a write cycle, and samples it during a read cycle. When the CPU is master, the bus is used to access DMA's internal registers.
S0#, S1#	87, 85	B	CPU or DMA cycle status indicators. The DMA drives these signals when it is bus master. When a slave, the DMA inputs these signals to track CPU cycles.
BHE#	84	O	Byte high enable. It is driven when the DMA owns the bus and tristated otherwise. This signal ties directly to the CPU BHE# output in an 80386SX machine.
PM/IO#	81	B	CPU memory / I/O indicator. The DMA drives PM/IO# when bus master, and inputs it when it is slave.
US0#, US1#	43, 44	I	Micro Channel status pins. Generated by the Bus controller when the CPU or DMA is master. When a slot-resident master owns the bus, it generates US0M# and US1M#, and the DMA inputs these so as to recognize when the slot-resident master relinquishes the bus. (The slot-resident master end-of-transfer is recognized when US0M#, US1M#, the channel CMD# signal, and the channel BURST# signal are all negated.)
OARB0-OARB3	58-55	O	DMA/CACP arbitration bus outputs. These signals are driven by the DMA/CACP to arbitrate on behalf of a floppy disk service at priority level 2.
PBA#	107	O	Processor Bus Access. The signal indicates a CPU bus access to the numeric coprocessor or to one of the DMA/CACP registers.
ARB3-ARB0	59-62	I	DMA/CACP arbitration bus inputs. These signals tie directly to the Micro Channel. All competing masters including the DMA/CACP drive these during an arbitration cycle, and the master with the highest priority takes control of the Micro Channel after the arbitration cycle is complete.
OPMT#	92	O	Preempt Bus Master. DMA/CACP drives this output whenever it wishes to preempt the current bus master. This can occur when arbitrating on behalf of a DMA channel service or when arbitrating on behalf of a refresh request, or when arbitrating on behalf of the CPU so as to let it respond to a NMI (non-maskable interrupt) request.
PREEMPT#	45	I	Wired "OR" of the PREEMPT# signals from all Micro Channel masters, including the DMA/CACP (PMTO#). It signifies that a master wishes to force an arbitration cycle.
ARB/GNT#	63	O	Arbitration Cycle indicator. The DMA/CACP drives this Micro Channel signal high to signify an arbitration cycle. During the arbitration cycle, all competing masters drive their priorities onto the arbitration bus (ARB03-ARB00). The falling edge of ARBGNT# signifies the end of the arbitration cycle, at which time the master with the highest priority takes control of the bus. If no master competes for the bus, the pullups on ARB03-ARB00 will read binary 1111 by default, which is the normal operating priority of the CPU.

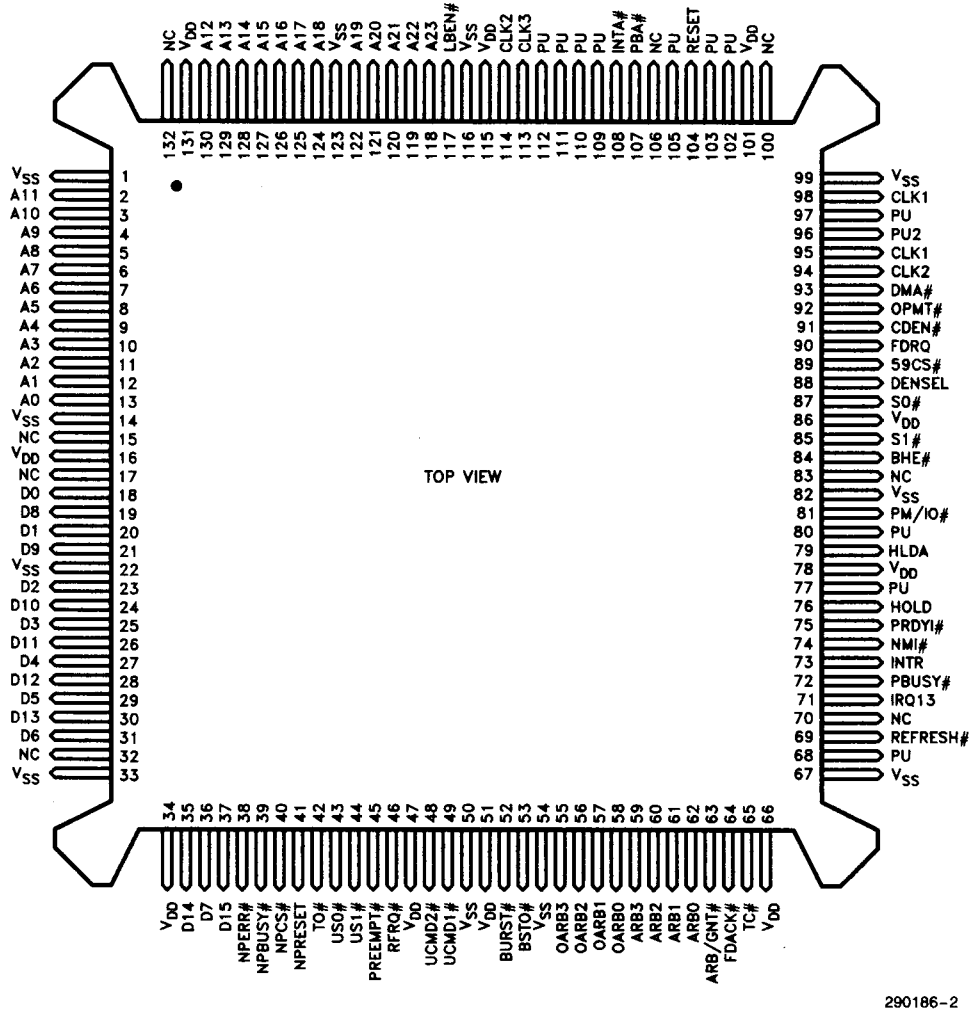
82307 DMA/Micro Channel Arbitration Controller Pin Definitions (Continued)

Signal Name	Pin Number	I/O	Description
BSTO#	53	O	Burst Output. The DMA/CACP drives this output in order to own the Micro Channel for multiple cycles. Specifically, since all PS/2 DMA cycles are two-cycle, BSTO# is driven to allow the DMA controller to own the bus for both halves of a two-cycle transfer.
BURST#	52	I	Burst Request Input. It is an input to the CACP from the current master wishing to own the bus for multiple cycles. It is derived by "OR"ing the Micro Channel BURST# signal with the DMA/CACP BSTO# signal.
HOLD, HLDA	76, 79	(HOLD = O) (HLDA = I)	Hold/Hold Acknowledge to the CPU.
FDRQ, FDACK#	90, 64	(FDRQ = I) (FDACK# = O)	Floppy DMA Request, Acknowledge signals. The motherboard FDC requests DMA service via FDRQ. In response, the DMA/CACP arbitrates for the Micro Channel on behalf of the floppy disk system. Once the DMA/CACP has gained control of the bus, it acknowledges the FDC via FDACK#.
TC#	65	O	DMA Transfer Complete.
UCMD1#, UCMD2#	49, 48	I	Micro Channel Command Inputs. These inputs are driven directly by the Micro Channel CMD# signal.
RFRQ#	46	I	Refresh Cycle Request from the Address Bus Controller.
REFRESH#	69	O	Refresh Cycle Signal. The DMA/CACP drives this output active during refresh cycles. This signal is buffered to become the Micro Channel REFRESH# signal.
59CS#	89	O	Interrupt Controller Chip Select (8259s). Note that this output is activated if either interrupt controller is selected. It is then externally gated with the local I/O channel address bit A7 to distinguish between controller 1 and controller 2.
DENSEL	88	I	Density Selected for the motherboard FDC
CDEN#	91	O	Card Setup Enable. During system setup, a bit pattern is written to port 96H to select a particular slot for configuration. CDEN# enables the decode of these bits to send an active CDSETUP# signal to the selected slot. CDEN# is simply a combinatorial (non-clocked) decode of ports 100H–107H.
CLK1, CLK2, CLK3	95, 98, 94, 114, 113	I	Clock Inputs
RESET	104	I	Power-up System Reset
INTR, INTA#	73, 108	I	Interrupt Request/Acknowledge. The PS/2's 8259 based interrupt system generates interrupt requests to the CPU via INTR. In response, the CPU fetches the appropriate interrupt vector from the interrupt controller in an interrupt acknowledge cycle. The Bus controller decodes the CPU status outputs, and drives INTA# to identify a CPU interrupt acknowledge cycle. The DMA/CACP monitors this activity via its INTR and INTA# inputs. In response to INTA#, the DMA/CACP drives LBEN# so as to enable the 8259 vector onto the Micro Channel. The CACP uses INTR to ensure that the CPU has an opportunity to service an interrupt within one "fairness" cycle; i.e., it prevents the CPU from being totally locked out by higher priority arbiters.

82307 DMA/Micro Channel Arbitration Controller Pin Definitions (Continued)

Signal Name	Pin Number	I/O	Description
NMI#	74	B	Non-Maskable Interrupt to force arbitration cycle to allow CPU bus ownership. As an output, this appears to the system as an open drain, which allows for an external wire "OR" with other NMI sources.
PRDYI#	75	I	Processor Ready Input. The Bus controller generates this signal to terminate CPU and DMA cycles.
NPCS#	40	O	Chip select for the Numeric Coprocessor. It is an unlatched decode that acts as a chip select for CPU accesses to the numeric coprocessor's internal registers.
NPRESET	41	O	Numeric Coprocessor Reset. It resets the numeric coprocessor either upon a system reset or under software control.
NPERR#	38	I	Numeric Coprocessor Error Input. It is an input from the numeric coprocessor error output. The DMA/CACP uses it to generate an interrupt request (IRQ13) to inform the CPU of a coprocessor error.
NPBUSY#	39	I	Numeric Coprocessor Busy
PBUSY#	72	O	Processor Busy Output. It drives the CPU numeric coprocessor busy input. It is activated normally when the coprocessor is busy executing an instruction, but is also activated when a coprocessor error is detected. The CPU will not attempt to utilize the coprocessor as long as PBUSY# is active.
IRQ13	71	O	Numeric Coprocessor Error Interrupt
LBEN#	117	O	Local Bus Enable. This signal is used to enable the data buffers between the Micro Channel and local I/O bus. It is activated for decoded accesses to the 8259 interrupt controllers, as well as for interrupt acknowledge cycles. It is also driven during the DMA acknowledge cycle to the FDC.
DMA#	93	O	DMA/CACP as the Bus Master. It is driven low at the end of an arbitration cycle (ARB/GNT# falling) to indicate that the DMA controller has gain control of the Micro Channel. It is negated during arbitration cycles, and is negated when either the CPU or slot-resident master owns the bus. It is also negated during refresh cycles.
TO#	42	O	Bus Timeout signal. The DMA/CACP also issues an NMI to the CPU in response to the Bus timeout, and forces an arbitration cycle.
V_{DD}	16, 34, 47, 51, 66, 78, 86, 101, 115, 131		Power
V_{SS}	1, 14, 22, 33, 50, 54, 67, 82, 99, 116, 123		Ground
NC	15, 17, 32, 70, 83, 100, 106, 132		No Connect
PU	68, 77, 80, 97, 102, 103, 105, 109–112	I	Pull Up
PU2	96	I	Pull Up. This input must have its own pullup.

82307 DMA/Micro Channel Arbitration Controller



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NOTES:
Important!! No other node allowed to share pull-up with PU2.
NC = No Connect
PU = Pull-Up
—Pull-Up Resistor Value = 2K to 10K
—No more than three nodes to a single pull-up resistor.

82307 PARAMETRICS

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Case Temperature under Bias .... −40°C to +85°C
Storage Temperature ..... −65°C to +150°C
Voltage to Any Pin with Respect to Ground ..... −0.3V to (V_{CC} + 0.3)V
DC Supply Voltage (V_{CC}) ..... −0.3V to +7.0V
DC Input Current ..... ±10 mA

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

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D.C. CHARACTERISTICS

T_C = 0°C to +70°C, V_{CC} = 5V ±10%

Symbol	Parameter	Min	Max	Units	Conditions
V_{IL}	Input Low Voltage		0.8	V	
V_{IH}	Input High Voltage	2.0		V	
V_{IL}	Input Low Voltage		0.8	V	CLK1, CLK2, CLK3
V_{IH}	Input High Voltage	V_{CC} − 0.8		V	CLK1, CLK2, CLK3
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = 2 mA
I_{CC}	Power Supply Current		180	mA	No DC Loads
I_{LI}	Input Leakage Current		±10	μA	$V_{SS} < V_{IN} < V_{CC}$
I_{OZ}	Tri-State Output Leakage Current		±10	μA	$V_{SS} < V_{OUT} < V_{CC}$

82307 DMA CONTROLLER A.C. SPECS

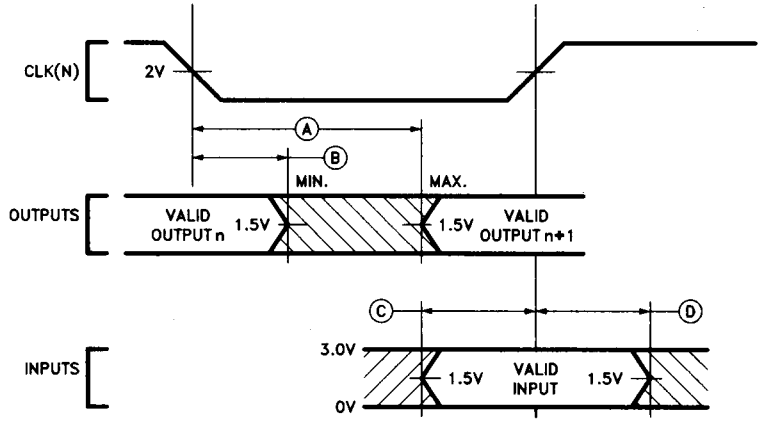
T_C = 0°C to +70°C, V_{CC} = 5V ±10%

Symbol	Parameter	Kit 16 MHz		Kit 20 MHz		Kit 25 MHz		C_L (pF)	Notes
		Min	Max	Min	Max	Min	Max		
T1	CLK1, CLK2, CLK3 LOW TIME	15		15		14			
T2	CLK(N) NON-OVERLAP TIME	4		4		0			
T3	RESET(IN), NPRESET(OUT) PULSE WIDTH	500		500		500		50	
T4	TO# PULSE WIDTH	60		60		60		50	
T5	A23–A0, PM/IO#, BHE#, REFRESH# DELAY	4	35	4	35	4	32	75	
T6	A23–A0, PM/IO#, BHE#, STATUS FLOAT DELAY	4	40	4	40	4	40	75	
T7	WRITE DATA VALID DELAY	2	35	2	35	2	28	75	
T8	WRITE DATA FLOAT DELAY	2	40	2	35	2	35	75	
T9	READ DATA SETUP TIME	15		13		11			
T10	READ DATA HOLD TIME	4		4		4			
T11A	STATUS VALID DELAY (TPHL)	2	25	2	25	2	20	75	
T11B	STATUS VALID DELAY (TPLH)	2	35	2	35	2	30	75	
T12	ADDR-TO-STATUS SETUP	35		27		22		75	
T13A	PRDYI# SETUP TIME	25		20		20			2, 3
T13B	PRDYI# SETUP TIME	8		8		8			2, 3
T14	PRDYI# HOLD TIME	5		5		5			2
T15	A15–A0, PM/IO# SETUP TIME	35		35		35			
T16	A15–A0, PM/IO# HOLD TIME	10		10		10			
T17	STATUS SETUP TIME	26		26		24			
T18	STATUS HOLD TIME	10		10		10			
T19	WRITE DATA SETUP TIME	25		25		25			1
T20	WRITE DATA HOLD TIME	25		25		25			1
T21	READ DATA VALID DELAY	2	100	2	100	2	100	75	
T22	READ DATA FLOAT DEALY	8	40	8	35	8	35	75	
T23	HOLD DELAY	2	35	2	32	2	32	50	
T24	ARB/GNT# DELAY FROM EOT	30		30		30		50	
T25	ARB/GNT# PULSE WIDTH	6 × CLK3		6 × CLK3		6 × CLK3		50	4
T26	OARB3–OARB0 DELAY		32		32		32	50	
T27	OPMT# INACTIVE DELAY		35		35		35	50	
T28	BSTO# DELAY	2	40	2	40	2	40	50	
T29	TC# DELAY	2	36	2	33	2	33	50	
T30	FDACK#, DMA# DELAY	2	40	2	40	2	40	50	
T32	LBEN# VALID DELAY	0	35	0	35	0	35	50	
T33	CDEN# VALID DELAY	2	35	2	35	2	35	25	
T34	NPCS# DELAY	2	65	2	65	2	50	50	
T35	59CS# VALID DELAY	6	42	6	42	6	42	50	
T36	PBA# DELAY	2	45	2	45	2	45	50	

NOTES:

1. Write data is sampled on different clock edges by different DMA internal registers. T19 is speced relative to the earliest sampling edge, while T20 is relative to the latest edge.
2. PRDYI# must be inactive and stable according to these specs at all DMA state boundaries except at the end of the TC boundary at which the cycle is to be terminated.
3. T13A must be met to insure the 82307 properly recognizes PRDYI# at the end of the cycle. T13B must be met to insure that status (S0#, S1#) activation is not delayed if the 82307 has a cycle pending and will move directly into a TS state upon completion of the current cycle. If T13B is not met, the status valid delay (T11A) may no longer apply since PRDYI# rather than CLK1 may gate status activation.
4. T25 is specified as 3 times the CLK3 period. This is a typical value which is not tested. Also, this spec does not comply with Micro Channel timings at 25 MHz. To remedy this situation, external hardware, such as the PAL used in the 82311 Designer's Guide, must be implemented in order to guarantee T25's compatibility with Micro Channel specifications.

DRIVE LEVELS AND MEASUREMENT POINTS FOR A.C. SPECIFICATIONS



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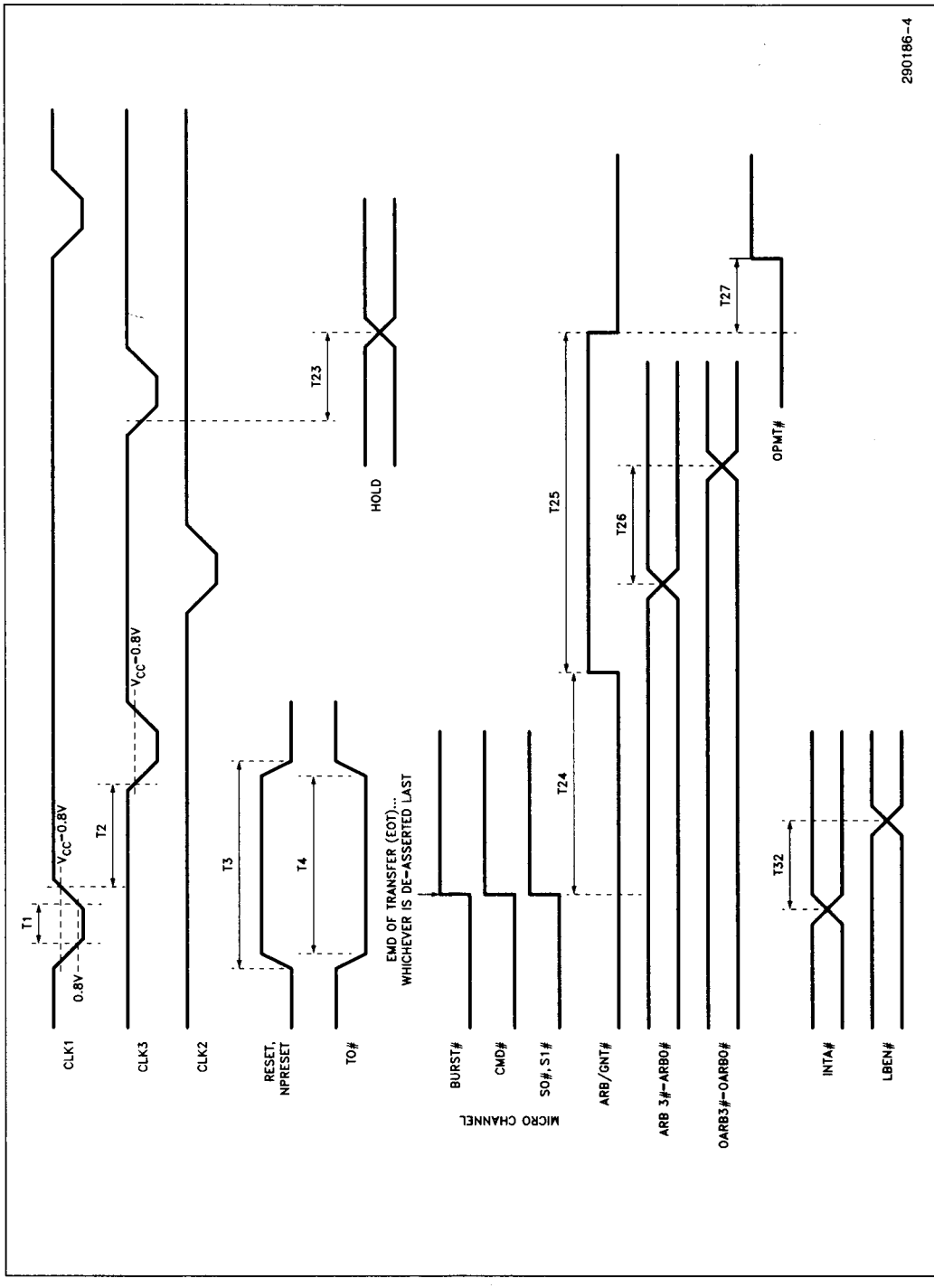
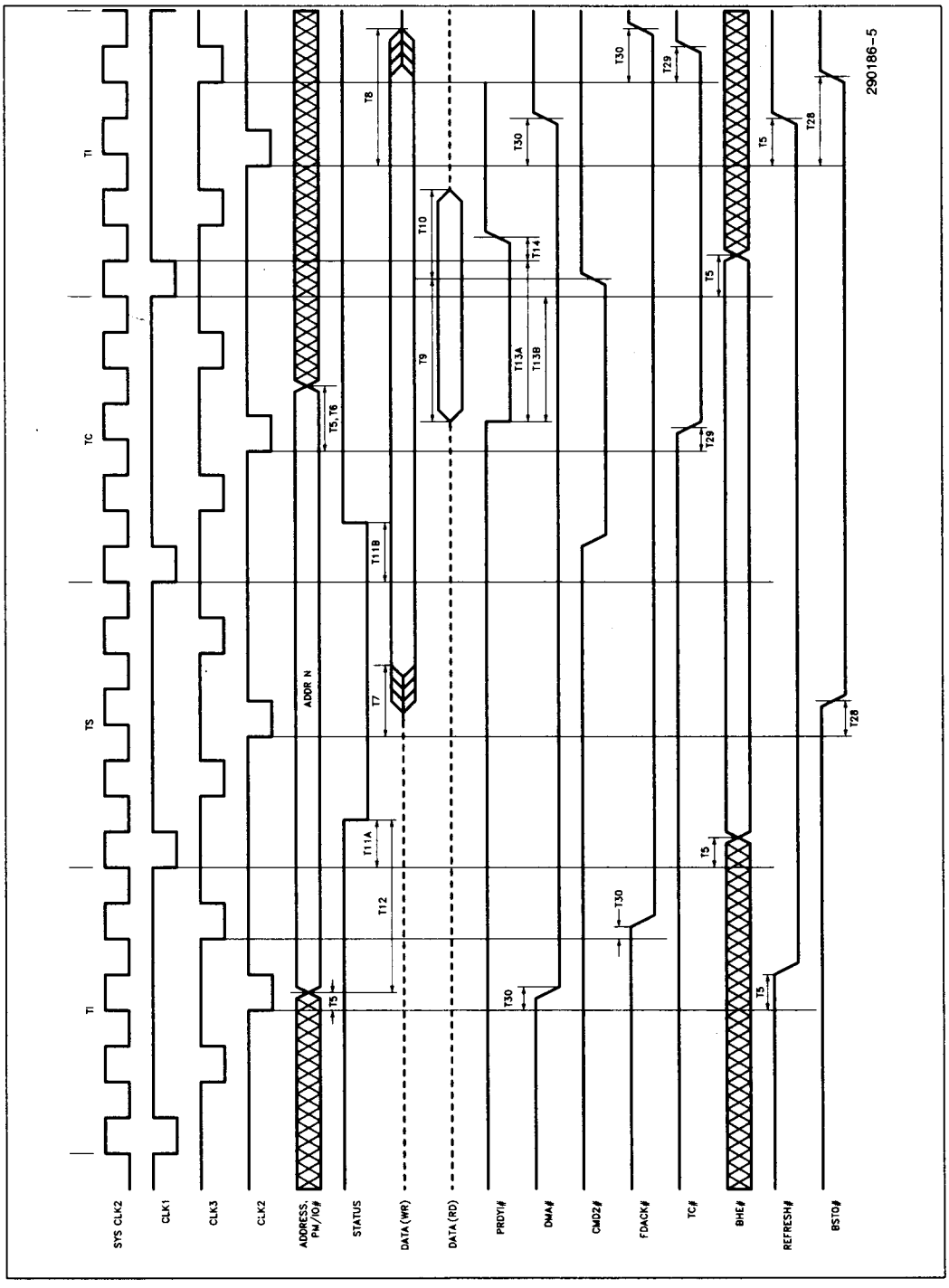
LEGEND:
A. Maximum Output Delay Specification.
B. Minimum Output Delay Specification.
C. Minimum Input Setup Specification.
D. Minimum Input Hold Specification.

Input waveforms have tr ≤ 2.0 ns from 0.8V to 2.0V.

SYSTEM TIMINGS



DMA ... MASTER MODE



DMA ... SLAVE MODE