3.3V/5V, Single-Channel 500mA Current-Limited Power Distribution Switch

DESCRIPTION

The MP62055 Power Distribution Switch features internal current limiting to prevent damage to host devices due to faulty load conditions. The MP62055 analog switch features $115m\Omega$ on-resistance and operates from 2.7V to 5.5V input. It is available with a guaranteed current limit, making it ideal for load switching applications. The MP62055 has builtin protection for both over current and increased thermal stress. For over current, the device will limit the current by changing to a constant current mode.

As the temperature increases as a result of short circuit, the device will shut off. The device will recover once the device temperature reduces to approx 120°C.

The MP62055 is available in a TSOT23-5 package.

FEATURES

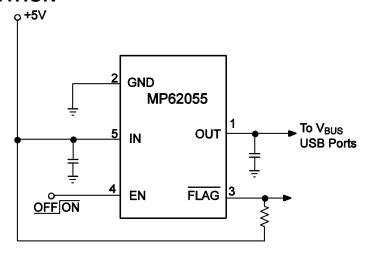
- 500mA Continuous Current
- Accurate Current Limit
- 2.7V to 5.5V Supply Range
- 90uA Quiescent Current
- 115mQ MOSFET
- Thermal-Shutdown Protection
- Under-Voltage Lockout
- 8ms FLAG Deglitch Time
- No FLAG Glitch During Power Up
- Reverse Current Blocking
- TSOT23-5 Package
- UL File # E322138

APPLICATIONS

- Smartphone and PDA
- Portable GPS Device
- Set-top-box
- USB Power Distribution

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TYPICAL APPLICATION



SINGLE-CHANNEL



UL Recognized Component



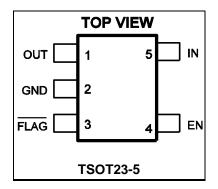
ORDINARY INFORMATION

| Part Number | Enable | Switch | Maximum Continuous Load Current | Typical Short- Circuit Current @ T _A =25℃ | Package | Top Marking | Free Air Temperature (T _A) |
|-------------|----------------|--------|---------------------------------------|--|----------|----------------|--|
| MP62055EJ | Active High | Single | 500mA | 1100mA | TSOT23-5 | 6G | -40°C to +85°C |

^{*} For Tape & Reel, add suffix -Z (e.g. MP62055EJ-Z).

For RoHS Compliant Packaging, add suffix -LF (e.g. MP62055EJ-LF-Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

| IN | 0.3V to +6V |
|---|------------------------------|
| EN, FLAG, OUT to GND | 0.3V to +6V |
| Continuous Power Dissipation | $(T_A = +25^{\circ}C)^{(2)}$ |
| | 0.56W |
| Junction Temperature | |
| Lead Temperature | 260°C |
| Storage Temperature | 65°C to +150°C |
| Operating Junct. Temp (T _J) | 40°C to +125°C |

| Thermal Resistance (3) | $oldsymbol{	heta}_{JA}$ | $\boldsymbol{\theta}_{JC}$ | |
|------------------------|-------------------------|----------------------------|------|
| TSOT23-5 | 220 | 110 | °C/W |

- 1) Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-toambient thermal resistance θ_{JA} , and the ambient temperature TA. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D(MAX) = (T_J(MAX) - T_J(MAX))$ T_A)/ θ_{JA} . Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage Measured on JESD51-7 4-layer PCB.



ELECTRICAL CHARACTERISTICS (4)

V_{IN}=5V, T_A=+25°C, unless otherwise noted.

| Parameter | Condition | Min | Тур | Max | Units |
|---|--|------|-----|------|-------|
| IN Voltage Range | | 2.7 | | 5.5 | V |
| Supply Current | Single Channel | | 90 | 120 | μA |
| Shutdown Current | Device Disable, V _{OUT} =float, V _{IN} =5.5V | | 1 | | μA |
| Off Switch Leakage | Device Disable, V _{IN} =5.5V | | 1 | | μA |
| Current Limit | | 550 | | 1100 | mA |
| Trip Current | Current Ramp (slew rate≤100A/s) on Output | | 1 | 1.4 | А |
| Under-voltage Lockout | Rising Edge | 1.95 | | 2.65 | V |
| Under-voltage Hysteresis | | | 250 | | mV |
| FET On Resistance | I _{OUT} =100mA, and -40°C <t<sub>A<85°C</t<sub> | | 115 | 168 | mΩ |
| EN Input Logic High Voltage | | 2 | | | V |
| EN Input Logic Low Voltage | | | | 0.8 | V |
| FLAG Output Logic Low Voltage | I _{SINK} =5mA | | | 0.4 | ٧ |
| FLAG Output High Leakage Current | V _{IN} =V _{FLAG} =5.5V | | | 1 | μA |
| Thermal Shutdown | | | 140 | | °C |
| Thermal Shutdown Hysteresis | | | 20 | | °C |
| V _{OUT} Rising Time, Tr ⁽⁵⁾ | $V_{IN}=5.5V, C_{L}=1\mu F, R_{L}=11\Omega$ | | 0.9 | | ms |
| | $V_{IN}=2.7V, C_{L}=1\mu F, R_{L}=11\Omega$ | | 1.7 | | ms |
| V _{OUT} Falling Time, Tf (5) | V_{IN} =5.5V, C_L =1 μ F, R_L =11 Ω | | | 0.5 | ms |
| | V_{IN} =2.7V, CL=1 μ F, R _L =11 Ω | | | 0.5 | ms |
| Turn On Time, Ton (6) | $C_L = 100 \mu F, R_L = 11 \Omega$ | | | 3 | ms |
| Turn Off Time, Toff (6) | C_L =100 μ F, R_L =11 Ω | | | 10 | ms |
| FLAG Deglitch Time | | 4 | 8 | 15 | ms |
| EN Input Leakage | | | 1 | | μA |
| Reverse Leakage Current | OUT=5.5V, IN=GND | | 0.2 | | μΑ |

NOTE:

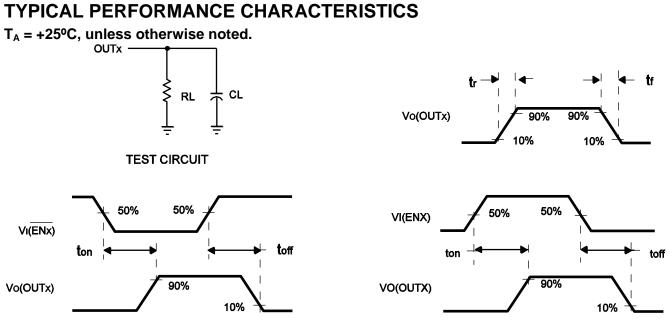
 ⁴⁾ Production test at +25°C. Specifications over the temperature range are guaranteed by design and characterization.
 5) Measured from 10% to 90%.

⁶⁾ Measured from (50%) EN signal to (90%) output signal.



PIN FUNCTIONS

| Pin# | Name | Description |
|------|------|---|
| 1 | OUT | Power-Distribution Switch Output. |
| 2 | GND | Ground |
| 3 | FLAG | IN-to-OUT Over-current, active-low output flag. Open-Drain. |
| 4 | EN | Enable Input. Active High. |
| 5 | IN | Input Voltage. Accepts 2.7V to 5.5V input. |

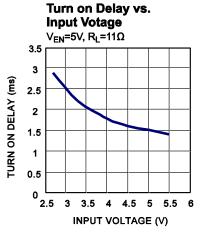


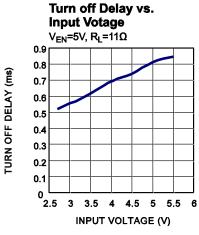
VOLTAGE WAVEFORMS Figure 1—Test Circuit and Voltage Waveforms

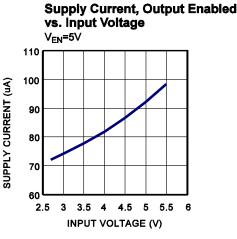


TYPICAL PERFORMANCE CHARACTERISTICS

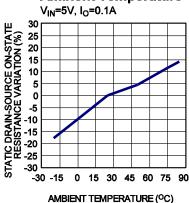
 $V_{IN}=5.5V$, $C_L=2.2\mu F$, $T_A=+25^{\circ}C$, unless otherwise noted.



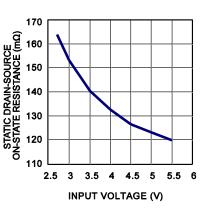




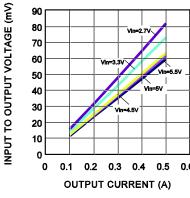
Static Drain-Source On-State Resistance Variation vs. Ambient Temperature



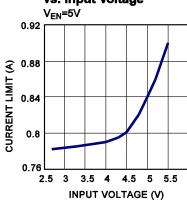
Static Drain-Source On-State Resistance vs. Input Voltage V_{EN}=5V, I_{OUT}=0.5A



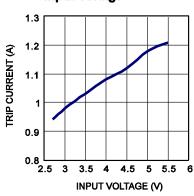
Input to Output Voltage vs. Load Current V_{EN}=5V



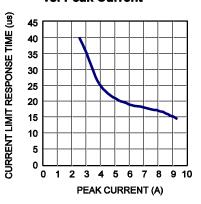
Current Limit vs. Input Voltage







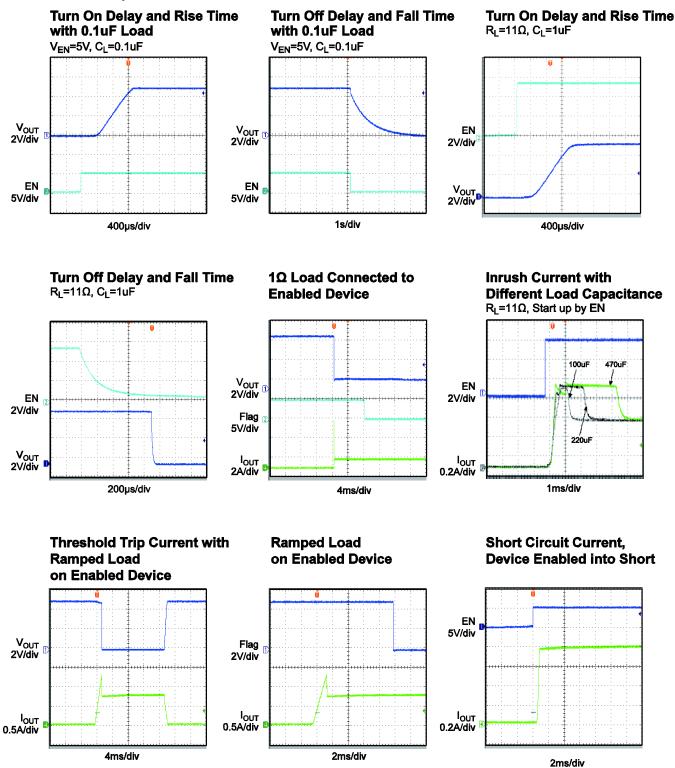
Current Limit Response Time vs. Peak Current





TYPICAL PERFORMANCE CHARACTERISTICS (continued)

 V_{IN} =5.5V, C_L = 2.2 μ F, T_A = +25 $^{\circ}$ C, unless otherwise noted.





FUNCTION BLOCK DIAGRAM

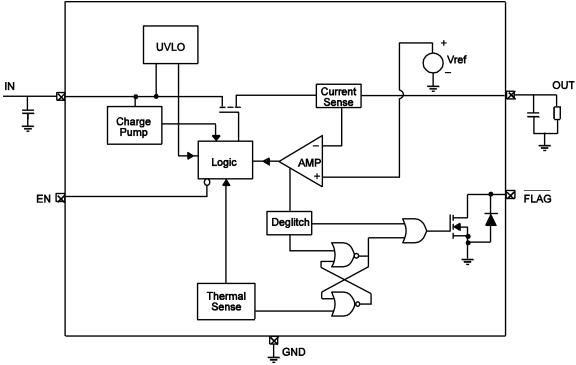


Figure 2—Functional Block Diagram

DETAILED DESCRIPTION

Over Current

When the load exceeds trip current (minimum threshold current triggering constant-current mode) or a short is present, MP62055 switches into to a constant-current mode (current limit value). MP62055 will be shutdown only if the overcurrent condition stays long enough to trigger thermal protection.

Trigger overcurrent protection for different overload conditions occurring in applications:

- The output has been shorted or overloaded before the device is enabled or input applied. MP62055 detects the short or overload and immediately switches into a constant-current mode.
- 2) A short or an overload occurs after the device is enabled. After the current-limit circuit has been tripped (reached the trip current threshold), the device switches into constantcurrent mode. However, high current may flow for a short period of time before the current-limit circuit can react.

3) Output current has been gradually increased beyond the recommended operating current. The load current rises until the trip current threshold is reached or until the thermal limit of the device is exceeded. The MP62055 is capable of delivering current up to the trip current threshold without damaging the device. Once the trip threshold has been reached, the device switches into its constant-current mode.

Flag Response

The FLAG pin is an open drain configuration. This FAULT will report a fail mode after an 8ms deglitch timeout. This is used to ensure that no false fault signals are reported. This internal deglitch circuit eliminates the need for extend components. The FLAG pin is not deglitched during an over temp. or a voltage lockout.



Thermal Protection

The purpose of thermal protection is to prevent damage in the IC by allowing exceptive current to flow and heating the junction. The die temperature is internally monitored until the thermal limit is reached. Once this temperature is reached, the switch will turn off and allow the chip to cool. The switch has a built-in hysteresis.

Under-voltage Lockout (UVLO)

This circuit is used to monitor the input voltage to ensure that the MP62055 is operating correctly. This UVLO circuit also ensures that there is no operation until the input voltage reaches the minimum spec.

Enable

The logic pin disables the chip to reduce the supply current. The device will operate once the enable signal reaches the appropriate level. The input is compatible with both COMS and TTL.

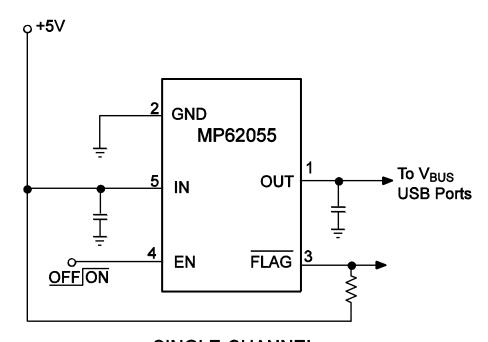


APPLICATION INFORMATION

Power-Supply Considerations

Over $10\mu F$ capacitor between IN and GND is recommended. This precaution reduces power-supply transients that may cause ringing on the input and improves the immunity of the device to short-circuit transients.

In order to achieve smaller output load transient ripple, placing a high-value electrolytic capacitor on the output pin(s) is recommended when the load is heavy.

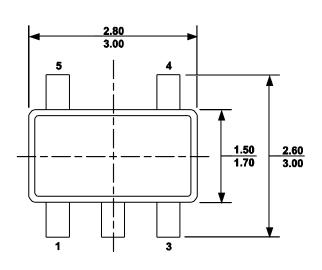


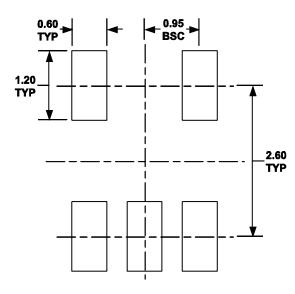
SINGLE-CHANNEL
Figure 3—Application Circuit



PACKAGE INFORMATION

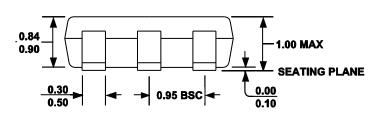
TSOT23-5

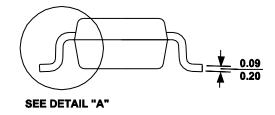




TOP VIEW

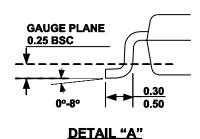
RECOMMENDED LAND PATTERN





FRONT VIEW

SIDE VIEW



NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
- 5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AA.
- 6) DRAWING IS NOT TO SCALE.

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